Design Impact of Positive Temperature Dependence of Drain Current in Sub 1V CMOS VLSI's

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Abstract

In sub 1V CMOS designs, especially around 0.5V CMOS designs, the on-state drain current of MOSFET's shows positive temperature dependence, being different from the negative temperature dependence in the conventional voltage designs. Together with the low threshold voltage less than 0.2V in the low-voltage CMOS, a possibility of temperature instability increases. The paper describes possible temperature instabilities in the low-voltage regime by using circuit simulation environments incorporating temperature change in time and experiments using MOSFET's and 32-bit adder circuit in quarter micron CMOS technology with low threshold voltage of 0.25V.

Introduction

Recently, low-power, high-performance VLSI design is attracting much attention due to the emerging needs for portable multimedia equipments and heat problems for high-end processors. Since the dynamic power component of CMOS digital circuit is proportional to the square of the supply voltage, V_{DD}, the scaling of V_{DD} is very effective to reduce the power dissipation. The low V_{DD} CMOS, however, suffers from large delay [1] and the low threshold voltage less than 0.2V is used [2] to mitigate the delay degradation, since the delay is expressed as follows.

$$\text{Delay} \propto \frac{CV_{DD}}{I} \propto \frac{CV_{DD}}{(V_{DD} - V_T)^\alpha}, \quad (1)$$

where I_D is the drain current, V_T is the threshold voltage and α denotes the velocity saturation index whose typical value is around 1.3 for short-channel MOSFET's [3]. From the discussions above, the low-power design in the future tends to use low-V_{DD} and low-V_T.

It has been reported in [4] that the temperature dependence is a function of V_{DD} and at around 1V, the temperature dependence is minimized. Historically speaking, this zero temperature coefficient (ZTC) point has been recognized as an important voltage by analog designers for a long time. It is predicted, however, in the SIA roadmap [5] that in the year 2010, the main stream supply voltage will be around 0.6V and 0.5V circuit implementation is getting focus recently [6]. The voltage is much smaller than the ZTC point and the positive temperature dependence of drain current is observed in the region. The impact of the positive temperature dependence in this low-voltage regime has not been investigated. This paper reports the design implications of the positive temperature dependence using temperature-varying circuit simulation environments and through measurements for the first time.

Temperature Dependence of On Current

The drain current of MOSFET, I_D, is expressed as follows.

$$I_D \propto \mu(T)(V_{DD} - V_T(T))^\alpha \quad (2)$$

The threshold voltage $V_T(T)$ and the mobility $\mu(T)$ have temperature dependence [4].

$$V_T(T) = V_T(T_0) - \kappa(T - T_0) \quad (3)$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \quad (4)$$

where T is the temperature, T_0 is the room temperature (T_0=300°K), κ is the threshold voltage temperature coefficient whose typical value is 2.5mV/K and m is the mobility temperature exponent whose typical value is 1.5. It is seen from above expressions that the mobility shows negative dependence on temperature, and V_T decreases as temperature increases.

When temperature increases by 100°K, the threshold voltage decreases typically by 0.25V and the mobility decreases about 35%. .If the V_{DD} is relatively large like 2.5V in the conventional designs, the increase of the drain current by the V_T decrease of 0.25V is only about 10%. This does not surmount the current decrease by the mobility degradation.

On the other hand, if the V_{DD} is 0.5V, the current increase by the V_T decrease is 55% that surmounts the mobility degradation. This leads to the overall positive temperature dependence of on-state current.

The measured drain voltage characteristics for 0.3μm NMOS and PMOS are shown in Figs. 1-4. These figures clearly show negative temperature dependence of the drain

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current on temperature in sub 1V region. The figures also include fitted SPICE model calculation that shows the same temperature dependence with the measurements.

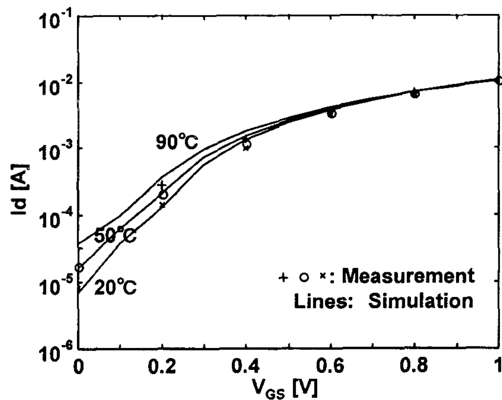

Fig. 1 Measured and simulated temperature dependence of drain current for NMOS under 1V V_{DD}

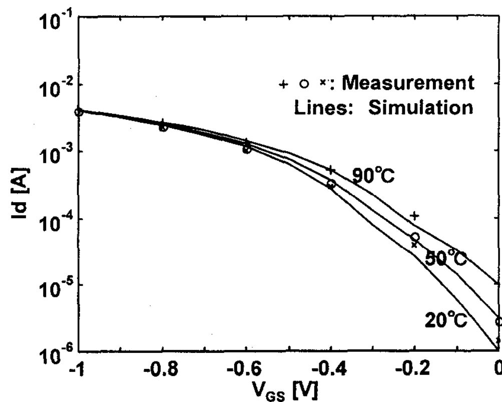

Fig. 2 Measured and simulated temperature dependence of drain current for PMOS under 1V V_{DD}

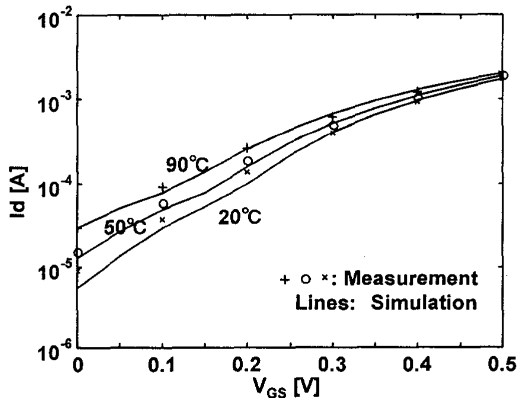

Fig. 3 Measured and simulated temperature dependence of drain current for NMOS under 0.5V V_{DD}

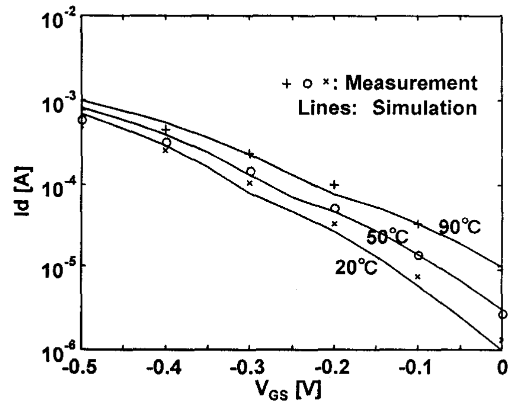

Fig. 4 Measured and simulated temperature dependence of drain current for PMOS under 0.5V V_{DD}

Temperature Varying Circuit Simulation

In order to simulate the temperature effects on the circuit behavior, a simulation environment is developed whose flow chart is shown in Fig. 5. First a SPICE simulation is carried out and then the average power consumption of the circuit, P_{av}, over a small time step, Δt, is calculated using the average current over Δt.

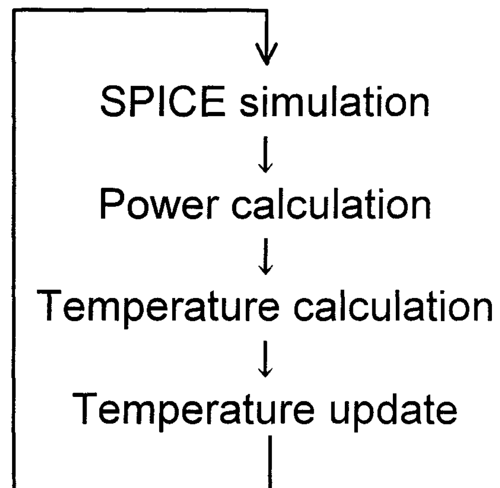

Fig. 5 Flowchart for temperature varying circuit simulation

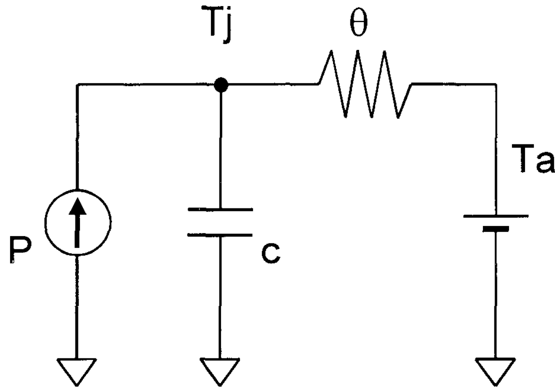

Fig. 6 Power-temperature model

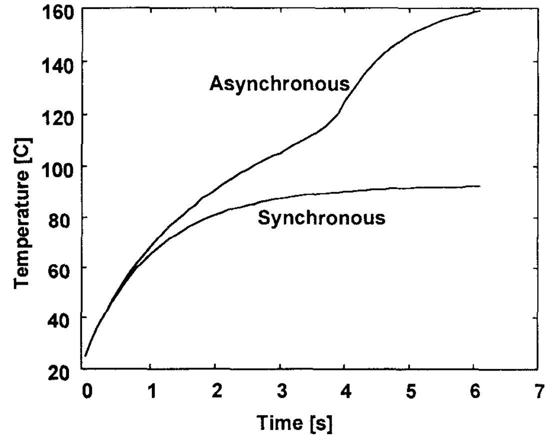

Fig. 7 Temperature varying simulation results of asynchronous circuit (2-input NAND ring osc.) and synchronous circuit (2-input NAND chain put between F/F's)

The temperature change during Δt is calculated by using the first order model shown in Fig. 6. In the model, node voltage corresponds to the temperature. In the figure, T_j signifies the junction temperature and T_a signifies the ambient temperature. θ is the heat resistance of the package, c is the heat capacity of the system. Power consumption of the chip corresponds to the current source. The system has an exponential solution which changes from $T_{j,initial}$ to $T_a + \theta P$ with a time constant of $c\theta$ if the power consumption is constant.

$$T_j = (T_a + \theta P_{av}) + (T_{j,initial} - T_a - \theta P_{av}) \exp\left(-\frac{\Delta t}{c\theta}\right) \quad (5)$$

Now that the new temperature is calculated using the above formula, the temperature is updated by using .TEMP statement in SPICE and the simulation is carried out using the new temperature. This loop is iterated. All procedures are automated using Perl scripts in the environments.

Figures 7 shows simulation results for asynchronous circuit and synchronous circuit. In the asynchronous circuit, when the drain current increases, the frequency of the circuit increases as is predicted by Eq.(1) and hence the dynamic power component, $afCV^2$, increases. This results in higher operating temperature and positive feedback in temperature occurs. The abnormal kink at about 120°C is due to the fact that 'L' and 'H' voltage begin to deviate from V_{SS} and V_{DD} and signal swing is reduced so that the speed of the circuit increases. Above the kink, since the static margin of the circuit is small, it is not practical to operate the circuit.

On the other hand, in the synchronous circuit, although the frequency does not change, the subthreshold component of the power increases and may become dominant, since the V_T decreases about 0.2V from the room temperature to 100°C. When the subthreshold power becomes dominant, the power gets to have highly positive dependence on temperature and the temperature positive feedback takes in. The resiliency for the temperature instability is tabulated for various circuit styles.

TABLE I: Resiliency for Temperature Instability

	Synch. Digital	Asynch. Digital	Memory	Analog
High-V_{DD}	H	H	H	H
Low-V_{DD} High-V_T	M	L	L	L
Low-V_{DD} Low-V_T	L	L	L	L

H: High, M: Medium, L: Low

Measurement Results and Discussions

Figure 8 shows a test chip fabricated with a quarter micron CMOS technology with a low threshold voltage of 0.25V. Figure 9 shows the measured temperature dependence of a 32-bit adder. It is seen from the figure that the temperature dependence of the circuit is greater in the low voltage region compared with the relatively high V_{DD} region.

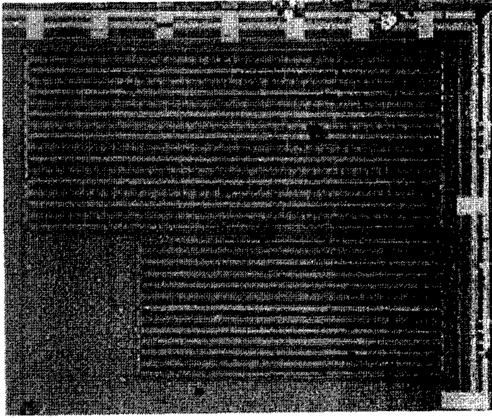

Fig. 8 Microphotograph of test chip

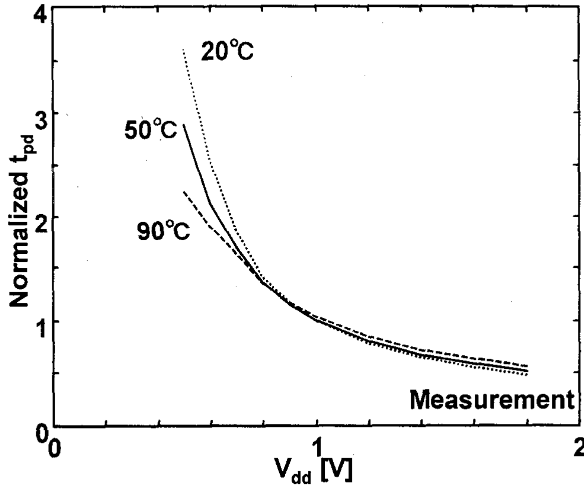

Fig. 9 Measured temperature dependence of 32-bit adder delay

Let us consider the minimum threshold voltage at room temperature, $V_{T0,min}$, which assures to keep the juction temperature less than $T_{j,max}$. The following three equations determines the

$$T_j = T_a + \theta P \tag{6}$$

$$P / N = a f C V_{DD}^2 + V_{DD} I_C \exp\left(-\frac{qV_T}{nkT_j}\right)(\text{sub} - V_T) \tag{7}$$

$$= a f C V_{DD}^2 + V_{DD}\beta|V_T|^{\alpha} \text{ (depletion mode)} \tag{8}$$

$$V_T = V_{T0} - \kappa(T - T_0) \tag{9}$$

where I_c, q/nk, and ß, are constants and N is the number of gates on a chip. When the leakage power is determined by the subthreshold leakage, that is, when the threshold voltage is positive, (7) holds but when the threshold voltage becomes negative, the leakage power is determined by the drain current of the depletion mode MOSFET and (8) holds. In the 0.5V V_{DD} designs, a very low threshold voltage like 0.15V is used and in this case, the (8) is applicable for the high temperature. In this case, $V_{T0,min}$ can be solved as follows.

$$V_{T0,min} = -\left(\frac{T_{j,max} - T_a}{N\theta\beta V_{DD}}\right)^{1/\alpha} + \kappa(T_{j,max} - T_0) \tag{10}$$

When typical values are used, $V_{T0,min}$ can be approximated as follows.

$$V_{T0,min} \approx -\left(\frac{73}{N\theta\beta V_{DD}}\right)^{1/\alpha} + 0.2 \tag{11}$$

It is seen from the expression that the minimum threshold voltage at room temperature should be more than 0.2V with high heat resistance package. 0.2V deviation of the threshold voltage in the high temperature range from the room temperature should be always considered.

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