Low Power and Flexible Braille Sheet Display with Organic FET's and Plastic Actuators

Makoto Takamiya[1], Tsuyoshi Sekitani[2], Yusaku Kato[2], Hiroshi Kawaguchi[3], Takao Someya[2], and Takayasu Sakurai[4]

[1] VLSI Design and Education Center, University of Tokyo, Japan
[2] Quantum-Phase Electronics Center, School of Engineering, University of Tokyo, Japan
[3] Department of Computer and Systems Engineering, Kobe University, Japan
[4] Center for Collaborative Research, University of Tokyo, Japan
E-mail: mtaka@iis.u-tokyo.ac.jp

Abstract

Organic FETs (OFETs) are integrated with actuators, and a Braille sheet display is demonstrated. A newly developed back-gated OFETs SRAM and the circuits technology for the Braille sheet display to enhance speed, yield and lifetime are presented, which will be essential for future large-area electronics made with OFETs.

Introduction

As shown in Table I, flexible and low-cost organic FETs (OFETs) are suitable for large-area applications where functional units are distributed on plastic films, 10 cm – 10 m on a side. An integrated system of OFETs and pressure sensors was reported in [1], and that of OFETs and photodetector was reported in [2]. In this paper, an integrated system of OFETs and plastic actuators is proposed, and a Braille sheet display is demonstrated [3]. Device and process technology of the OFETs and the actuators are shown in [4].

The transition time of the actuator is about 1 s. The Braille sheet display has an actuator array. When the actuator is sequentially driven, it takes more than 1 minute to change the Braille, which is impractical. The OFETs also have several problems. OFETs are chemically degraded by the oxygen and moisture in the atmosphere. Threshold voltage (V_{TH}) control process technology such as an ion implantation is not yet established for OFETs. To increase the speed of the actuator, OFET SRAM and overdrive techniques for a driver transistor is proposed. To achieve a reliable and stable SRAM operation, a V_{TH} control technology using a back gate is developed. 5-transistor SRAM cell is also developed to reduce the number of bit lines and cell area.

Table I Comparison between our organic FETs (OFETs) and the state-of-the-art silicon MOSFETs.

	OFETs	Si MOSFETs
Design rule	50 µm	90 nm
Hardness	Flexible	Solid
Drive current	25 nA / µm @ 40 V	1 mA / µm @ 1 V
Gate delay	0.3 ms	10 ps
Cost / area	Low	High
Cost / transistor	High	Low
Lifetime	Days	Years

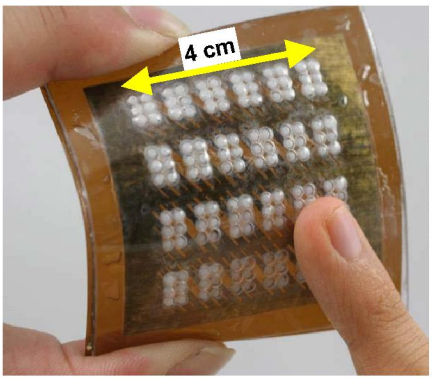


Fig. 1 Braille sheet display.

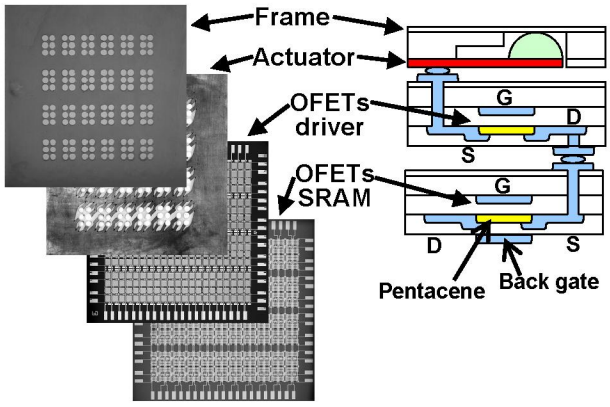


Fig. 2 Device structures for the Braille sheet display. 4 films are stacked.

Braille Sheet Display

Figure 1 shows the developed Braille sheet display. Braille characters in a 6 x 4 array are shown on the 4 cm x 4 cm display. Each Braille character consists of 2 x 3 dots, and the display has a total of 144 dots. The Braille character is changed by moving the dots up and down by means of the actuator, depending on the input data. As shown in Fig. 2, four films (frame, actuator, OFETs driver, and OFETs SRAM) are stacked in the Braille sheet display. Each Braille dot has an OFET SRAM to compensate for the slow transition of the actuator. After the input data are written to all SRAMs, all the actuators are driven at once using the drivers depending on the data. In this way, the time required to

change the whole Braille is reduced.

Key Circuit Technologies

A. 5-Transistor SRAM Cells and Pipelining for Write-Operation

Figure 3 shows the circuit of the SRAM and the driver for one actuator. Only pMOS OFETs are used, because the performance of nMOS OFETs is commonly worse than pMOS. The OFETs for SRAM have back gates [5] to control V_{TH}. A write-only SRAM is enough for our Braille application, because the actuator moves depending on the hold data (DATA, DATAb) and a SRAM read-operation is not required. Therefore, to save the film area, a 5-transistor SRAM cell is developed. Compared with a conventional 6-transistor SRAM cell, a 5-transistor SRAM cell reduces the number of the bit lines by one-half and reduces the SRAM cell area by 20%. Figure 4 shows a micrograph of the 5-transistor SRAM cell. The cell area is 3.7 mm by 2.0 mm. The whole cell is covered with the back gate.

In the 5-transistor SRAM cell, a foremost concern is the slow write-time of DATAb, because DATAb has no access transistors. Our design target for the write-time of the whole SRAM (= 144 cells) is within 2 s. Figure 5 shows the measured waveforms of DATA and DATAb during a write-operation. When BL is low, the transition time of DATAb is 2 ms. In contrast,

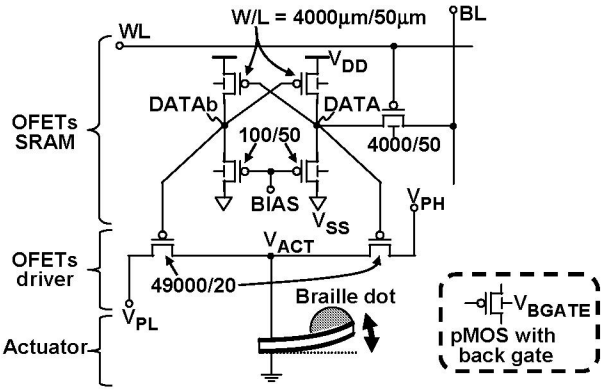


Fig. 3 Circuit of OFETs SRAM and the driver for one actuator.

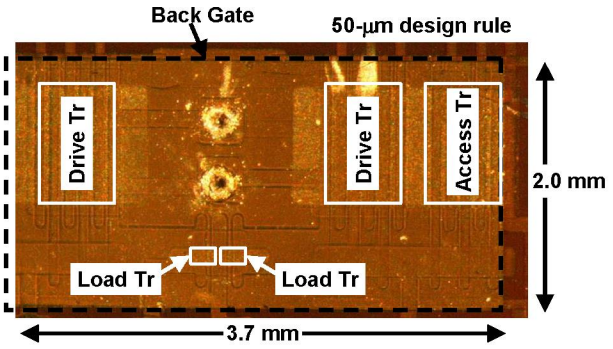


Fig. 4 Micrograph of the 5-transistor SRAM cell.

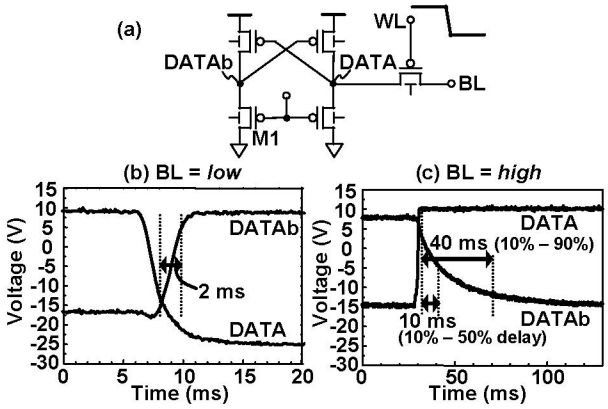


Fig. 5 (a) Measured SRAM circuits. Measured SRAM write-operation when BL is low (b) and high (c).

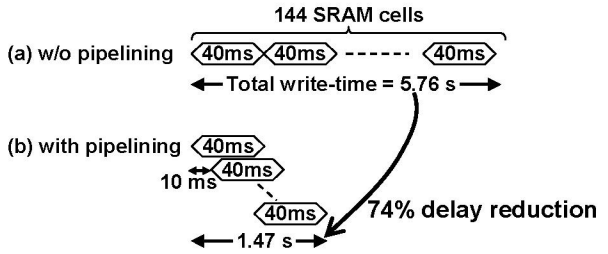


Fig. 6 Timing chart for write-time of SRAM. (a) Without pipelining. (b) With pipelining.

when BL is high, the transition time of DATAb is 40ms, because the drive current of M1 in Fig. 5 is small. This slow transition time can be hidden in the SRAM system-level by pipelining the write-operation. Figure 6 shows the timing chart for the pipeline. By pipelining, the total write-time for the 12 x 12 SRAM cells is reduced from 5.76 s (= 40 ms x 144) to 1.47 s (= 10 ms x 143 + 40 ms), which satisfies our design target.

B. Control of SRAM Static Noise Margin with A Back Gate

The V_{TH} control technology using a back gate is shown to compensate for the immature V_{TH} control process technology and to achieve a reliable SRAM operation. Figure 7 shows $I_D - V_{GS}$ characteristics of a pMOS OFET. Back gate voltage (V_{BGATE}) is varied. Figure 8 shows the measured butterfly curves of the SRAM with varied V_{BGATE}. The static noise margin (SNM) increases as V_{BGATE} increases.

The V_{TH} control technology is also applied to compensate for the chemical degradation of OFETs and to achieve a reliable SRAM operation. Figure 9 shows the measured aging characteristics of the inverter in the SRAM. The OFETs were kept in a nitrogen atmosphere except for the measuring time. As time passes, the inverter characteristics show a rightward shift due to the reduced |Vth| of OFETs. Figure 10 shows the aging characteristics of SNM calculated based to Fig. 9. By compensating the reduced |Vth| of OFETs due to the chemical degradation with the back gate, a constant

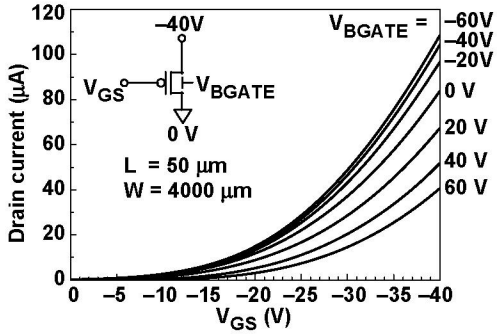


Fig. 7 $I_D - V_{GS}$ characteristics of a pMOS OFET with varied V_{BGATE}.

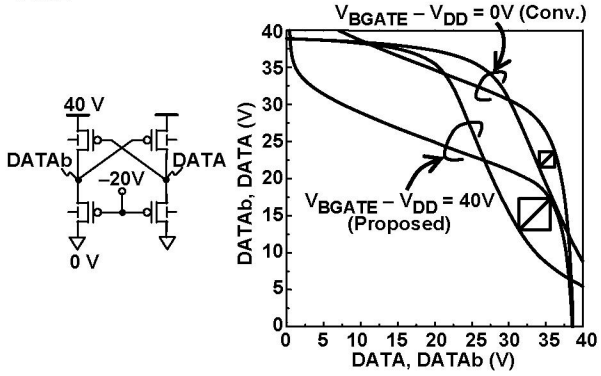


Fig. 8 Measured butterfly curves of SRAM with varied V_{BGATE}.

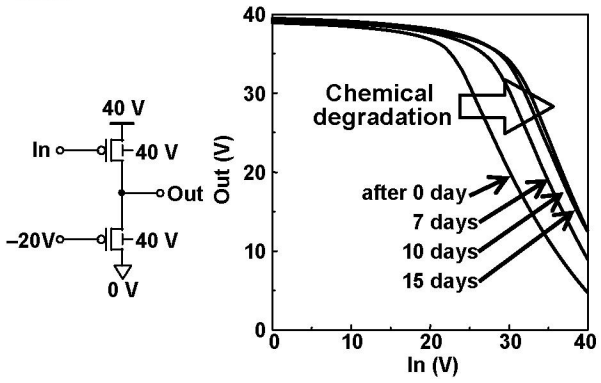


Fig. 9 Measured aging characteristics of the inverter in the SRAM.

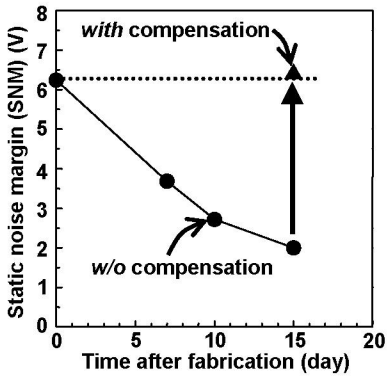


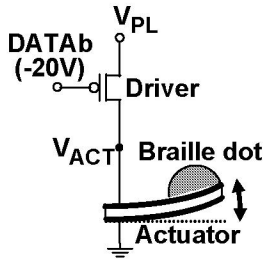
Fig. 10 Aging characteristics of the static noise margin and compensation for the aging.

SNM can be achieved. Because the chemical degradation is inherent in OFETs, the proposed compensation technology is essential to OFET applications.

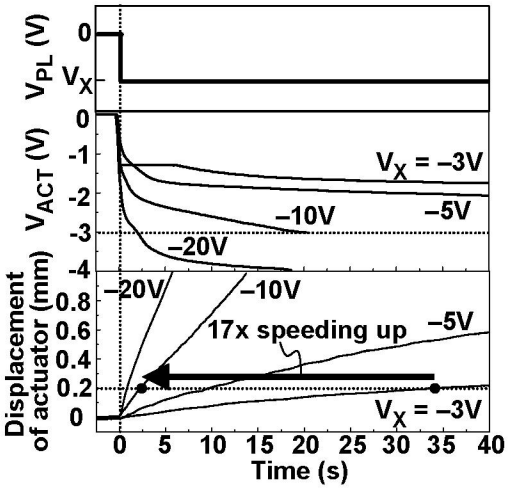
C. Overdrive Techniques for Driver Transistors

Our design target for the transition time of the actuator is within 2 s. The actuator has a large capacitance (100 μF). The breakdown voltage of the actuator is 3 V. Figure 11 shows the measured waveforms of the actuator voltage (V_{ACT}) and the actuator displacement. The step voltage height (V_X) of V_{PL} is varied. The required displacement by Braille users is 0.2 mm. When V_{PL} is equal to the breakdown voltage of -3 V, the transition time is 34 s, which exceeds our design target. In order to reduce the transition time, V_{PH} and V_{PL} overdrive techniques are proposed. By increasing V_X from -3 V to -10 V, the transition time is reduced from 34 s to 2.0 s, which satisfies our design target. In order to avoid the breakdown of the actuator, the overdrive period is determined by the time when V_{ACT} is within ±3V.

Finally, an operation of the Braille sheet display is demonstrated. Figure 12 shows the measured waveforms of the driver and the actuator for a Braille dot. Movement of the Braille dot, both up and down, has been successfully demonstrated. By using overdrive techniques in V_{PH} and V_{PL}, a 1.6-s actuator transition time is achieved.



(a)



(b)

Fig. 11 (a) Measured driver and actuator circuits. (b) Accelerated actuator by overdrive techniques.

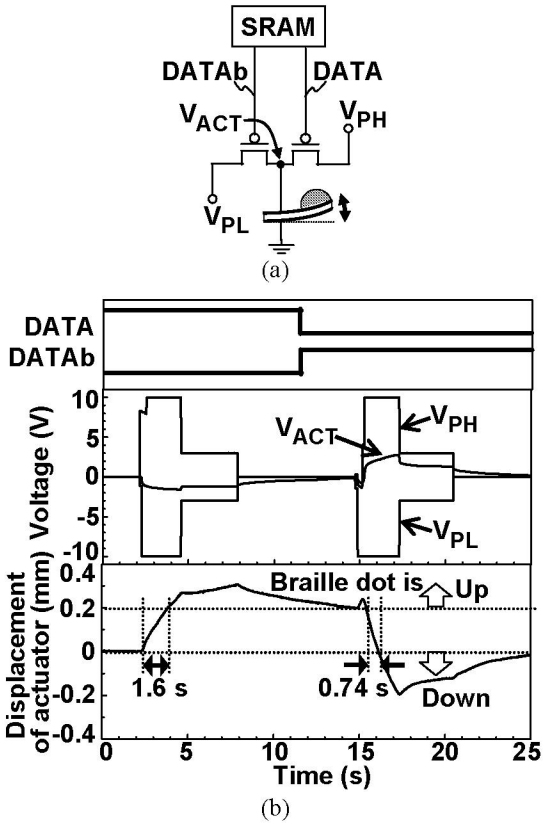


Fig. 12 (a) Measured Braille sheet display circuits. (b) Braille sheet display operation.

Performance Summary

Figure 13 summarizes the time to change 144 Braille dots and the speeding up by the developed circuit technologies. At an initial design without the SRAM, it takes 4896 s, because the 144 actuators are sequentially driven. When the SRAM is added, it takes 40 s, because all actuators are a simultaneously driven after the data are written to SRAM. At a final design, the developed pipelining for SRAM write-operation and overdrive technology for the driver increased the speed of the Braille sheet display 1580 times, and achieved the practical 3.1-s operation.

Figure 14 shows the power consumption for the whole Braille sheet display at 0.1-Hz operation. The dominant component is the leakage power of the actuators (21.6 mW= 50 µA x 3 V x 144). In contrast, the leakage power of piezo actuators used in a commercially available Braille display [6] is 230.4 mW (= 8 µA x 200 V x 144) which is 10.7 times larger than that of our actuators.

Conclusions

OFETs were integrated with actuators, and a Braille sheet display was demonstrated. An SRAM made with OFETs is demonstrated for the first time. Pipelining the write-operation reduced the SRAM write-time by 74%. Threshold voltage control technology using a back gate increased the SNM and compensated for the chemical degradation of the OFETs after 15 days. The

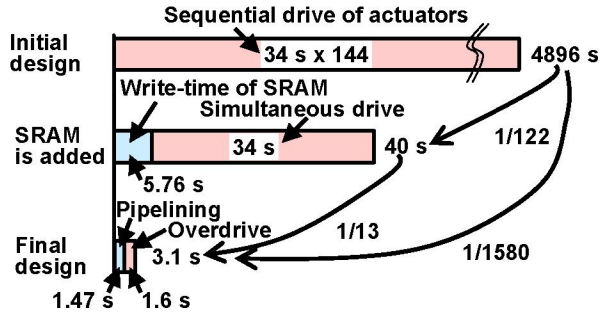


Fig. 13 Summary of speeding up Braille sheet display.

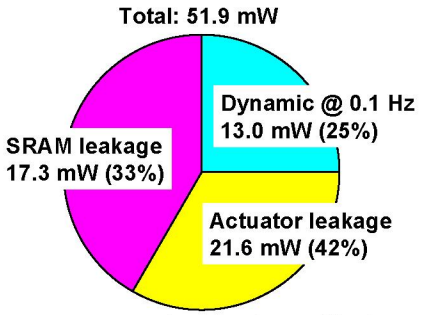


Fig. 14 Power consumption for the Braille sheet display at 0.1-Hz operation.

overdrive techniques for the driver OFETs reduced the transition time of the actuator from 34 s to 2 s.

These developed circuit technologies will be essential for the future large area electronics made with OFETs.

Acknowledgement

The authors acknowledge Prof. M. Doi, University of Tokyo, and Dr. K. Asaka, AIST, for the sheet-type soft actuator made of perfluorinated polymer electrolyte. This work is partially supported by JST, IT program, MEXT, and NEDO.

References

[1] T. Someya, H. Kawaguchi, and T. Sakurai, "Cut-and-paste organic FET customized ICs for application to artificial skin," ISSCC Dig. of Tech. Papers, pp. 288-289, Feb. 2004.

[2] H. Kawaguchi, S. Iba, Y. Kato, T. Sekitani, T. Someya, and T. Sakurai, "A sheet-type scanner based on a 3D stacked organic-transistor circuit with double word-line and double bit-line structure," ISSCC Dig. of Tech. Papers, pp. 580-581, Feb. 2005.

[3] M. Takamiya, T. Sekitani, Y. Kato, H. Kawaguchi, T. Someya, and T. Sakurai," An Organic FET SRAM for Braille sheet display with back gate to increase static noise margin," ISSCC Dig. of Tech. Papers, pp. 276-277, Feb. 2006.

[4] Y. Kato, S. Iba, T. Sekitani, Y. Noguchi, K. Hizu, X. Wang, K. Takenoshita, Y. Takamatsu, S. Nakano, K. Fukuda, K. Nakamura, T. Yamaue, M. Doi, K. Asaka, H. Kawaguchi, M. Takamiya, T. Sakurai, and T. Someya, "A flexible, lightweight Braille sheet display with plastic actuators driven by an organic field-effect transistor active matrix," IEDM Tech. Dig., pp. 105-108, Dec. 2005.

[5] S. Iba, T. Sekitani, Y. Kato, T. Someya, H. Kawaguchi, M. Takamiya, T. Sakurai, and, S. Takagi, "Control of threshold voltage of organic field-effect transistors with double gate structure," Applied Physics Letters, 87, 023509, July 2005.

[6] Braille cells, http://www.kgs-jpn.co.jp/epiezo.html, KGS Corporation.