A design methodology of chip-to-chip wireless power transmission system

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Abstract— **A design methodology to transmit power using a chip-to-chip wireless interface is proposed. The proposed power transmission system is based on magnetic coupling, and the power transmission of 5mW/mm^2 was verified. The transmission efficiency trade-off with the transmitted power is also discussed.**

I. Introduction

A System-in-a-Package (SiP) is getting a major 3D integration approach in recent years. For data communication among stacked chips in SiP's, wireless data transmission technologies have been investigated for high speed, low power and low cost [1][2]. Power delivery in these systems, however, is not wireless and is based on bonding. Then, it is difficult to get two stacked chips close, since the bonding needs several hundred microns separation between chips. One solution is to skew the stacked chips but this is difficult if the upper chip should be connected in the middle of the lower chip and is covered by the topmost chip.

If the power is supplied wirelessly, the chips can be stacked closely and the wireless data transmission performance will be increased, since the data bandwidth and communication reliability increases as the chip-to-chip distance is decreased in wireless data communication. The cost is also decreased due to the elimination of mechanical bonding. Furthermore, chip detachability can also be achieved by combining the wireless data and power transmission. This opens up a totally new system customization scheme after the fabrication as we sometimes change a daughter board for system upgrade.

Fig.1 illustrates a proposed wireless power delivery scheme based on inductive coupling between the lowest chip and upper chips. The shortest inductor-to-inductor distance depends on the thinning of the chip thickness, which is as small as 20 microns. If a face-to-face configuration is possible, the distance is further reduced, which is used in the measurement setup in this paper.

Fig.2 shows the concept of system customization after the fabrication of an SiP to reduce mask set cost and to increase post-fabrication system modification freedom. Chips like accelerators, special engines, analogs, memories are attached wirelessly on top of the lower base chip. The lower chip embedded in the package has a data transceiver and a "power transmitter". The upper chip attached to the package has a data transceiver and a "power receiver". This system may give users the ability to upgrade the SiP's like a daughterboard upgrade nowadays. The risk of ESD problem is mitigated because this system eliminates the naked interconnections and metal pads with coils for wireless transmission being covered by passivation layer.

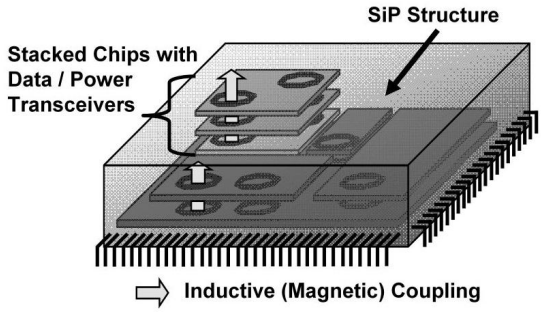


Fig. 1. Concept of chip-to-chip wireless power transmission assisting wireless interchip communication.

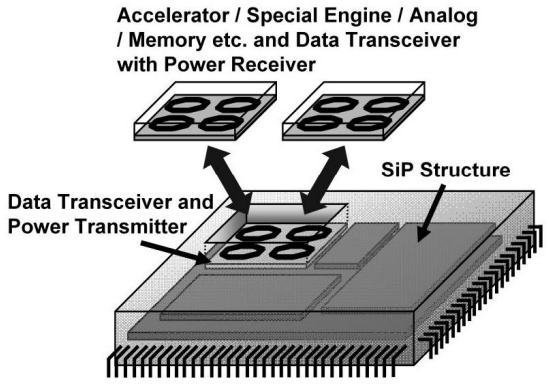


Fig. 2. Concept of system modification after fabrication of SiP's/SoC's.

II. Test Circuit

A. Circuit Topology

Fig.3 shows the circuit diagram of the proposed system. The lower chip includes a transmitter circuit and an on-chip planar inductor L_1 for magnetic field generation. The transmitter circuit generates an RF signal from the DC supply voltage V_{DD} and activates L_1. The power is transmitted by magnetic fields rather than radio waves. Fig.4 describes a diagram of the adopted transmitter, where the oscillation frequency f of the

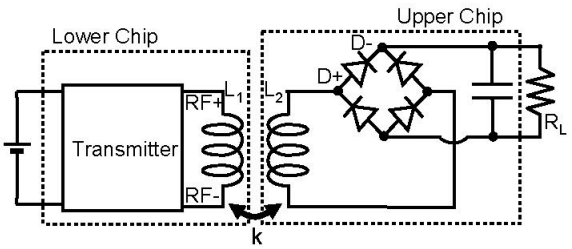


Fig. 3. Circuit diagram of proposed system.

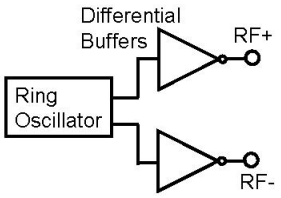


Fig. 4. Circuit diagram of transmitter.

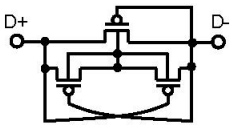


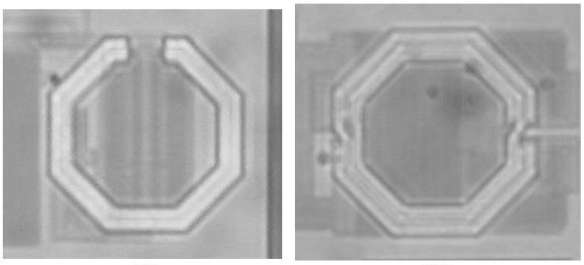
Fig. 5. Circuit diagram of PMOS-based diode.

ring oscillator is designed to be variable for the experiments. The upper chip includes an on-chip planar inductor L_2, a full-wave rectifier circuit using MOSFET-based diodes and a smoothing capacitor. Fig.5 shows the circuit diagram of the diode circuit whose two PMOS transistors reduce the undesirable body effect of the main PMOS transistor [3]. k indicates the coupling factor of the inductors.

B. Simulation and Measurement Results

The system shown in Fig.3 was designed in 0.35-μm CMOS and fabricated. Generally, on-chip planar inductors have considerable parasitic capacitive and resistive elements so that the Q factor is not high. Values of series resistance and parasitic capacitances of the inductor are calculated by approximation formulas and k is derived by momentum electromagnetic field simulator. The parasitic resistances of buffers, diodes and interconnections were be estimated carefully and minimized in design and layout process. The outside diameter of the inductor is set to 700x700μm and k is calculated to be 0.75. RF voltage generated between two terminals of L_2 is set to be twice the nominal V_{DD} when $R_L=\infty$. This RF voltage is better to be higher to reduce the diode voltage loss but it can not surpass twice the tolerant voltage of the PMOS shown in Fig.5. Fig.6 shows microphotographs of the fabricated power transmitter and receiver chips. Fig.7 and 8 show the measurement setup. The lower (upper) chip is mounted on the lower (upper) board and the two chips gets closer together face-to-face.

Fig.9 shows the simulated and measured transmitted power dependence on output DC voltage. HSPICE is used for the simulation. In this implementation, L_1=1.0nH, L_2=9.3nH and



(a) (b)

Fig. 6. Chip microphotograph of (a) transmitter and (b) receiver.

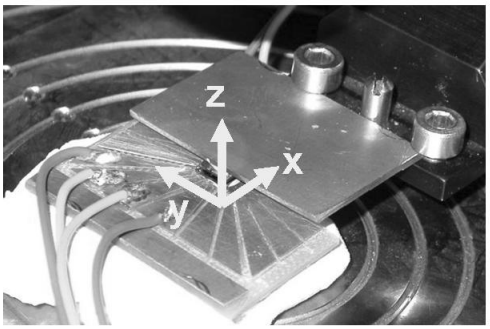


Fig. 7. Whole image of measurement setup.

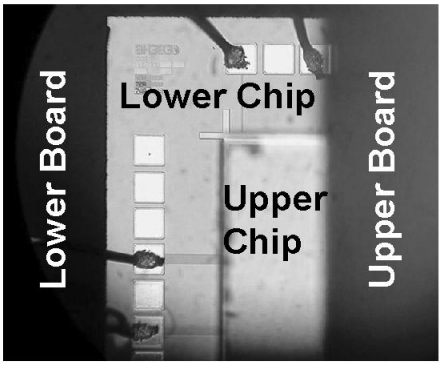


Fig. 8. Closeup view of measurement setup.

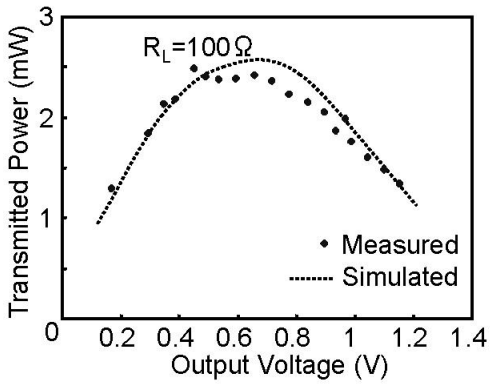


Fig. 9. Transmitted power dependence on output voltage.

the oscillation frequency is set to f = 330MHz for this graph. Output voltage is varied by changing DC output load R_L. The peak transmitted power 2.5mW which equals to 5mW/mm^2 is

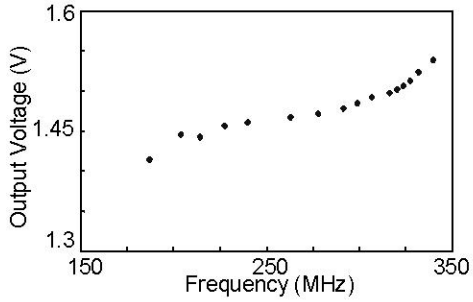


Fig. 10. Output voltage dependence on oscillation frequency *f*.

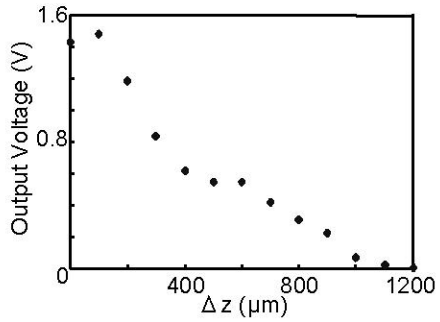


Fig. 11. Output voltage dependence on Δz.

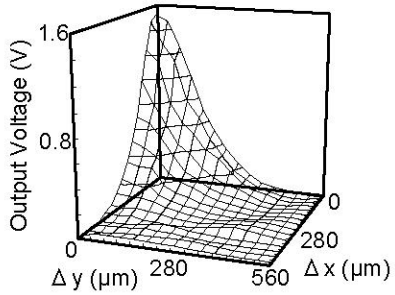


Fig. 12. Output voltage dependence on Δx and Δy.

observed when R_L is 100Ω, which is the equivalent source resistance of the wireless power source. The simulated results coincide well with the measured results. Thus the modeling accuracy is considered to be sufficiently high. Figs. 10, 11 and 12 show the measured output voltage dependence on frequency, Δz (distance between chips) and Δx (misplacement in x direction) and Δy (misplacement in y direction) when the load is open which equals to $R_L=\infty$.

III. CIRCUIT OPTIMIZATION

A. Circuit Model

Although the feasibility of the wireless power delivery system is demonstrated in the previous sections, it is preferable to increase the transmittable power and to maximize the power efficiency to further increase the variety of applications. In this section, the methodology for further increasing the transmitted power and maximizing the power efficiency are described using simple circuit model. Improvement can be achieved by adding resonance capacitors C_1 and C_2 as shown in Fig.13. R_S

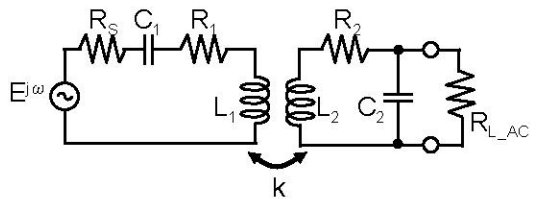


Fig. 13. Simplified circuit model.

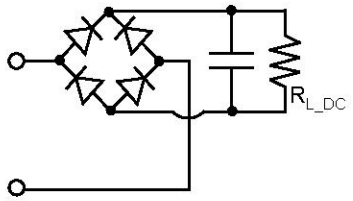


Fig. 14. Equivalent circuit of R_{L_AC}.

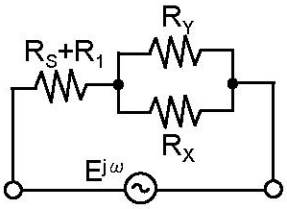


Fig. 15. Circuit model under resonance condition.

represents parasitic resistances of transmitter interconnections and driving transistors which equals to the internal impedance of the transmitter. R_1 and R_2 indicate series resistances of L_1 and L_2 respectively. Capacitances C_1 and C_2 resonate with L_1 serially and with L_2 in parallel respectively. R_{L_AC} relates to the equivalent total impedance of the rectifier, the smoothing capacitor and the DC load resistance R_{L_DC} as shown in Fig.14. R_{L_AC} was shown to be approximated as follows when the rectifier is ideal and the smoothing capacitor is large enough [4].

$$R_{L\_AC} \approx \frac{R_{L\_DC}}{2}. \quad (1)$$

Here, we assume the transmitted power is high (if not maximized) when transmitter circuit is in resonance. That is, C_1 is expressed as follows. Although this condition does not give the optimum condition, the resultant transmitted power is at least achievable.

$$C_1 = \frac{1}{4\pi^2 f^2 L_1}. \quad (2)$$

On the other hand, C_2 resonates under the following condition and the circuit model can be converted to a simple resistance model as shown in Fig.15.

$$4\pi^2 f^2 R_{L\_AC}^2 L_2 C_2^2 - R_{L\_AC}^2 C_2 + L_2 = 0. \quad (3)$$

R_X and R_Y are the transformed impedances of R_2 and R_L, and are described as follows.

$$R_X = 4\pi^2 f^2 k^2 L_1 L_2 \frac{1}{R_2}. \quad (4)$$

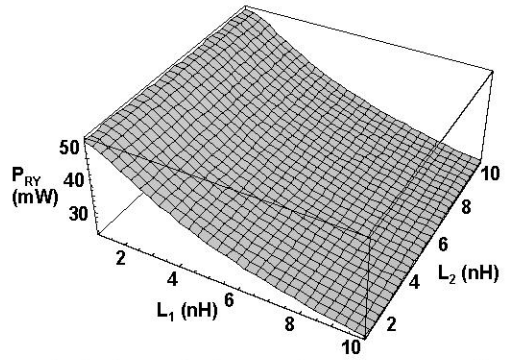


Fig. 16. Calculated transmitted power dependence on L_1 and L_2 when power efficiency is maximized.

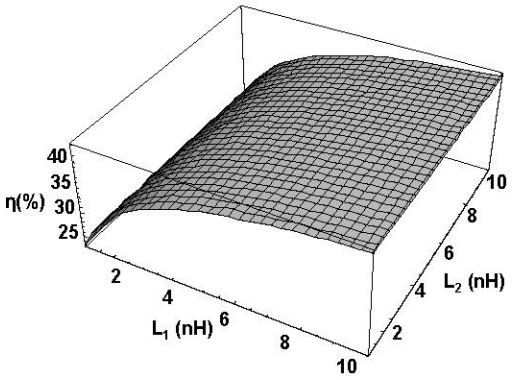


Fig. 17. Calculated power efficiency dependence on L_1 and L_2.

$$R_Y = 4\pi^2 f^2 k^2 L_1 L_2 \frac{\left(1+4\pi^2 f^2 C_2^2 R_{L\_AC}^2\right)}{R_{L\_AC}}. \qquad (5)$$

In this system, high power efficiency is as important as the transmitted power to increase the variety of applications. The power transmission efficiency for R_Y is maximized under the following condition.

$$R_Y = R_X \sqrt{\frac{R_S + R_1}{R_S + R_1 + R_X}}. \qquad (6)$$

In case of on-chip planar inductors, the relationship between R_N and L_N is approximated as follows with ζ being a technology parameter because both R_N and L_N are roughly proportional to the square of turns.

$$\zeta \approx \frac{L_N}{R_N}. \qquad (7)$$

The optimum values of C_2 and R_{L_AC} are calculated as functions of k, f, ζ, R_S, R_1, R_2 by using formulas (3) and (6).

$$C_2 = \frac{\xi\left(R_S + R_1\right)}{R_2\left[R_S + R_1 + 4\pi^2 f^2 \xi^2 \left(R_S + R_1 + k^2 R_1\right)\right]}. \qquad (8)$$

$$R_{L\_AC} = \frac{\xi}{C_2}\sqrt{\frac{R_S + R_1}{R_S + R_1 + 4\pi^2 f^2 \xi^2 k^2 R_1}}. \qquad (9)$$

Figs.16 and 17 show the calculated transmitted power and power efficiency η when f=330MHz, k=0.75 and ζ=1.7×10^{-9} which are the same conditions with the real circuit presented in section II, and R_S=2. In this design region, the power efficiency improves as the value of L_1 increases although the transmitted power degrades. On the other hand, both the power efficiency and the transmitted power are independent of the value of L_2. In a real design, both the transmitted power and the power efficiency are lower than the calculation results due to other independent power losses including switching loss and rectifying loss however, this optimization is valuable for the fundamental design.

B. Example of Improved Design

To show further capability of the proposed system, an example of improved design using the optimization theory is described in this section. To gain higher transmitted power and power efficiency, Class-E amplifier and improved rectifier[5] are also valuable. Assuming that those techniques are utilized in 90nm CMOS, other parameters are chosen as f=900MHz, k=0.75, ζ=2.6×10^{-9}, L_1=3.9nH, L_2=6.8nH and C_2=3.5pF with inductor outer diameter of 500μm. As a result, the transmitted power of 306mW/mm^2 and the power efficiency of 23.4% for V_{DD}=2.5V are simulated by using HSPICE with all the parasitic elements.

IV. CONCLUSIONS

In summary, a chip-to-chip 5mW/mm^2 wireless power transmission system was proposed and demonstrated by 0.35-μm CMOS technology. Maximization of the power efficiency and an example of improved design are also discussed.

ACKNOWLEDGMENT

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Rohm Corporation, Toppan Printing Corporation and Cadence Design Systems, Inc. This research was partially supported by Japan Society for the Promotion of Science (JSPS), Grant-in-Aid for Scientific Research (KAKENHI) 16760271.

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