Design Impact of Positive Temperature Dependence on Drain Current in Sub-1-V CMOS VLSIs

Kouichi Kanda, Kouichi Nose, *Student Member, IEEE*, Hiroshi Kawaguchi, and Takayasu Sakurai, *Member, IEEE*

***Abstract*—In sub-1-V CMOS designs, especially around 0.5-V CMOS designs, on-state drain current of MOSFETs shows positive temperature dependence, being different from the negative temperature dependence in the conventional voltage designs. Combined with low threshold voltage less than 0.2 V, the possibility of temperature instability increases. This paper describes possible temperature instabilities in the low-voltage regime by using circuit simulation environments incorporating temperature change in time and experiments using MOSFETs and the 32-bit adder circuit in quarter-micrometer CMOS technology with a low threshold voltage of 0.25 V.**

***Index Terms*—Leakage power, low power, low threshold voltage, package, temperature dependence, thermal breakdown.**

I. Introduction

RECENTLY, low-power and high-performance VLSI design is attracting much attention due to the emerging needs for portable multimedia equipments and due to the stringent heat problems for high-end processors. Since the dynamic power component of CMOS digital circuits is proportional to the square of the supply voltage, $V_{\rm DD}$, the scaling of $V_{\rm DD}$ is very effective to reduce the power dissipation. The low-$V_{\rm DD}$ CMOS, however, suffers from large delay [1], and low threshold voltage less than 0.2 V is used [2] to mitigate the delay degradation. The delay is expressed as

$$\text{Delay} \propto \frac{CV_{\rm DD}}{I_{\rm D}} \propto \frac{CV_{\rm DD}}{(V_{\rm DD}-V_{\rm TH})^{\alpha}} \tag{1}$$

where

- $I_{\rm D}$ drain current;
- $V_{\rm TH}$ threshold voltage;
- α velocity saturation index, whose typical value is around 1.3 for short-channel MOSFETs [3].

From the discussions above, the low-power design in the future tends to use low $V_{\rm DD}$ and low $V_{\rm TH}$.

It has been reported in [4] that the temperature dependence is a function of $V_{\rm DD}$, and at around 1.2 V, the temperature dependence is minimized (measurement results shown in Fig. 1). Historically speaking, this zero-temperature coefficient (ZTC) point has been recognized as an important voltage by analog designers for a long time. It is predicted, however, in the SIA roadmap [5] that in the year 2010, the mainstream supply voltage will be around 0.6 V, and the circuit implementation with 0.5-V supply voltage is getting focus recently [6]. The voltage is much smaller than the ZTC point and the positive temperature dependence of drain current is observed in the region. This reverse temperature dependence has been pointed out in [7] as a favorable effect in the low-$V_{\rm DD}$ region. The minimum value of $V_{\rm DD}$ and $V_{\rm TH}$ used in [7], however, still remains rather high, such as 1.2 V for $V_{\rm DD}$ and 0.7 V for $V_{\rm TH}$. This paper shows that in practical low-$V_{\rm DD}$ designs which utilize lower $V_{\rm TH}$ such as 0.2 V, temperature instability may occur.

Thermal instability in the low-$V_{\rm TH}$ regime has not been investigated. This paper reports the design implications of the temperature dependence of circuit performance in low-$V_{\rm TH}$ region using temperature-varying circuit simulation environments and through measurements for the first time.

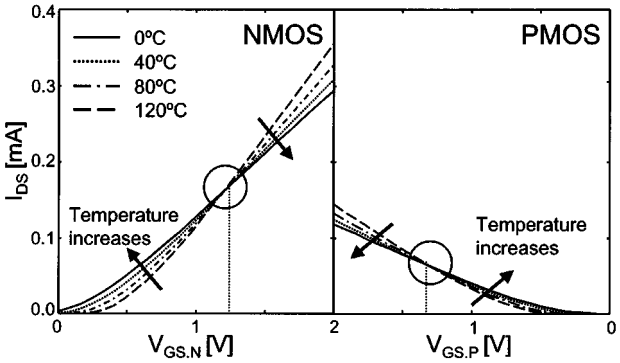

Fig. 1. Measured temperature dependence for nMOS and pMOS transistors (temperature range from 0 to 120 °C).

II. Temperature Dependence on Drain Current

The MOSFET drain current $I_{\rm D}$ is expressed as

$$I_{\rm D} \propto \mu(T)(V_{\rm DD}-V_{\rm TH}(T))^{\alpha}. \tag{2}$$

The threshold voltage $V_{\rm TH}(T)$ and the mobility $\mu(T)$ have temperature dependence [4] as follows.

$$V_{\rm TH}(T) = V_{\rm TH}(T_0) - \kappa(T-T_0) \tag{3}$$

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m} \tag{4}$$

where

- T temperature;
- T_0 room temperature ($T_0 = 300$ K);
- κ threshold voltage temperature coefficient whose typical value is 2.5 mV/K;
- m mobility temperature exponent whose typical value is 1.5.

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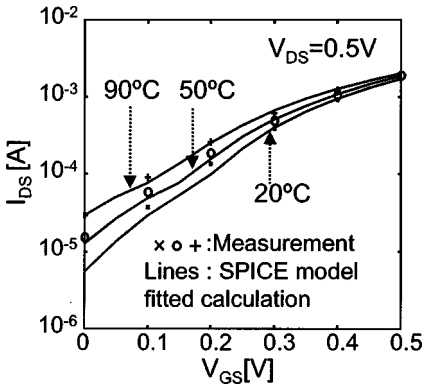

Fig. 2. Measured and simulated temperature dependence of drain current for nMOS.

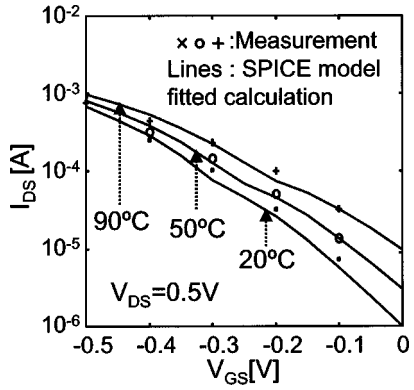

Fig. 3. Measured and simulated temperature dependence of drain current for pMOS.

It is seen from [3] and [4] that the mobility and $V_{\rm TH}$ shows negative dependence on temperature. When temperature increases by 100 K, the threshold voltage decreases typically by 0.25 V and the mobility decreases about 35%. If $V_{\rm DD}$ and $V_{\rm TH}(T_0)$ are relatively large, such as 2.5 and 0.7 V, respectively, as in the conventional designs, the increase of the drain current by the $V_{\rm TH}$ decrease of 0.25 V is only about 10%. This does not surmount the current decrease by the mobility degradation. On the other hand, if $V_{\rm DD}$ is below 1 V, the current increase by the $V_{\rm TH}$ decrease is 55% that surmounts the mobility degradation. This leads to the overall positive temperature dependence of on-state current.

The measured $I_{\rm DS}$–$V_{\rm GS}$ characteristics for 0.35-μm nMOS and pMOS are shown in Figs. 2 and 3. These figures clearly show positive temperature dependence of the drain current on temperature in sub-1-V region. The figures also show a fitted SPICE model calculation that coincides well with the measurement results. This suggests that the built-in temperature dependence in SPICE can be used to simulate circuits with temperature effects taken into account.

The positive temperature dependence inevitably impacts on gate delay. Fig. 4 shows simulation results for the temperature dependence of the gate delay of a two-input NAND gate with fanout of two for the high-$V_{\rm DD}$, high-$V_{\rm TH}$ case and low-$V_{\rm DD}$, low-$V_{\rm TH}$. The graph indicates that the operation speed of circuits gets faster as temperature increases in the low-$V_{\rm DD}$

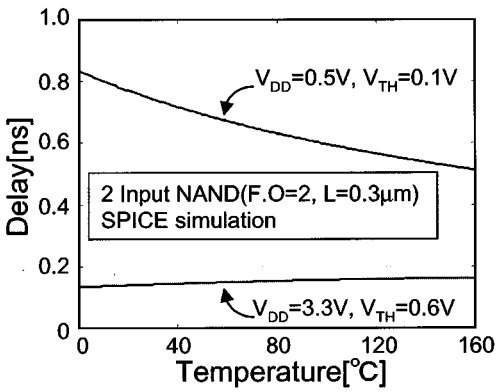

Fig. 4. Simulated temperature dependence of gate delay for high-$V_{\rm DD}$ and high-$V_{\rm TH}$ case and low-$V_{\rm DD}$ and low-$V_{\rm TH}$ case.

designs, being different from the conventional high-$V_{\rm DD}$ case, where the worst delay occurs at the highest temperature.

III. Temperature-Varying Circuit Simulation

In order to set up circuit simulation environments with temperature-varying effects taken into consideration, an expression for CMOS power consumption and modeling of a chip and a package as a thermal system are necessary. Equation (5) shows the total power consumption of CMOS circuits, which consists of two components, $P_{\rm AC}$ and $P_{\rm LEAK}$, which represent a dynamic power component and a leakage power component, respectively. A short-circuit power component has been neglected, since it has been shown that the component is much smaller compared with the dynamic power component, even in the low-$V_{\rm DD}$, low-$V_{\rm TH}$ region [9].

$$P_{\rm TOTAL} = P_{\rm AC} + P_{\rm LEAK} \tag{5}$$

Each component can be expressed by using the following expressions:

$$P_{\rm AC} = a \cdot C \cdot f \cdot V_{\rm DD}^2 \tag{6}$$

$$P_{\rm LEAK} = I_{\rm LEAK} \cdot V_{\rm DD} \tag{7}$$

where a, C, f, and $I_{\rm LEAK}$ correspond to switching activity, total capacitance, clock frequency, and leakage current, respectively. In order to introduce temperature effects in these expressions, two cases have to be separated. The first case is a synchronous circuit case, where a clock frequency f is independent from temperature, and the other is an asynchronous case, where f is a function of temperature. In the former case, f is fixed at a certain value, and in the latter case, f is inversely proportional to gate delay. For both cases, the temperature dependence of $I_{\rm LEAK}$ is shown in Fig. 5. For the high-$V_{\rm DD}$, high-$V_{\rm TH}$ case, the line is almost straight since subthreshold leakage current is exponentially dependent on temperature. On the other hand, the line is not straight for the low-$V_{\rm DD}$, low-$V_{\rm TH}$ case, because the leakage at high temperature is no longer subthreshold leakage but on-state drain current, since the threshold voltage decreases by 0.25 V as temperature goes up by 100 K, and therefore the MOSFET is in a depletion mode at the high temperature.

Fig. 6 shows an equivalent electrical circuit for a thermal system of a chip and a package used in this work. In the model,

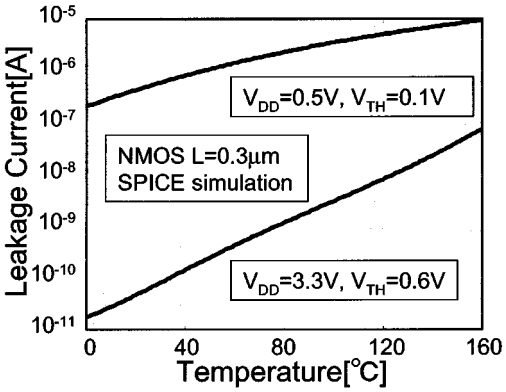

Fig. 5. Simulated temperature dependence of leakage current for high-$V_{\rm DD}$ and high-$V_{\rm TH}$ case and low-$V_{\rm DD}$ and low-$V_{\rm TH}$ case.

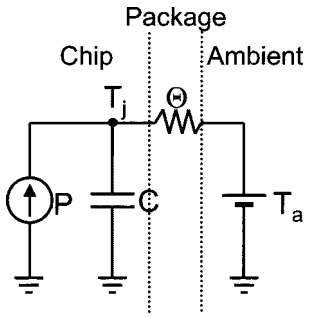

Fig. 6. Equivalent electrical circuit of chip and package system.

temperature corresponds to node voltage and heat corresponds to current. In the figure, $T_{\rm j}$ signifies a junction temperature, $T_{\rm a}$ signifies an ambient temperature, θ is the heat resistance of a package, and c is the heat capacity of a system. The power consumption of the chip corresponds to the current source. This model is a simple first-order approximation in which the whole chip has a single temperature. Actually, each circuit block on a chip has different activity, and therefore has different temperature. However, it is a well-known fact that when a latchup phenomenon occurs in some part of a chip, the local increase of temperature rapidly spreads over the whole chip and causes thermal breakdown. Though all the parameters in the model are treated in average, this simple model in Fig. 6 is still valid for the latter discussion on the possibility of thermal breakdown due to the positive feedback mechanism. For a small time interval of Δt from time t during which the power consumption is constant, the system has an exponential solution as in (8), which changes from $T_{\rm j,initial}$ toward $T_{\rm a}+\theta P$ with a time constant of $c\theta$.

$$T_{\rm j}(t+\Delta t) = (T_{\rm a}+\theta P_{\rm av}) + (T(t)-T_{\rm a}-\theta P_{\rm av}) \times \exp\left(-\frac{\Delta t}{c\theta}\right). \quad (8)$$

In reality, the power consumption changes in time and this solution can be applied only for a short time interval Δt. Thus, the asymptotic temperature in (8), $T_{\rm a}+\theta P$, does not mean that the system asymptotes to this temperature. In order to simulate the response of the system, a simulation environment is set up, the flow chart of which is shown in Fig. 7. First, SPICE simulation is carried out and then the average power consumption of

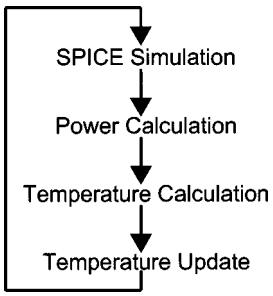

Fig. 7. Flowchart for temperature-varying circuit simulation.

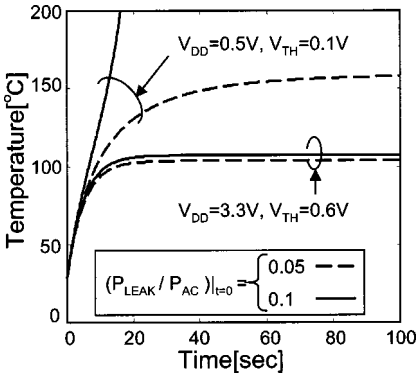

Fig. 8. Transient response of chip temperature for synchronous circuits using two different initial conditions.

the circuit, $P_{\rm AV}$, over a short time step, Δt, is calculated using the average current over Δt. The time step Δt should be small enough to precisely track the thermal behavior of the system. Dynamically changing the value of Δt gives more efficient and precise simulation, but the time constant of the thermal system depicted in Fig. 6 is far larger compared with the time step used in the transient analysis of circuits. Therefore, Δt is treated as constant in this simulation. The temperature change during Δt is calculated by using (8). Now that the new temperature is calculated, using the above expression, the temperature is updated by using the TEMP statement in SPICE and the simulation is continued using the new temperature. This loop is iterated. All procedures are automated using Perl scripts [8] in UNIX environments.

IV. Simulation Results

Transient responses of a synchronous circuit for two different initial $P_{\rm LEAK}/P_{\rm AC}$ are shown in Fig. 8 (chip temperature) and Fig. 9 (total power), using the same value for c and θ. Package parameters c and θ are chosen so that the chip temperature settles around 100 °C in high-$V_{\rm DD}$, high-$V_{\rm TH}$ design. The simulation time step is 50 ms. The high-$V_{\rm DD}$, high-$V_{\rm TH}$ case and the low-$V_{\rm DD}$, low-$V_{\rm TH}$ case are compared in the figures. Although total power consumption at room temperature is equal for both cases, the final temperature becomes over 150 °C for the low-$V_{\rm DD}$, low-$V_{\rm TH}$ design, while it does not change much from 100 °C for the high-$V_{\rm DD}$, high-$V_{\rm TH}$ design even when the same package is used. 150 °C is not desirable in view of both proper operation of circuits and long-term reliability of devices. Fig. 8 also indicates that there is a possibility of thermal runaway in some cases.

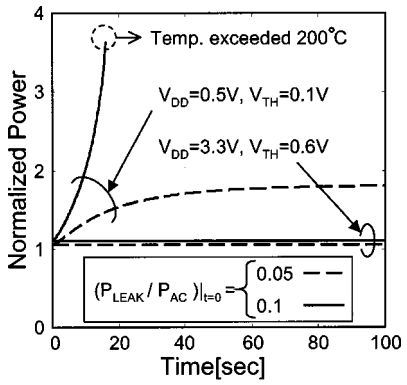

Fig. 9. Transient response of total power consumption for synchronous circuits (all parameters are same as those in Fig. 8).

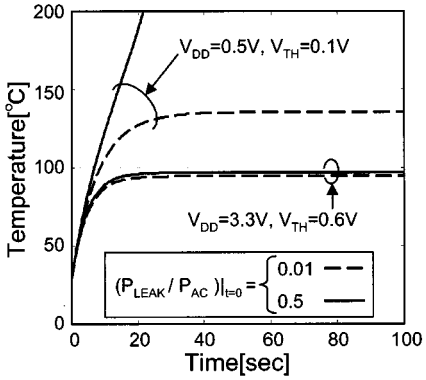

Fig. 10. Transient response of chip temperature for asynchronous circuits for two different initial conditions.

Transient responses for an asynchronous circuit are shown in Fig. 10 (chip temperature) and Fig. 11 (gate delay). All the parameters are the same as those in the previous simulations for the synchronous case. In the asynchronous circuit, when the temperature increases, the drain current increases and, as a result, the frequency of the circuit increases. Then, the dynamic power component $af\mathrm{CV}^2$ increases and the temperature increases further. This is a positive feedback loop. This temperature dependence of P_{AC}, in addition with the increase of P_{LEAK}, results in the easier thermal runaway than the synchronous circuit case.

The positive feedback loop in the low-V_{DD}, low-V_{TH} region is depicted in Fig. 12 for both of the synchronous and asynchronous cases. Actually, this positive feedback also exists even in circuits operated in the high-V_{DD}, high-V_{TH} region, since the clock frequencies for synchronous circuits are usually maintained at a certain value by using phase-locked loops (PLLs) against a wide range of temperature variations, and therefore the P_{AC} does not decrease, though the gate delay slightly increases, as shown in Fig. 4. In the high-V_{TH} region, however, the leakage component of the power consumption is much lower than the dynamic component, and hence the P_{DC} does not become a dominant factor in the heat generation. This is the reason why the thermal runaway is not observed frequently in the conventional designs. The resiliency for the temperature instability is tabulated for various circuit blocks in Table I. In this table, memory and analog circuits are added. Except for synchronous circuits, all the others can become unstable in the low-V_{DD} region because they are essentially

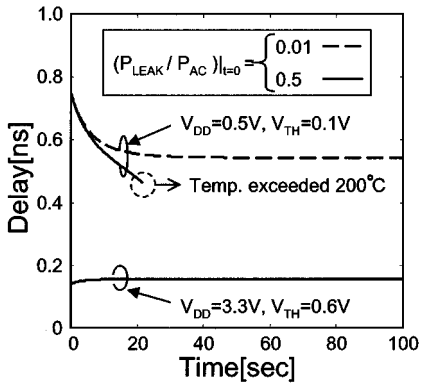

Fig. 11. Transient response of gate delay for asynchronous circuits ($P_{\mathrm{LEAK}}/P_{\mathrm{AC}}$ is 0.01 at $t = 0$).

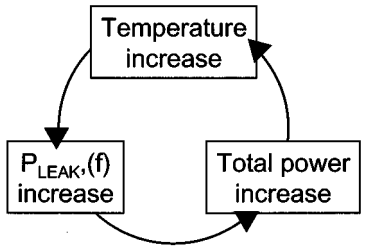

Fig. 12. Positive feedback thermal system.

TABLE I
RESILIENCY FOR TEMPERATURE INSTABILITY FOR VARIOUS CIRCUIT BLOCKS

	Synch. Digital	Asynch. Digital	Memory	Analog
High-V_{DD}, High-V_{TH}	H	H	H	H
Low-V_{DD}, High-V_{TH}	M	L	L	L
Low-V_{DD}, Low-V_{TH}	L	L	L	L

H: High, M: Medium, L: Low

asynchronous operation, and in addition, they usually have dc current paths such as current sources, sinks, and mirrors in amplifiers. Therefore, their resiliency is written as "Low." A memory circuit with large capacity and low threshold voltage is the most dangerous case. As for synchronous circuits in the low-V_{DD}, high-V_{TH} region, they have positive temperature dependence that can cause a thermal instability problem, while leakage current can be well suppressed. Its stability depends on operation frequency. Therefore, its resiliency is written as "Medium." Synchronous circuits in the low-V_{DD}, low-V_{TH} region have a large possibility of thermal instability as mentioned above, and therefore denoted as "Low."

V. MEASUREMENT RESULTS AND DISCUSSIONS

Fig. 13 shows a test chip fabricated with a quarter-micrometer CMOS technology with a low threshold voltage of 0.25 V. Fig. 14 shows the measured temperature dependence of a 32-bit adder. It can be seen from the figure that the temperature dependence of the circuit speed is not only opposite in the low-V_{DD} region, but also is greater compared with the relatively high-V_{DD} design.

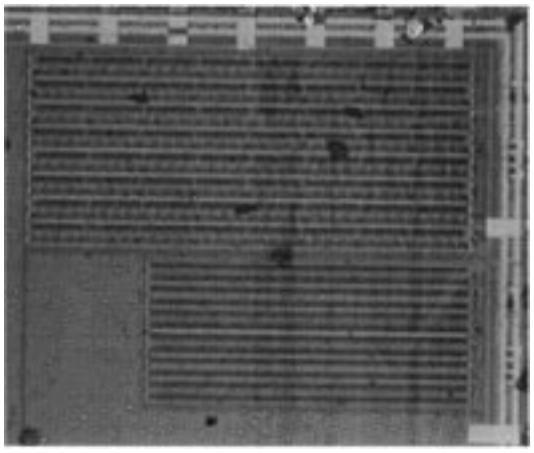

Fig. 13. Microphotograph of test chip.

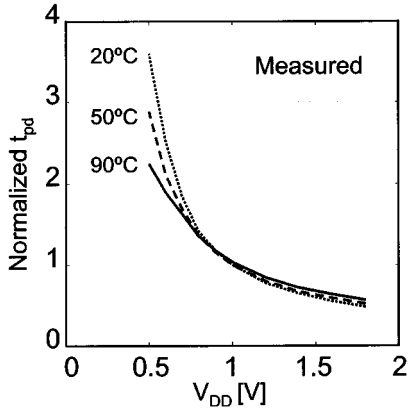

Fig. 14. Measured temperature dependence circuit delay in a 32-bit adder.

Let us consider the minimum threshold voltage at room temperature, $V_{\mathrm{TH0,min}}$, that assures the junction temperature to be less than $T_{\mathrm{j,max}}$. The following equations determine the system.

$$T_{\mathrm{j}} = T_{\mathrm{a}} + P\theta \tag{9}$$

$$\frac{P}{N} = afCV_{\mathrm{DD}}^2 + V_{\mathrm{DD}} I_{\mathrm{C}} \exp\left(-\frac{qV_{\mathrm{TH}}}{nkT_{\mathrm{j}}}\right) \quad (\text{Positive } V_{\mathrm{TH}}) \tag{10}$$

$$= afCV_{\mathrm{DD}}^2 + V_{\mathrm{DD}}\beta|-V_{\mathrm{TH}}|^{\alpha} \quad (\text{Negative } V_{\mathrm{TH}}) \tag{11}$$

$$V_{\mathrm{TH}} = V_{\mathrm{TH0}} - \kappa(T - T_0) \tag{12}$$

where I_{c}, q/nk, and β are constants and N is the number of gates on a chip. When the leakage power is determined by the subthreshold leakage, that is, when V_{TH} is positive, (10) holds [11], but when V_{TH} becomes negative, the leakage power is determined by the drain current of a depletion mode MOSFET and (11) holds. In 0.5-V V_{DD} designs, a very low threshold voltage such as 0.2 V is used, and in this case, (11) is applicable at high temperature. In this case, $V_{\mathrm{TH0,min}}$ can be solved from (9), (11), (12), as follows:

$$V_{\mathrm{TH0,min}} = -\left(\frac{T_{\mathrm{j,max}} - T_{\mathrm{a}}}{N\theta\beta - V_{\mathrm{DD}}}\right)^{1/\alpha} + \kappa(T_{\mathrm{j,max}} - T_0). \tag{13}$$

When typical values are used, $V_{\mathrm{TH0,min}}$ can be approximated as follows:

$$V_{\mathrm{TH0,min}} \approx -\left(\frac{73}{N\theta\beta - V_{\mathrm{DD}}}\right)^{1/\alpha} + 0.2. \tag{14}$$

It can be seen from the expression that the minimum threshold voltage at room temperature should be more than 0.2 V, which coincides with the theoretical optimum threshold voltage given in [10]. A 0.25-V decrease of the threshold voltage should always be considered in the high temperature range.

Now, let us consider package selection. As Figs. 8–11 show, thermal stability of a system has a close relation with package parameters and the initial condition for $P_{\mathrm{LEAK}}/P_{\mathrm{AC}}$. It is clear from (14) that the package with low heat resistance is desirable to decrease the threshold voltage. In selecting a package, the following equation needs to be satisfied to avoid the thermal runaway, which is derived from (9) and (10).

$$\theta < \frac{T_{\mathrm{j}} - T_{\mathrm{a}}}{P_{\mathrm{AC}} + P_{\mathrm{LEAK}}}. \tag{15}$$

The tolerable thermal resistance of a package becomes lower in the low-V_{TH} region where P_{LEAK} is dominant compared with the conventional high-V_{TH} region, because the second term in the denominator can be neglected.

VI. Conclusion

With sub-1-V supply voltage, the on-state drain current and hence the operating speed of circuits shows positive dependence on temperature. This will change the design validation process for worst-case conditions. In the future when low V_{DD} is used, the worst delay occurs at low temperature, being different from the current situation. This positive temperature dependence has been regarded as an advantageous phenomenon for low-V_{DD} LSIs [7]. In low-V_{DD}, low-V_{TH} designs, however, chip temperature goes up much more than in the high-V_{DD}, high-V_{TH} designs, even if power consumption at room temperature and package are the same. In both of the synchronous and asynchronous designs, thermal runaway is more threatening in the sub-1-V and low-V_{TH} region, and more careful choice is required for a package and a cooling system.

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