Cut-and-Paste Customization of Organic FET Integrated Circuit and Its Application to Electronic Artificial Skin

Hiroshi Kawaguchi, *Member, IEEE*, Takao Someya, *Member, IEEE*, Tsuyoshi Sekitani, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—The concept of cut-and-paste customization is introduced for the first time in designing integrated circuits based on mechanically flexible organic field-effect transistors, and is applied to electronic artificial skin. The electronic artificial skin comprise of three separate integrated circuits that are a pressure-sensor array, row decoders, and column selectors to read out pressure information over a large area. All of three integrated circuits are scalable in size because the pressure-sensor array is a simple repetition of sensor cells and the row and column decoders adopt wired-NAND circuits, which enables the cut-and-paste customization in size. The physical cut-and-paste procedure is employed by cutting a part of the integrated circuits and pasting it to another integrated circuit with a connecting plastic tape. The integrated circuits are designed with a standard SPICE simulator and layout design tool, and the operation is confirmed by measurement.**

***Index Terms*—area sensor, cut-and-paste customization, dynamic boosted-gate E/E, electronic artificial skin, organic transistor.**

I. Introduction

ORGANIC-TRANSISTOR circuits are attracting attention for complementing the high-performance yet expensive silicon VLSIs [1]–[5]. It is believed that fabrication cost of organic field-effect transistors (OFETs) can be low even for large-area electronics by introducing roll-to-roll processing. The OFETs are mechanically flexible, which is also suitable for the large-area electronics. The OFET circuits may not compete with silicon VLSIs when we consider cost per function, but they have a definite advantage over silicon VLSIs when cost per area is considered. The carrier mobility in an OFET is about three orders of magnitude lower than that of silicon and the resultant circuit is slow in speed. Although the major driving applications of the OFETs have been limited to radio-frequency identification (RFID) tags and displays including an organic electroluminescence (EL) display and electronic paper (e-paper), these applications except the e-paper sometimes require the higher speed operation than the OFET has ever achieved. Moreover, a silicon RFID is so small that it cannot be broken even in a sheet of paper. Meanwhile, an organic circuit can bend but can be broken if it is bent sharply. In addition to that, the silicon RFID is potentially so cheap that it could be difficult even for the organic circuit to compete with the silicon counterpart. Thus, in the near future, it is difficult for the organic electronics to compete with the silicon electronics in these applications.

The feature of OFETs that they are slow in speed but low in cost per area makes it suitable for area-sensor applications. In particular, the importance of pressure sensing is increasing in applications such as area sensor networks and robots for the next generation. Recently, we have successfully manufactured a large-area and flexible pressure-sensor linear array [4] and array [5], [6] using OFETs, and successfully taken pressure image with resolution of 10 dpi over 4 cm $\times$ 4 cm [6]. In this work, customized OFET ICs are manufactured by combining a pressure-sensor array, row decoders, and column selectors to read out information of area pressure from such a large-area and flexible pressure sensors.

A scalable-circuit concept based on cut-and-paste programmability of the organic ICs is proposed and demonstrated by physically cutting a part of the circuits and pasting it to another circuit with a connecting plastic tape. The ICs are designed with a level 1 SPICE MOS model and standard layout design tool, and the operation of the pressure sensor is confirmed by measurement.

II. Organic Field-Effect Transistor

A. Manufacturing Process and Device Structure of Sensor Cell

The manufacturing process of the OFET devices can be seen in [4]–[7] in detail but will be summarized briefly as shown in Fig. 1.

(1) The base film is PEN (polyethylene naphthalate) or PI (polyimide). First, gate electrodes consisting of adhesion 5-nm Cr (chromium) and 100-nm Au (gold) layers are deposited on the base film through a shadow mask by a vacuum evaporator.

(2) Then 900-nm-thick PI is spin-coated with rotation speed of 3000 rpm as a gate insulator layer and cured at 180 °C for 1 hr in a clean oven (class 100) under the nitrogen environment.

Manuscript received April 18, 2004; revised May 31, 2004. This work was supported in part by the Industry Technology Research Grant Program in 2003 by NEDO, Japan, and a Grant-in-Aid for Scientific Research and IT Program, MEXT, Japan.

H. Kawaguchi is with the Institute of Industrial Science, University of Tokyo, Meguro-ku, Tokyo 153-8505 Japan (e-mail: kawapy@iis.u-tokyo.ac.jp).

T. Someya and T. Sekitani are with the School of Engineering, University of Tokyo, Bunkyo-ku, Tokyo 113-8656, Japan (e-mail: someya@ap.t.u-tokyo.ac.jp; sekitani@ap.t.u-tokyo.ac.jp).

T. Sakurai is with the Center for Collaborative Research, University of Tokyo, Megouro-ku, Tokyo 153-8505, Japan (e-mail: tsakurai@iis.u-tokyo.ac.jp).

Digital Object Identifier 10.1109/JSSC.2004.837259

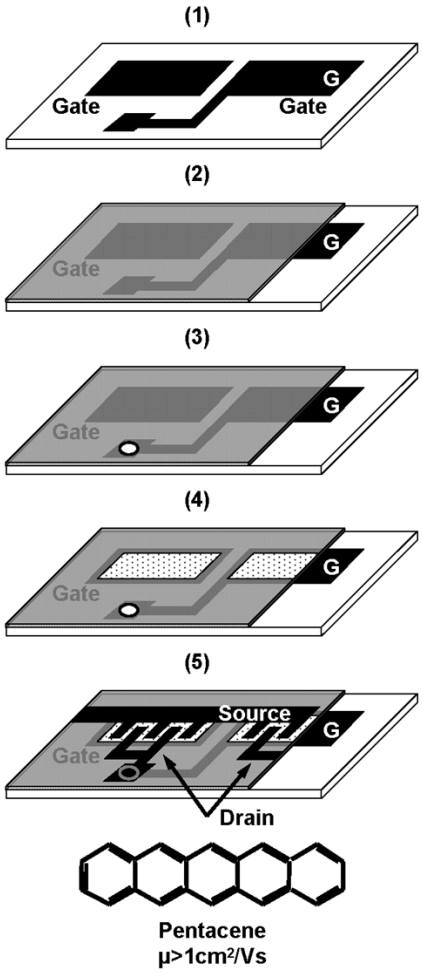

Fig. 1. Manufacturing flow of OFET. (1) Patterning of Cr/Au gate electrodes on PEN/PI base film. (2) Spin-coating and curing of gate insulator PI. (3) Via process with CO_2 laser drill machine. (4) Deposition of pentacene. (5) Deposition of Au source/drain electrodes.

(3) Some parts of the gate insulator layer is removed by a CO_2 laser to make via holes, which is described in the following subsection.
(4) Next, pentacene is deposited as an organic semiconductor layer through a shadow mask by vacuum sublimation at the pressure of 30 μPa at ambient substrate temperature. The nominal thickness of the pentacene layer is 50 nm. The chemical structure of pentacene is shown in the bottom of the figure. Pentacene is one of the fastest and most popular low-molecular-weight p-channel organic semiconductors. Deposition of pentacene thin film requires the vacuum systems, but the mobility of pentacene sometimes exceeds 1 cm^2/Vs, which is one or two orders of magnitude higher than those of other n-channel organic semiconductors and polymer.
(5) Finally, 60-nm-thick Au is deposited though a shadow mask to form source and drain electrodes.

This device structure is called top contact geometry. The device dimensions are determined by resolution of the shadow masks, which adopt 100-μm rule in this study. The initial transistor yield exceeds 99%. The major fault mode is gate leakage caused by a pinhole. One may think about incorporating redundancy and error correction code in the array. Unfortunately, however, being different from the memories, the pressure sensor is close to a display where physical location of a sensor cell is meaningful. As is a common practice in normal displays, the number of defects of a certain level will be tolerated even in a product.

The cross section of the sensor cell is shown in Fig. 2(a). The device structure of the OFET looks similar to a silicon MOSFET but the channel layer is made of pentacene. On the OFET sheet, a through-hole sheet, pressure-sensitive conductive rubber sheet, and top electrode sheet are laminated to form the sensor cell, whose circuit diagram is shown in Fig. 2(b). Hereafter, we call the sensor cell "sencel" for short. The through-hole sheet with round diameter of 100 μm is prepared by the conventional method of making flexible circuit boards, combination of chemical etching, mechanical drilling, and plating. Note that this through-hole connects pressure-sensitive conductive rubber and OFETs, and is totally different from the via holes described in the next subsection, which connects gates and drains of OFETs. The pressure-sensitive conductive rubber sheet is a 0.5-mm-thick silicone rubber containing graphite particles. The upper one is the Cu (copper) electrode sheet suspended by PI. The access OFET is connected to the pressure sensor via the through hole. WL and BL mean word line and bit line, respectively.

B. Via Holes

A CO_2 laser marker selectively formed via holes through the PI gate insulator layer. The CO_2 laser can drill one via hole per second, and implements an OFET drain to an OFET gate interconnection. This via hole is in the OFET sheet and different from the through hole found in the through-hole sheet. In order to improve productivity of the via holes, other industrial laser drill machines could be utilized. When the laser power is set to more than 8 mJ, good interconnection can be realized. By optimizing condition of the laser-via process, the yield exceeds 99% per pulse when a criterion of the conductance is set to more than 10^{-2} S. This result means that the yield becomes as high as 99.99% if the two laser pulses are irradiated onto each electrode, which is adopted in the experiments. Fig. 3 is a micrograph of the laser-via hole with a diameter of 90 μm.

C. Device Characteristics

Fig. 4 shows the measured V_{DS}–I_{DS} characteristics of the fabricated p-channel OFET. In the circuit design, only p-channel OFETs are used since mobility of n-channel organic semiconductors ever reported is 0.1 cm^2/Vs at best, which is an order of magnitude smaller than n-channel OFET, and resultant circuits made from n-channel OFET are slow. Moreover, n-channel materials are much more sensitive to oxygen and humidity than pentacene. They deteriorate in a shorter time in the atmosphere.

The measurement curves can be closely reproduced by the simulation based on the level 1 SPICE MOS model with 200-kΩ serial resistors to both source and drain when L (channel length) and W (channel width) are 100 μm and 2 mm, respectively. The maximum % error between the measured results and SPICE simulation is 7.2% when the on current I_{D0} is set to 100%. Since I_{D0} can be fit 100%, the delay simulation

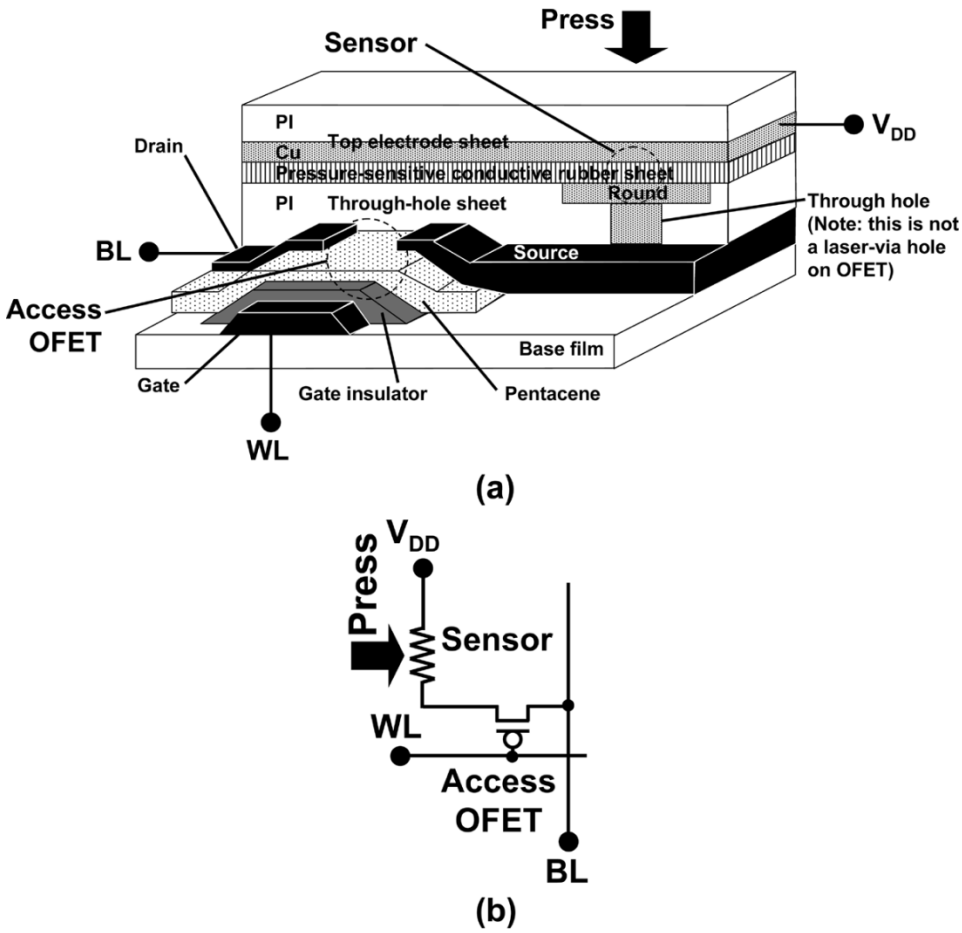

Fig. 2. (a) Cross section and (b) circuit diagram of sensor cell.

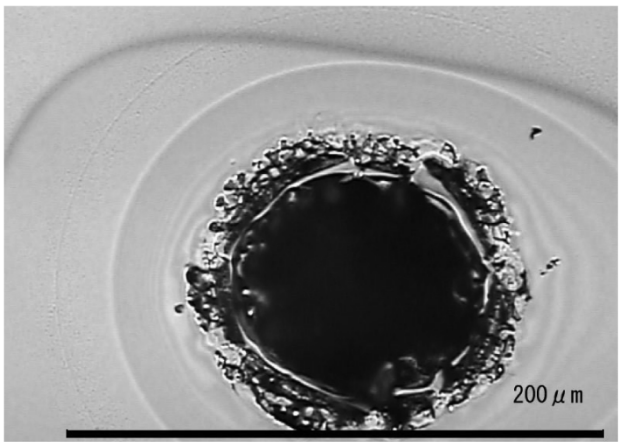

Fig. 3. Micrograph of 90-μm diameter laser via-hole.

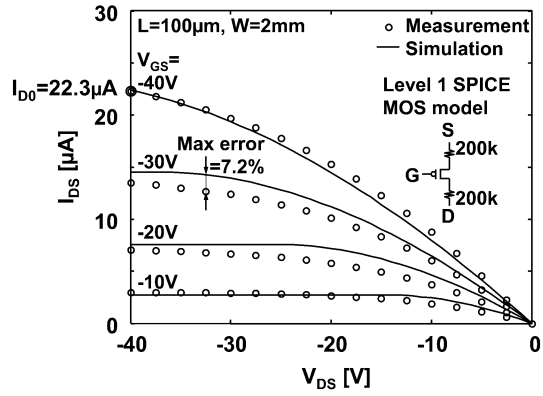

Fig. 4. $V_{\rm DS}$–$I_{\rm DS}$ characteristics of fabricated p-channel OFET.

is sufficiently accurate. It is possible to predict the circuit behavior by the SPICE simulations, which is good news for the circuit community. The layout of the circuit is carried out using the existing EDA tool, which is also good news to circuit designers. The GDS II data file resulted from the layout design is then converted into a DXF file format and handed to a metal mask manufacturer.

$I_{\rm DS}$ changes in time in the atmosphere. The rapid change in $V_{\rm DS}$–$I_{\rm DS}$ characteristics occurs on the order of minutes to days with the materials and structure used in this study. This should be the most stringent problem related to OFETs but silicon in very early days was suffering from the same problem, and it was fully remedied by now. OFETs have a hysteresis in $I_{\rm DS}$, but it does not affect the digital circuit operation.

III. Concept of Cut-and-Paste Customization

A. Concept

Fig. 5 shows the photograph of the assembled electronic artificial-skin system. A 16×16 sencel matrix, row decoders, and column selectors are separately fabricated. The sencel size is 2.54 mm $\times$ 2.54 mm (0.1 in $\times$ 0.1 in), which corresponds to

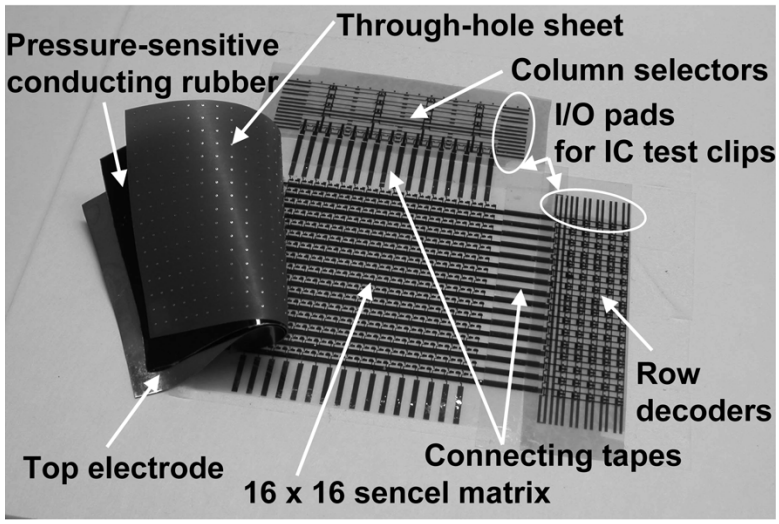

Fig. 5. Photograph of electronic artificial-skin system.

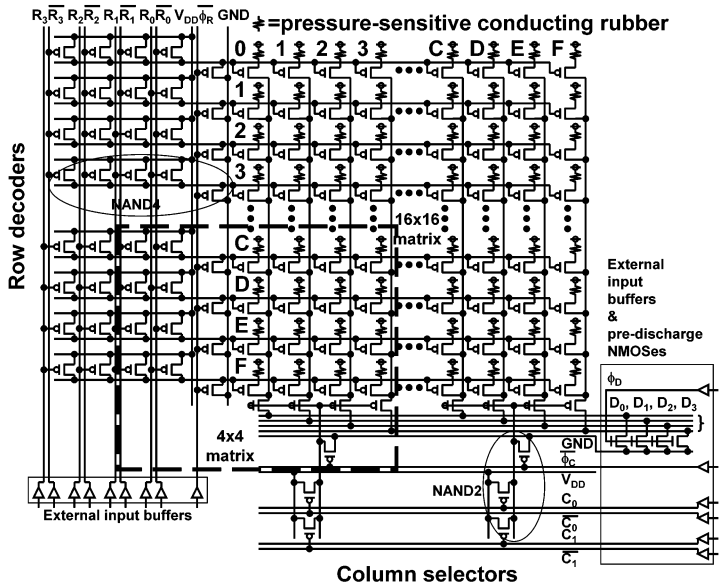

Fig. 6. Circuit diagram of electronic artificial-skin system.

10 dpi and the total area of the sencel matrix is 4 cm $\times$ 4 cm. The three parts are connected together with a PET film with evaporated Au stripes of 2.54-mm pitch and conductive glue, which is called a connecting tape in this paper. This connecting tape enables the cut-and-paste customization in size.

A circuit diagram of the electronic artificial-skin system is shown in Fig. 6. All inputs are driven by the Toshiba TD62981P buffers that can output up to 120 V. The data outputs $(\mathrm{D}_0, \ldots, \mathrm{D}_3)$ are externally pre-discharged by the pre-discharge signal ϕ_D with the NMOSes (Siemens BSS101). The off current of the NMOS is less than 30 nA. A high-voltage probe with 100-MΩ input resistance and 3-pF input capacitance that can be driven by the OFETs is used to observe waveforms. The 3 pF is not much of a problem because the gate capacitance of the OFET is as much as 60 pF. As shown in Fig. 5, the I/O pads are wide enough for IC test clips to easily connect test leads. The electrostatic discharge (ESD) immunity is 200 V at the input pads with 10-MΩ protection resistor when IEC61000-4-2 test is carried out.

In order to realize the cut-and-paste customization, all parts of the system must have scalability in size. The sencel matrix is scalable since it is a simple repetition of sencels. The sencel matrix in the required size is just cut out of the original sheet. The row decoder and column selector are laid out so that any m rows $\times\, 4n$ columns $(m \leq 16, n \leq 4)$ sencel matrix can be driven just by cutting required parts out of the original sheets of the circuits to maintain the scalability.

The left figure in Fig. 7 shows the original row decoders, which activates 1 word line out of 16 word lines. When 1 out of 4 decoders is needed, just cut the dotted rectangle from the original row decoders. The scalability is achieved by using wired-NAND type decoders. In the figure, $\overline{\phi_\mathrm{R}}$ is the row-decoder activation signal, which makes one word line low to activate sencels on the word line. The decoder circuit is explained in the following subsection in detail. This type of circuit can be realized thanks to the high on/off ratio of the OFET (more than 10^5), and is also preferable since the characteristics of the OFETs are suffering from large process

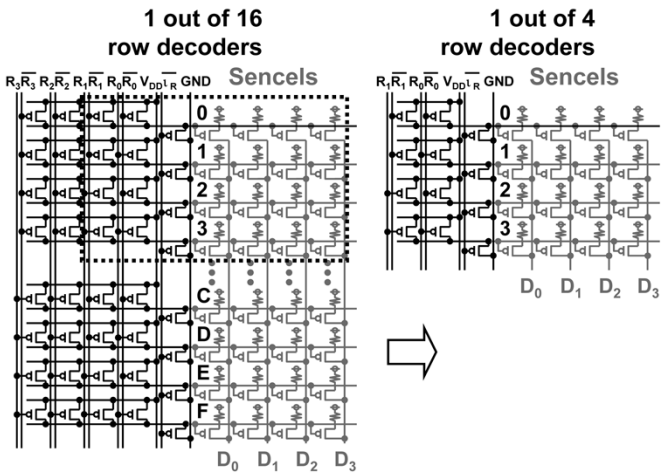

Fig. 7. Scalability of row decoders.

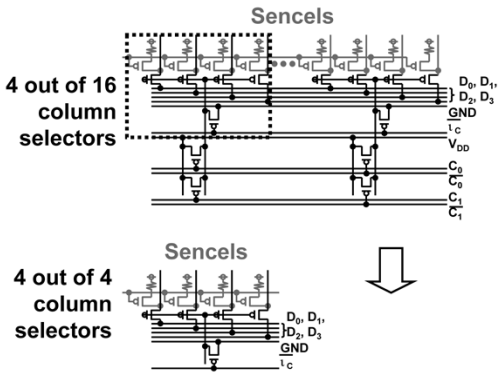

Fig. 8. Scalability of column selectors.

fluctuation. Similarly, the column selectors can have scalability as shown in Fig. 8.

Since each part has the scalability, if for example a smaller area sensor of 4×4 sencels surrounded by the dashed line in Fig. 6 is needed, the scaled-down version works without modification. The photograph of the 4×4 version is shown in Fig. 9. Unless the row decoder and column selector sides are cut off, it works fine to cut and remove the corner of the other two sides as far as the matrix is convex. The required shape of the sencel matrix does not need to be rectangular being different from a normal memory matrix. This feature is suitable for robot skin application where a nonrectangular area sensor is sometimes needed.

Although the fabricated sencel matrix in this paper has 16×16 cells, the concept can be expanded not only to small sizes but also to arbitrarily large size. A long sheet of row decoder and column selectors, and a large area sensor matrix can be fabricated and prepared in advance. When the required size and shape is fixed, an appropriate part of the circuit are cut out of the pre-fabricated sheets and then glued together with the connecting tape. For humanoid robots, fingers need small-area electronic artificial skin while a body requires large area. It is not cost-effective to prepare all different sizes of masks or products. In terms of mask cost, the concept of cut-and-paste customization is preferable because there is no need to make new masks depending on the required sizes and shapes. This

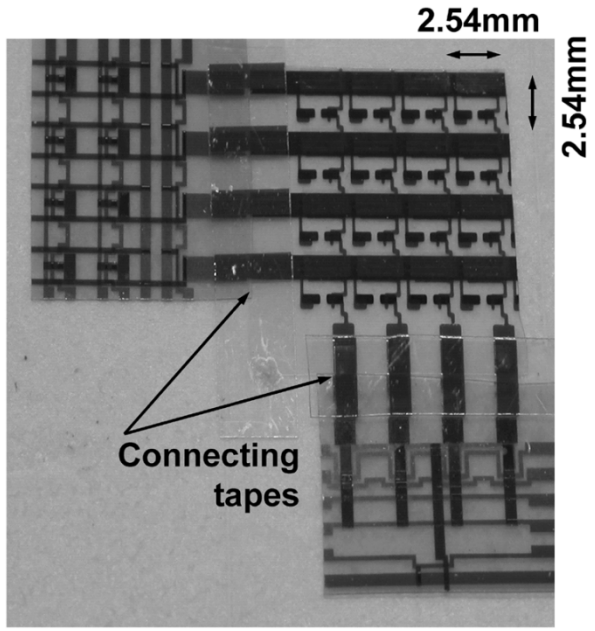

Fig. 9. 4×4 version of electronic artificial skin.

reduces turnaround time and nonrecurring engineering (NRE) cost as well.

B. Decoder Circuit

Fig. 10 shows three candidates for a decoder circuit. It should be noted that the fabricated OFET shows enhancement type characteristics and the threshold voltage of OFET cannot be changed by impurity doping like in silicon. Fig. 10(a) has an off-state load, and is similar to an $\mathrm{E/D}$ (enhancement/depletion) configuration but the load is also enhancement. Since the load is the enhancement type, the load transistor must be large to sink current, which leads to slow speed as shown in the waveforms in the figure. The second candidate is an $\mathrm{E/E}$ (enhancement/enhancement) configuration as shown in Fig. 10(b), and the load acts as a MOS diode. The current drive of the load in this configuration is low where the output is around the threshold voltage, $|V_{\mathrm{THP}}|$. Therefore, the output does not go below $|V_{\mathrm{THP}}|$, which leads to lower operational margin.

The last candidate in Fig. 10(c) has a boosted-gate load that is adopted in this design. The waveform of the decoder activation signal, $\overline{\phi}$, is shown in the waveform. The negatively boosted voltage to the gate keeps the output of the decoder "high" in a dormant state while it accelerates the transition to "low" when activated with the positively boosted voltage. The "high" outputs suppress leakage in the sencel matrix as well as the leakage current of the decoder itself. The output easily goes to GND level, which increases on-current of a pressed sencel in the matrix. This circuit is named a dynamic boosted-gate $\mathrm{E/E}$. Although $\overline{\phi}$ works out of the rails, reliability issue of the gate insulator is not existent because the gate breakdown voltage is more than 100 V. Since $\overline{\phi}$ is supplied from the external circuit, it can be used to adjust the operation point change due to variability.

Each input-output transfer characteristics of the decoders are shown in Fig. 11. The off-load decoder, Fig. 11(a), works nearly

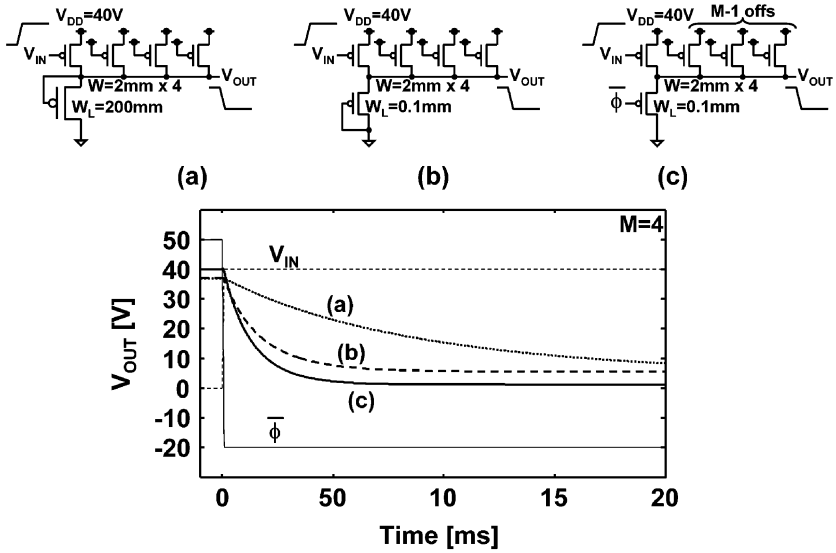

Fig. 10. Decoder circuits with (a) off-state load, (b) diode load, and (c) boosted-gate load. Their simulation waveforms are also depicted.

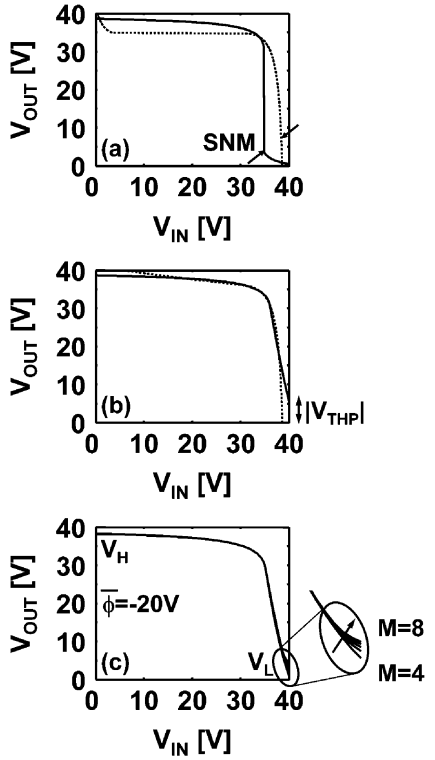

Fig. 11. Solid lines indicate input–output transfer characteristics corresponding to Fig. 10 while dotted lines are *X–Y* symmetry of the solid lines.

between the full rails, and opens an eye pattern with some static noise margin (SNM). A circuit with deep logic depth like an inverter chain requires an appropriate SNM. On the other hand, the diode-load decoder has smaller SNM as shown in Fig. 11(b), and cannot output complete "low," which is apart from GND by $|V_{\rm THP}|$. In Fig. 11(c), the dynamic boosted-gate $\rm E/E$ configuration can closely output the rail-to-rail ($V_{\rm H}$ and $V_{\rm L}$), and thus is adopted in this design. Althoug the dynamic boosted-gate decoder is superior, $V_{\rm L}$ is worsen as the number of the off-state OFETs in the decoder [$\rm M-1$ in Fig. 10(c)] increases.

C. Scalability Limit

In this subsection, factors that hinder scalability of the area sensor are discussed. The $\rm S/N$ (signal-to-noise ratio) determines the maximum number of sencels in the matrix. In this electronic artificial-skin system, there are four output lines, and each output line can convey 1-bit data to the external electronics as described previously.

Fig. 12(a) shows a case where only one of the accessed sencels is pressed, which means that on-current of the accessed sencel, $I_{\rm SON}$, flows to the bit line. This corresponds to the smallest on-current case. This should be compared to the largest off-current case, which is shown in Fig. 12(b) where the accessed sencel is not pressed and all the other sencels are pressed. The worst-case off-current is $(2^M-1+2^{N-2}-1)I_{\rm SOFF}$, where M and N signify the number of bits in row decoders and column selectors, respectively. Thus, the $\rm S/N$ is $I_{\rm SON}/I_{\rm SOFF}/(2^M-1+2^{N-2}-1)$. Assuming that $M=N$ and M and N are large, the $\rm S/N$ is expressed as $0.8I_{\rm SON}/I_{\rm SOFF}/2^M$.

Although the original on/off ratio of the OFET is more than 10^5, $I_{\rm SON}/I_{\rm SOFF}$ can be lowered to 10^3 because $V_{\rm H}$ and $V_{\rm L}$ are not strictly on the rail. $V_{\rm H}$ is slightly lower than $V_{\rm DD}$ as well as $V_{\rm L}$ is degraded as increasing M, which is discussed in the previous subsection. Thus, the theoretical maximum size of the simple matrix is around 512×512 in our current process technology. This number, however, will be improved to almost infinity if hierarchical arrangement of simple matrix is used to extend the size in the future when more complicated circuits can be manufactured without a risk of yield degradation.

IV. Experimental Result and Discussion

Fig. 13 shows a measured $I_{\rm DS}$ dependence on pressure. The resistance of the pressure-sensitive conducting rubber rapidly changes from 10 MΩ to 1 kΩ when certain pressure is given. Therefore, the pressure-sensitive rubber is not suitable for an analog circuit, and in this paper, is for the digital use. The off resistance is sufficiently larger than the drain resistance and the on resistance is much smaller than the drain resistance in the

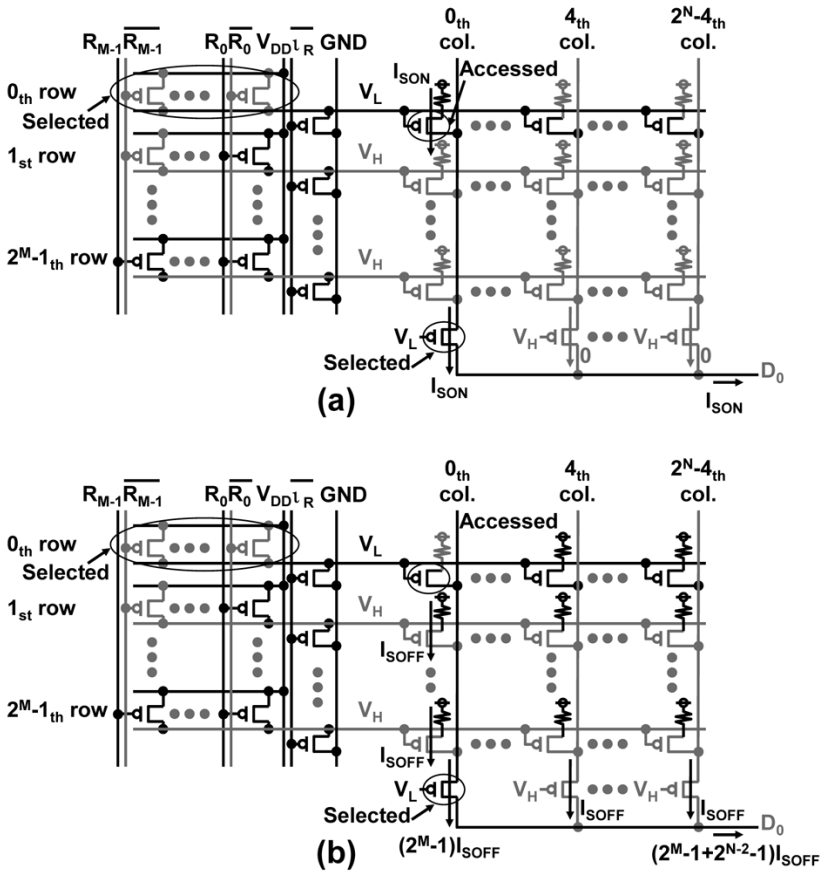

Fig. 12. (a) is a case where only one sencel is pressed while (b) shows a case where only one sencel is not pressed and the others are pressed.

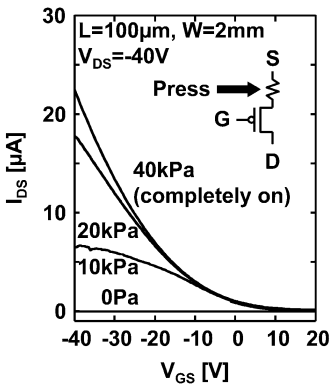

Fig. 13. Pressure dependence of sencel.

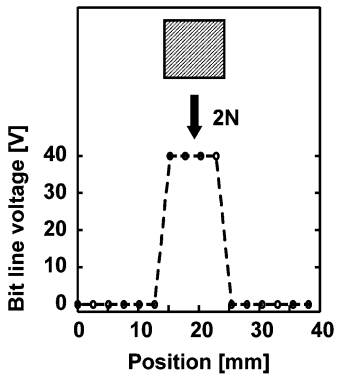

Fig. 14. Bit line voltage when pressed.

wide temperature range between $-30°$C and 120°C [8]. When a rectangular object presses one line of the sencel matrix, only corresponding parts of the pressure-sensitive conducting rubber turn on and the corresponding sencels pull the bit lines up to $V_{\rm DD}$ as shown in Fig. 14. The measured dynamic power consumption is 100 μW for the 16×16 sencel matrix. The static power is 20 μW when 100% of the area is pressed.

Fig. 15 shows access time dependence on the sencel size. Since interconnects are wide and its resistance is negligible, the access time linearly depends on the capacitance as in a silicon implementation. As known in silicon memory designs, if the matrix size is very large, a double word and bit line architecture can be adopted to reduce delay caused by long and capacitive word and bit lines. Thus, in the future the delay for the larger matrix can be reduced by implementing architectural improvements with some extra cost.

Fig. 16 shows the measured and simulated operation waveforms of the electronic artificial-skin system. The access time from the row decoder activation signal $\overline{\phi_{\rm R}}$ to the bit-out signal is 23 ms when the sense voltage of the bit-out signal is 20 V. The cycle time can be within 30 ms, which means that the time needed to scan over the whole 16×16 sencel matrix is about $2{\rm s}(=30\ {\rm ms} \times 16 \times 4)$ since 4-bit data can be read out in parallel. It is also shown in the figure that the scan speed can be enhanced by an order of magnitude if L is scaled down to 25 μm assuming a future process technology and the sense voltage is lowered to 10 V instead of 20 V. Reducing the line width of the

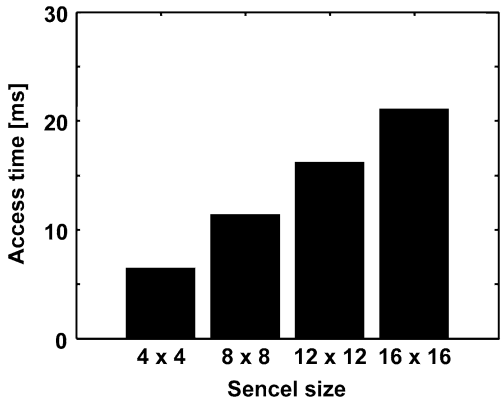

Fig. 15. Simulated access time dependence when sencel size is changed.

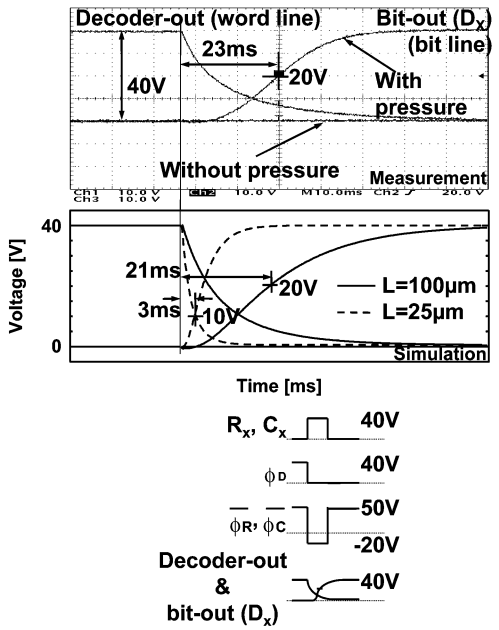

Fig. 16. Measured and simulated operation waveforms.

word lines, bit lines, and other bus lines to reduce capacitances is also effective in enhancing the scan time by another order of magnitude in the future process technology.

The access time dependence on $V_{\rm DD}$ is shown in Fig. 17. Increasing $V_{\rm DD}$ up to 100 V, the delay can be reduced to about a half. The simulation using the above-mentioned level 1 SPICE MOS model agrees well with the measurement points. In the future, however, the high operation voltage of 40 V should be lowered to less than 12 V for a typical consumer use. Lowering operation voltage is not considered very difficult by introducing shorter channel length to OFETs, which is feasible because the current channel length is 100 μm and there is much room to shrink down without technical obstacles. Thinning gate insulator layer that can be realized by increasing a rotation speed of spin coating without degrading surface roughness enhances conductivity of an OFET [7]. A use of high-k materials is also helpful for further reduction of the operation voltage as well as silicon.

The OFET can be bent down to 5 mm in radius without material fatigue or snapping off although the weakest part in bending

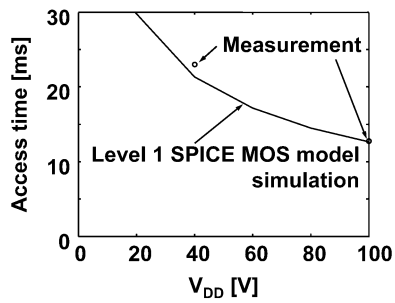

Fig. 17. Access time dependence on $V_{\rm DD}$.

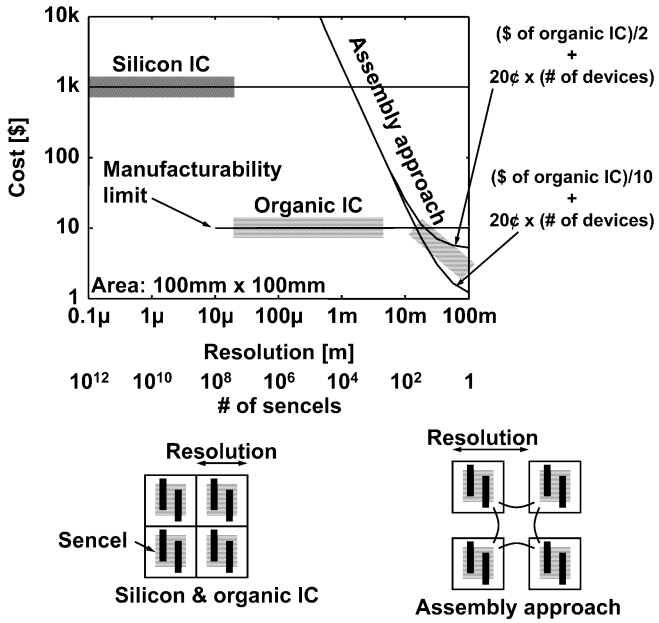

Fig. 18. Costs of technologies for large area. Area is assumed to be 100 mm $\times$ 100 mm, and silicon costs \$1 k per that area while organic costs \$10.

is a source/drain Au electrode on the pentacene, which is sufficient to wrap around the surface of a round object like a robot. The change of the OFET current caused by bending is measured using a bare OFET without a pressure-sensitive conductive conducting rubber sheet or encapsulation. When tensile strain is incurred to the OFET being bended around a bar of 5 mm in radius, the current is decreased by 3%. The OFET is fully functional even when bending radius is 1 mm [9]. This demonstrates the mechanical flexibility of the organic circuits.

A tentative cost comparison is given in Fig. 18. The range where organic ICs have cost advantage lies between tens of microns and millimeters resolution. Note that the resolution does not mean the design rule nor device size but it means sencel sparseness. The lower bound is limited by manufacturability of the organic IC while the upper bound is limited by the competition against an assembly approach. In the assembly approach, small organic sheets are assembled on a sheet of base material, and connected together by additional interconnections.

V. Summary

An electronic artificial-skin system based on organic field-effect transistors has been described, consisting of a large-area

pressure sensor, row decoders, and column selectors. The electronic artificial skin has mechanical flexibility and is low cost even for large-area electronics. A laser-via process is employed to make via holes through to the gate insulator layer. A scalable circuit concept with cut-and-paste customization is proposed and demonstrated. The circuit with dynamic boosted-gate E/E is designed using a standard SPICE simulator and layout design tool. The access time of the manufactured electronic artificial skin is 23 ms. Mechanical flexibility of the organic field-effect transistor is proven by bending it down to 5 mm in radius. A resolution range where organic IC is superior in terms of cost lies between tens of micrometers and millimeters resolution.

ACKNOWLEDGMENT

The authors would like to express their deep appreciation to S. Iba and Y. Kato for their assistance in the fabrication and experiment, and T. Kobayashi for useful discussions and valuable suggestions.

REFERENCES

[1] R. Brederlow, S. Briole, H. Klauk, M. Halik, U. Zschieschang, G. Schmid, J.-M. Gorriz-Saez, C. Pacha, R. Thewes, and W. Weber, "Evaluation of the performance potential of organic TFT circuits," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2003, pp. 378–379.

[2] E. Huitema, G. Gelinck, B. van der Putten, E. Cantatore, E. van Veenendaal, L. Schrijnemakers, B.-H. Huisman, and D. M. Leeuw, "Plastic transistors in active-matrix displays," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2003, pp. 380–381.

[3] E. Cantatore, C. M. Hart, M. Digioia, G. H. Gelinck, T. C. T. Geuns, H. E. A. Huitema, L. R. R. Schrijnemakers, E. van Veenendaal, and D. M. Leeuw, "Circuit yield of organic integrated electronics," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2003, pp. 382–383.

[4] T. Someya and T. Sakurai, "Integration of organic field-effect transistors and rubbery pressure sensors for artificial skin applications," in *IEDM Tech. Dig.*, Dec. 2003, pp. 203–206.

[5] T. Someya, H. Kawaguchi, and T. Sakurai, "Cut-and-paste organic FET customized IC's for application to artificial skin," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2004, pp. 288–289.

[6] T. Someya, T. Sekitani, S. Iba, Y. Kato, H. Kawaguchi, and T. Sakurai, "A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications," *Proc. Nat. Academy of Sciences USA*, vol. 101, no. 27, pp. 9966–9970, Jul. 6, 2004.

[7] Y. Kato, S. Iba, R. Teramoto, T. Sekitani, T. Someya, H. Kawaguchi, and T. Sakurai, "High mobility of pentacene field-effect transistors with polyimide gate dielectric layers," *Appl. Phys. Lett.*, May 5, 2004.

[8] *PCR Technical web page*, http://www.scn-net.ne.jp/~eagle/CSA-Japanese_right.html#h-ondo (in Japanese).

[9] T. Sekitani, H. Kawaguchi, T. Sakurai, and T. Someya, "Organic field-effect transistors with bending radius down to 1 mm," in *Proc. Materials Research Society Spring Mtg.*, Apr. 2004.

Hiroshi Kawaguchi (M'98) was born in Kobe, Japan, in 1968. He received the B.S. and M.S. degrees in electronic engineering from Chiba University, Japan, in 1991 and 1993, respectively.

He joined Konami Corporation, Japan, in 1993, where he developed arcade entertainment systems. He moved to the Institute of Industrial Science, University of Tokyo, Japan, in 1996 as a Technical Associate, and he is currently a Research Associate. His research interests include low-voltage VLSI designs, low-power hardware systems, wireless circuits, and organic-transistor circuits.

Mr. Kawaguchi is a member of the Association for Computing Machinery (ACM).

Takao Someya (S'92–M'94) received the Ph.D. degree in electrical engineering from the University of Tokyo in 1997.

In 1997, he joined the Institute of Industrial Science (IIS), University of Tokyo, as a Research Associate and was appointed to be a Lecturer of the Research Center for Advanced Science and Technology (RCAST), University of Tokyo, in 1998, and an Associate Professor of RCAST in 2002. From 2001 to 2003, he worked for the Nanocenter (NSEC) of Columbia University as a Visiting Scholar. Since 2003, he has been an Associate Professor of the Department of Applied Physics, University of Tokyo. His current research interests include organic transistors, flexible electronics, plastic circuits, and molecular scale electronics.

Prof. Someya is a member of the IEEE Electron Devices Society, the Materials Research Society (MRS), and the Japanese Society of Applied Physics.

Tsuyoshi Sekitani received the B.S. degree from Osaka University, Japan, and the Ph.D. degree in applied physics from the University of Tokyo, Japan, in 1999 and 2003, respectively.

From 1999 to 2003, he was with the Institute for Solid State Physics (ISSP), University of Tokyo, where he developed measurement techniques in magnetic fields up to 600 T and studied the solid-state physics of condensed matter, especially in high-T_c superconductors. Since 2003, he has been a Research Associate of the Quantum-Phase Electronics Center, University of Tokyo. His current object of physics research is organic semiconductors and organic-FET devices.

Dr. Sekitani is a member of the American Physical Society (APS), the Materials Research Society (MRS), the Physical Society of Japan, and the Japanese Society of Applied Physics.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from the University of Tokyo, Japan, in 1981.

In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 to 1990, he was a Visiting Researcher at the University of California at Berkeley, where he conducted research in the field of VLSI CAD. Since 1996, he has been a Professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, and wireless systems. He has published more than 400 technical papers including 70 invited papers and several books, and has filed more than 100 patents. He is also a consultant to U.S. startup companies.

Prof. Sakurai served as a Conference Chair for IEEE/JSAP Symposium on VLSI Circuits, and IEEE ICICDT, a Vice Chair for ACM/IEEE Asia and South Pacific DAC, and a program committee member for IEEE International Solid-State Circuits Conference, IEEE Custom Integrated Circuits Conference, ACM/IEEE Design Automation Conference, ACM/IEEE International Conference on CAD, ACM FPGA workshop, ACM/IEEE International Symposium on Low-Power Electronics and Design, ACM/IEEE International Workshop on Timing Issues, and other international conferences. He was a plenary speaker for the 2003 ISSCC. He is an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE Circuits and Systems Society Distinguished Lecturer.