Managing Subthreshold Leakage in Charge-Based Analog Circuits With Low-$V_{\rm TH}$ Transistors by Analog T- Switch (AT-Switch) and Super Cut-off CMOS (SCCMOS)

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***Abstract*—The analog T-switch (AT-switch) scheme is introduced to suppress subthreshold-leakage problems in charge-based analog circuits such as switched capacitors and sample-and-hold circuits. A 0.5-V sigma-delta modulator is manufactured in a 0.15-μm FD-SOI process with low $V_{\rm TH}$ of 0.1 V using the concept. The scheme is compared with another leakage-suppression scheme based on super cut-off CMOS (SCCMOS) and the conventional circuit which are also fabricated. The sigma-delta modulator based on AT-switch greatly improves 8.1-dB SNDR through reducing nonlinear leakage effects while the modulator based on SCCMOS improves the dynamic range rather than the SNDR by comparing with the conventional sigma-delta modulator**

***Index Terms*—Low $V_{\rm TH}$, FD-SOI, sigma-delta modulator, subthreshold leakage, switched capacitor.**

I. Introduction

LOW-VOLTAGE, low-power, yet inexpensive VLSIs are getting focus recently. To this end, analog building blocks tend to be embedded in scaled digital circuits as a part of system-on-a-chip (SoC) implemented with advanced VLSI technology. The International Technology Roadmap for Semiconductors (ITRS) predicts that the threshold voltage $V_{\rm TH}$ of high-performance logic technology will continue to decrease to sub-0.1 V. In the above-mentioned environments, very low $V_{\rm TH}$ processes compatible with the mainstream scaled digital circuits are to be used.

Several sub-1-V sigma-delta modulators and ADCs have been reported, but all are implemented in a high-threshold voltage process [1]–[3]. Previous works mainly tackled the realization of low-voltage analog circuits using high-$V_{\rm TH}$ devices, and consequently the issue in charge-based analog circuits was high resistance of MOS switches. To reduce on-state resistance, gates of MOS switches are widened or higher voltages are applied by bootstrap [4].

On the other hand, low-$V_{\rm TH}$ devices relax designs of low-voltage operation. In the low-$V_{\rm TH}$ process, however, nonlinear subthreshold leakage current can be a critical issue on analog circuits. To suppress the subthreshold-leakage problems for switched-capacitor circuits, a scheme based on super cut-off CMOS (SCCMOS) [5] was proposed [7]. This scheme, however, handles voltage outside the power rails and thus an oxide-stress-relaxed level shifter and a negative voltage generator such as a charge-pumping circuit is required [8].

In this paper, the analog T-switch (AT-switch) scheme, which can realize reverse gate-source voltage $V_{\rm GS}$ without voltages outside the power rails, is introduced to suppress subthreshold leakage problems for charge-based analog circuits.

Section II briefly reviews an issue caused by subthreshold leakage in charge-based analog circuits and the leakage-suppression scheme based on SCCMOS. Section III presents details of the proposed AT-switch scheme. Section IV demonstrates experimental results from the test chip of the 0.5-V sigma-delta modulator manufactured in a 0.15-μm FD-SOI process with low $V_{\rm TH}$ of 0.1 V using the concept, and discusses the performance and advantages comparing with the conventional scheme and the SCCMOS scheme. Finally, conclusions are given in Section V.

II. Subthreshold-Leakage Issue and SCCMOS Scheme

A. Subthreshold-Leakage Issue in Charge-Based Analog Circuits

The low-$V_{\rm TH}$ MOS transistor has advantages. First, it is compatible with the mainstream scaled digital circuits. Second, it enables low-voltage operation. Finally, it is useful in minimizing the size of MOS switches for the switched-capacitor circuit since the low-$V_{\rm TH}$ transistor has larger drivability. These advantages realize small and inexpensive analog circuits that can be implemented in the mainstream scaled digital process as part of SoC. However, there is a drawback, which is the large subthreshold leakage. The subthreshold leakage has been recognized as a cause of an exploding power issue in digital circuits, and SCCMOS has been proposed [5]. On the other hand, since bias current much larger than the subthreshold leakage always flows through typical analog circuits, the subthreshold-leakage current will not increase power consumption dramatically for typical analog circuits such as amplifiers. The subthreshold-leakage current, however, will be a critical issue in charge-based analog circuits such as switched-capacitor circuits and sample-and-hold circuits. Consequently, the leakage

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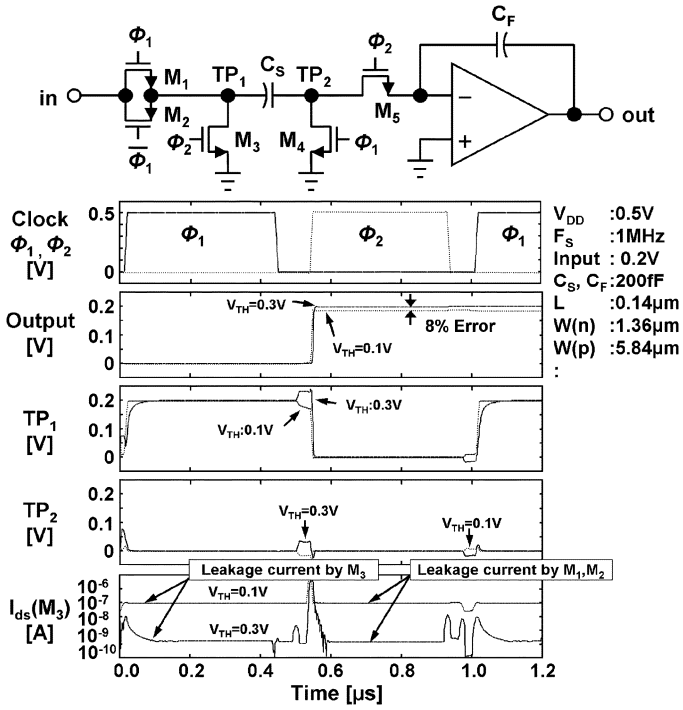


Fig. 1. Schematic and SPICE simulation results of the conventional switched-capacitor integrator.

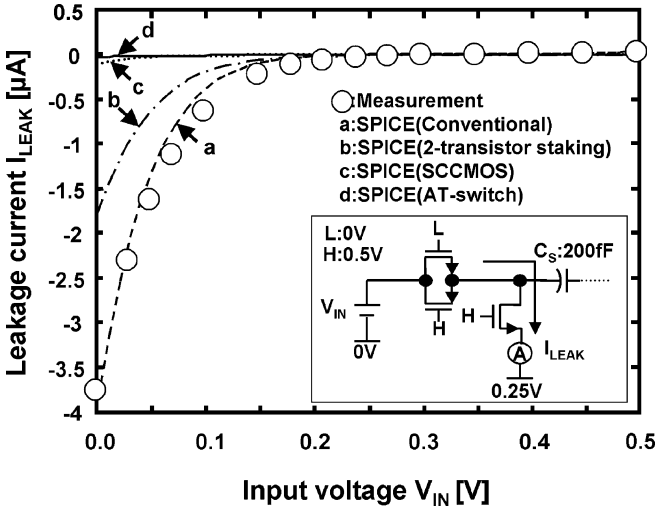


Fig. 2. Measured and simulated leakage current in the conventional switched-capacitor integrator. Simulation leakage current in the simple two-transistor staking scheme, the SCCMOS, and the AT-switch are also plotted.

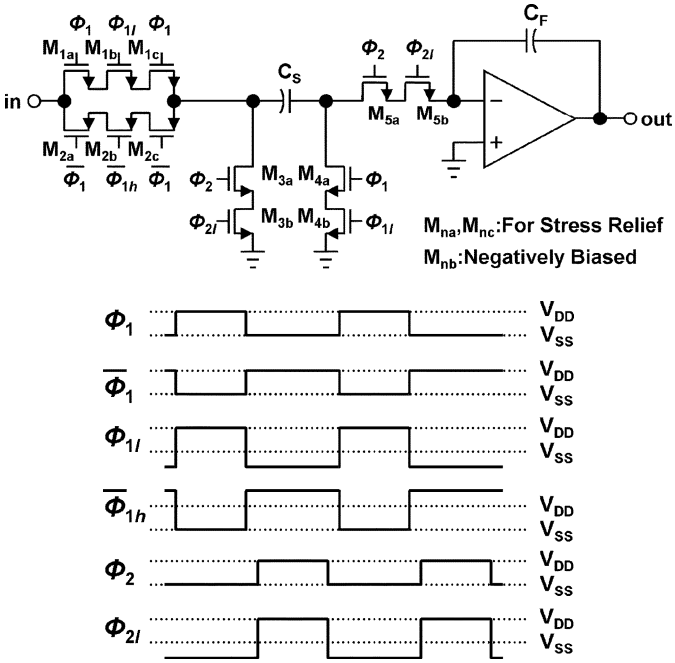


Fig. 3. Schematic of switched-capacitor integrator based on the SCCMOS [7].

current suppression scheme is becoming essentially important for the switched-capacitor-based building blocks in low-$V_{\rm TH}$ SoC environments.

Fig. 1 shows a schematic of the conventional switched-capacitor integrator and the SPICE simulation results. In the conventional switched-capacitor integrator with 0.1-V $V_{\rm TH}$ MOS switches, the leakage current exceeds 80 nA, that is over 500 times larger than the case with 0.3-V $V_{\rm TH}$ transistors. This leakage leads to the voltage error of the integrator output of 16 mV (8%), which can be considered as a voltage noise and the precision of the analog circuit is severely degraded. The expression for the subthreshold-leakage current including drain-induced barrier lowering (DIBL) effect, and the body bias effect is shown in [6]. The leakage current shows strongly nonlinear dependence on input and output voltages of the switched capacitor, which has been experimentally verified, as shown in Fig. 2, for the conventional switched capacitor implemented by a 0.15-μm FD-SOI technology with $V_{\rm THP} = -0.2$ V and $V_{\rm THN} = 0.1$ V. The measurement result shows that the voltage error of 8% is introduced by the subthreshold leakage, but this percentage error depends on the input voltage. Thus, the leakage current does introduce nonlinear errors such as in-band harmonic distortion that cannot be eliminated or digitally corrected. It is reasonable to choose low-$V_{\rm TH}$ MOS transistors to build low-voltage, low-cost, small-area switched-capacitor circuits if there is a subthreshold-leakage suppression technique.

B. Leakage-Suppression Scheme Based on SCCMOS

A schematic of a switched-capacitor circuit utilizing SCCMOS scheme presented in [7] for leakage suppression is shown in Fig. 3. In this scheme, subthreshold-leakage current is significantly suppressed by applying gate voltage below $V_{\rm SS}$ for nMOS transistors or over $V_{\rm DD}$ for pMOS transistors. The input node has a transmission gate with triply stacked structure since this node swings between $V_{\rm SS}$ and $V_{\rm DD}$. When the input signal is higher than the analog ground, the MOS transistors $\rm M_{1a}$ and $\rm M_{2c}$ relieve gate-oxide stress of the negatively biased MOS transistors $\rm M_{1b}$ and $\rm M_{2b}$. On the contrary, when the input signal is lower than the analog ground, the MOS transistors $\rm M_{1c}$ and $\rm M_{2a}$ relieve the stress. In the case that $V_{\rm TH}$ is medium to low, for example, 0.2 to 0.3 V, simple two-transistor stacking without negative bias can reduce subthreshold leakage, and the transmission gate with triply stacked structure can be replaced with doubly stacked structure.

The other nodes have doubly stacked structure since they only handle the signal around $V_{\rm SS}$. Each gate width of stacked

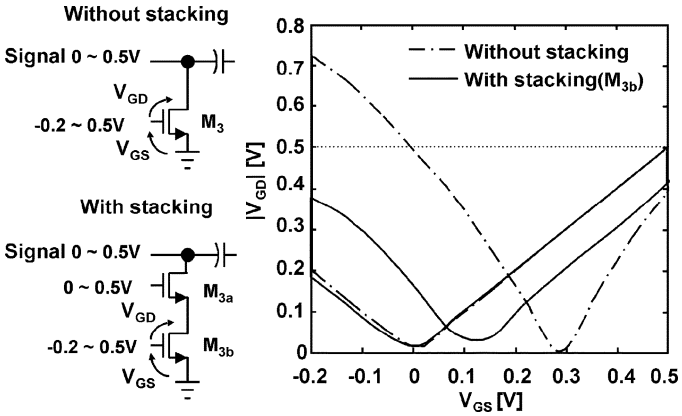


Fig. 4. Simulation results of $V_{\rm GS} - |V_{\rm GD}|$ trajectories of negatively biased switches.

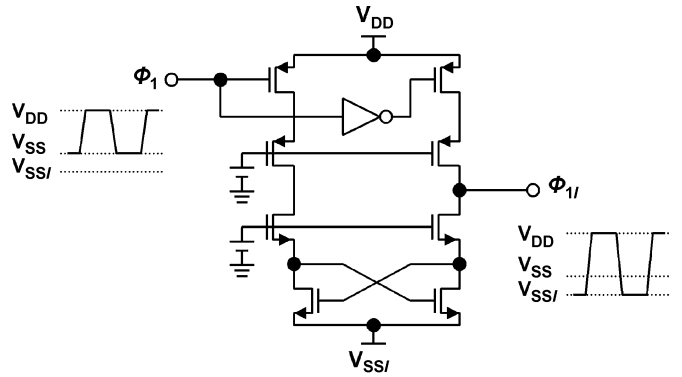


Fig. 5. Example of oxide-stress relaxed level shifter applicable to clock generator of the SCCMOS [8].

switches is two or three times wider than that of conventional switches to obtain same on-state resistance which limits bandwidth. For example, the gate of $\rm M_{3a}$ is driven by Φ_2 clock that swings between $V_{\rm SS}$ and $V_{\rm DD}$, and slightly leaky during the off phase of Φ_2. The gate of $\rm M_{3b}$ is driven by Φ_{2l} clock that swings between $V_{\rm SSL}$ and $V_{\rm DD}$ at the same timing of Φ_2. During the off phase of Φ_2, the node between the source of $\rm M_{3a}$ and the drain of $\rm M_{3b}$ is biased at intermediate voltage below the $V_{\rm DD}$. Hence, $\rm M_{3b}$ is completely cut off without gate-oxide stress.

Fig. 4 shows simulation results of $V_{\rm GS} - |V_{\rm GD}|$ trajectories of the negatively biased switches to show that the gate oxide is not over-stressed. In this case, the typical $V_{\rm DD}$ is assumed to be 0.5 V, and $V_{\rm SSL}$ is -0.2 V that is equivalent to 0.3-V $V_{\rm TH}$ during the off-state and 0.1-V $V_{\rm TH}$ during the on-state. The gate-induced barrier lowering (GIDL) effect is not an issue since the $V_{\rm TH}$ is rather low. The $|V_{\rm GD}|$ of the negatively biased switch without the stacked structure exceeds 0.5-V $V_{\rm DD}$. On the other hand, $|V_{\rm GD}|$ of the switch with a stacked structure is always below 0.5-V $V_{\rm DD}$. Although this scheme handles both low voltages below $V_{\rm SS}$ and high voltages above $V_{\rm DD}$, the gate oxide of all the transistors is biased less than $V_{\rm DD}$ for ensuring oxide reliability.

Fig. 5 depicts an example of a level shifter introduced in [8], which is applicable to a Φ_1 and Φ_2 generator. $V_{\rm DDH}$ and $V_{\rm SSL}$ can be generated by the charge-pumping circuit which was introduced in [8]. Again in these clock generation circuits, even

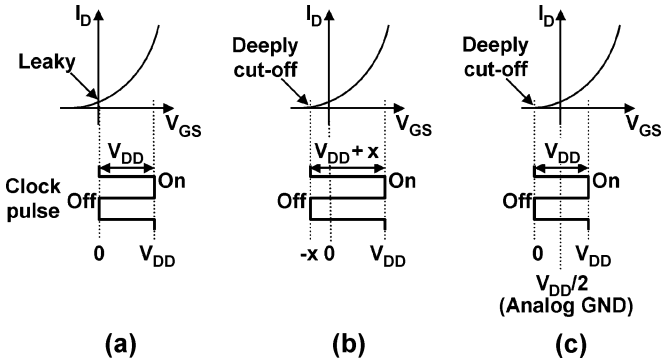


Fig. 6. Basic concept of AT-switch comparing with a conventional switch and the SCCMOS. (a) Conventional. (b) SCCMOS. (c) AT-switch.

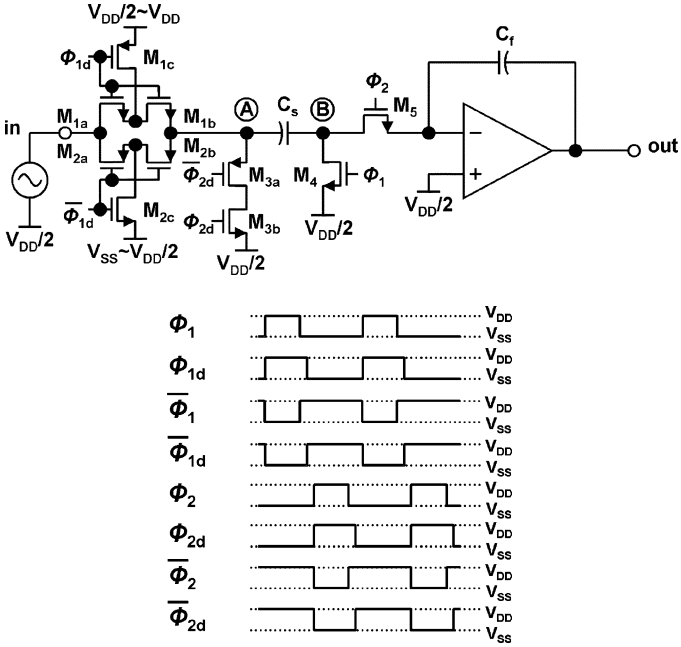


Fig. 7. Schematic of a switched-capacitor integrator using the AT-switch scheme.

though the circuit handles voltages outside the power supply rails, each transistor is free from oxide over-stress.

III. Analog T-Switch Scheme (AT-Switch)

The above-mentioned switched-capacitor circuit based on SCCMOS must handle voltage outside the power rails, and thus oxide-stress relaxed level shifters and negative voltage generators such as charge-pumping circuits are required. In this section, the AT-switch scheme, which can realize reverse gate-source voltage $V_{\rm GS}$ without voltages outside the power rails, is introduced.

Fig. 6 shows the basic concept of the AT-switch comparing with a conventional switch and the SCCMOS. A conventional switch is driven by a typical clock that swings between $V_{\rm SS}$ and $V_{\rm DD}$ as shown in Fig. 6(a), and it is leaky during the off-phase with a low-$V_{\rm TH}$ MOS. The SCCMOS shown in Fig. 6(b) is driven by a clock that swings between negatively biased voltage, below $V_{\rm SS}$, and $V_{\rm DD}$. The dynamic range of the clock is expanded and the switch is deeply cut off during the off-phase. The proposed AT-switch shown in Fig. 6(c) is driven by the typical

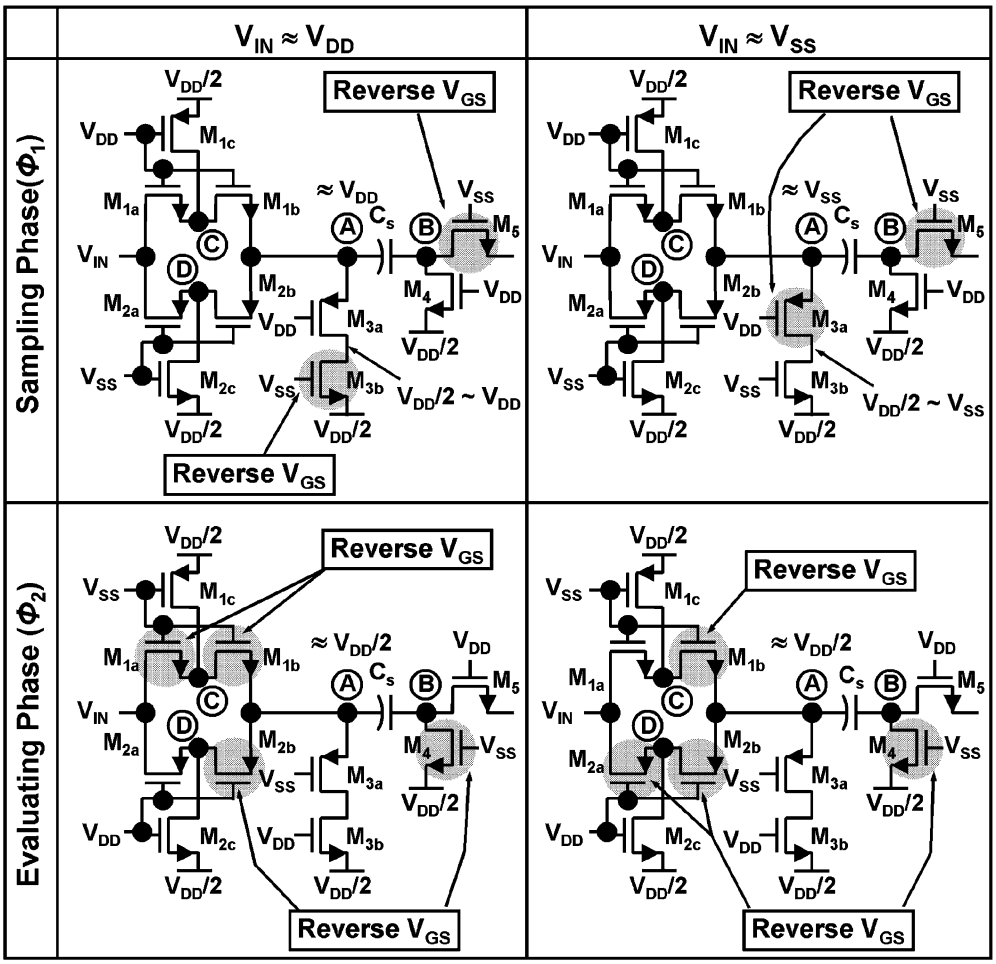


Fig. 8. Principle of the analog AT-switch scheme. Subthreshold leakage is suppressed by reverse-$V_{\rm GS}$ without voltages outside the power rails.

clock that swings between $V_{\rm SS}$ and $V_{\rm DD}$. The difference from the conventional switch is that the analog ground is set to intermediate voltage such as half $V_{\rm DD}$. Then the switch is deeply cut off by biasing with reverse $V_{\rm GS}$ during the off-phase.

To realize this concept, a schematic of a switched-capacitor integrator using the proposed AT-switch scheme is designed as shown in Fig. 7. The right-side topology of the sampling capacitor is not modified from the conventional topology since the node B in Fig. 7 is kept at a constant voltage for all the time. The gate-source of each switch is reversely biased and the leakage current is minimal. On the contrary, switches in the left side of the sampling capacitor must handle a wide range of signal voltage, and consequently the AT-switch scheme is required. $\rm M_{1a\text{-}c}$ and $\rm M_{2a\text{-}c}$ are the AT-switch that consists of two series-connected MOSFETs and an intermediate voltage-controlling MOSFET. Fig. 8 explains why the leakage can be suppressed. The analog ground is set to a proper voltage between $V_{\rm SS}$ to $V_{\rm DD}$. $V_{\rm DD}/2$ is used as an example in this paper. All MOS switches are driven by nonoverlapping clocks which swing between $V_{\rm SS}$ and $V_{\rm DD}$.

During the sampling phase, the gate voltage of $\rm M_{3b}$ is set to $V_{\rm SS}$ and that of $\rm M_{3a}$ is set to $V_{\rm DD}$ to cut them off deeply. When the input signal is around $V_{\rm DD}$, which corresponds to the upper left figure in Fig. 8, the node A is set to $V_{\rm IN}$ through $\rm M_{2a}$ and $\rm M_{2b}$. Although $\rm M_{3a}$ is still leaky, the gate-source of $\rm M_{3b}$ is reversely biased by $V_{\rm DD}/2$ and $\rm M_{3b}$ is completely cut off. If $V_{\rm DD}/2$ is 0.25 V, the leakage is reduced by two orders of magnitude.

When the input signal is around $V_{\rm SS}$, as in the upper right figure, the gate-source of $\rm M_{3a}$ is reversely biased although the $\rm M_{3b}$ is leaky.

During the evaluation phase shown in the lower figures, the gates of $\rm M_{1a}$ and $\rm M_{1b}$ are set to $V_{\rm SS}$ and the gates of $\rm M_{2a}$ and $\rm M_{2b}$ are set to $V_{\rm DD}$ to cut them off. The nodes C and D are connected to $V_{\rm DD}/2$ in this phase through $\rm M_{1c}$ and $\rm M_{2c}$, respectively. Then, both of the $V_{\rm GS}$ of $\rm M_{1b}$ and $\rm M_{2b}$ are reversely biased and they are deeply cut off even though $\rm M_{1a}$ and $\rm M_{2a}$ are leaky. Since this integrator scheme is insensitive to parasitic capacitances, added parasitic capacitances introduced by the proposed scheme do not affect the operation [9].

SPICE simulation is carried out to quantitatively compare the AT-switch with the SCCMOS and the simple two-transistor-staking scheme, as shown in Fig. 2. Although the simple two-transistor-staking scheme, "b" in Fig. 2, can reduce subthreshold leakage, it does not achieve sufficient performance for 0.1-V $V_{\rm TH}$ transistors. On the other hand, the SCCMOS, "c" in Fig. 2, and the AT-Switch, "d" in Fig. 2, reduces subthreshold leakage by almost two orders of magnitude that is reasonable performance for charge-based circuit.

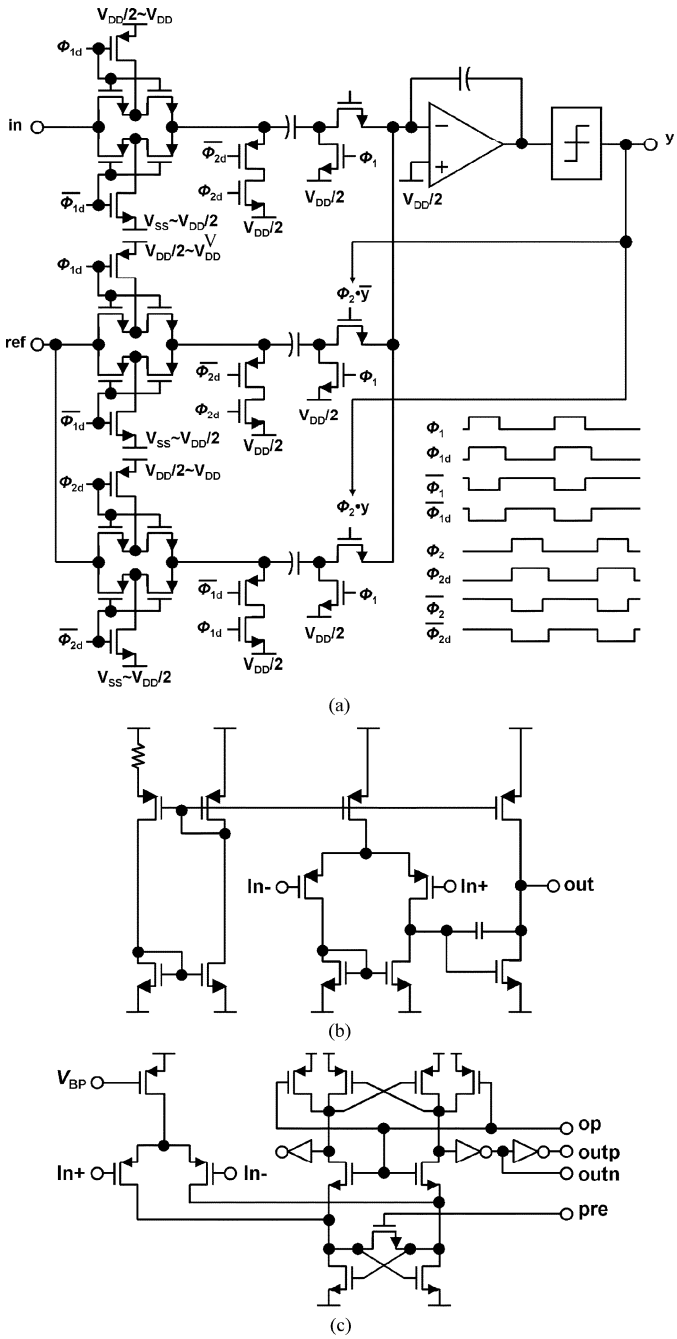


Fig. 9. Schematic of the delta-sigma modulator using AT-switch scheme designed for evaluations. (a) Overall schematic. (b) Class-A opamp. (c) Comparator.

Another type of T switch for RF/video application that is similar to the configuration of the AT-switch has been in production [10]. The switch in [10], however, addresses an issue of signal pass-through by capacitive coupling of MOS switches, that is different from the AT-switch. For the purpose in [10], nodes C and D in Fig. 8 are connected and an nMOS transistor is added to the node in order to realize a high-pass filter to cut out the signal pass-through. On the other hand, the AT-switch is intended to solve the subthreshold-leakage issue and thus nodes C and D are driven separately. That is, the node C is biased between a half

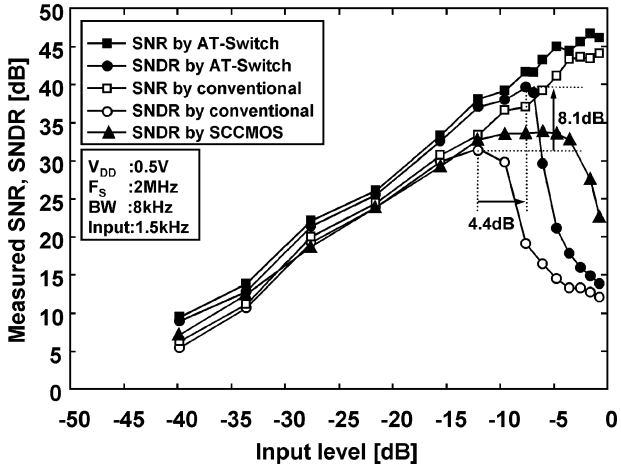


Fig. 10. Measured SNRs and SNDRs. The SNDR by SCCMOS is also plotted for comparison.

V_{DD} and V_{DD} to eliminate the leakage, while the node D is to be biased between V_{SS} to a half V_{DD}.

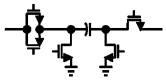
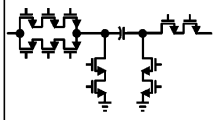
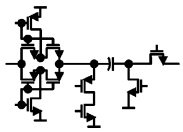
IV. Experimental Results and Discussion

Both the AT-switch scheme and the conventional scheme are applied to first-order low-pass sigma-delta modulators implemented in the 0.15-μm FD-SOI process with low V_{TH} of 0.1 V. Although the FD-SOI process is chosen for this work, the proposed scheme can also be applied to standard bulk CMOS processes. Fig. 9 depicts a schematic of the delta-sigma modulator based on the AT-switch scheme. The same circuit topology, parameters, and layout style, except for the switch array, are adopted in order to fairly compare various switched-capacitor circuits. The low-V_{TH} process can relax low-voltage circuit design. Although the amplifier in the integrator is based on the conventional two-stage class-A opamp, the circuit is operated under 0.5-V V_{DD}.

Fig. 10 demonstrates measured SNRs and SNDRs. For comparison, the SNDR by the SCCMOS scheme is also plotted. The conventional scheme achieves peak SNR of 44 dB. The SNDR of the conventional scheme, however, is degraded to 31.5 dB, which is below 5-bit resolution. The maximum power consumption is 71 μW. The proposed AT-switch scheme achieves peak SNDR of 39.6 dB, which realizes more than 6-bit resolution with maximum power consumption of 75 μW. The peak SNDR and the dynamic range are improved over the conventional approach at the same time. The SNDR by the AT-switch exceeds that of the SCCMOS by 5.8 dB. This result indicates that the AT-switch scheme can cut off the leakage more deeply than the SCCMOS approach since more reverse V_{GS} is applicable without voltage over-stress across gate oxide.

Fig. 11 shows measured output power spectra. The output bit streams were processed using Matlab. The output spectrum of the conventional scheme is taken at the input level of -7.6 dB and the large harmonic tones that degrade the SNDR are observed. This is due to the leakage current that introduces nonlinear errors. The proposed scheme shows the peak SNDR at the input level of -7.6 dB. It is seen that higher-than-third-order

TABLE I
SUMMARY OF COMPARISON ON SUBTHRESHOLD-LEAKAGE SUPPRESSED SWITCH SCHEME

	Conventional	SCCMOS	AT -switch
Number of MOS transistors	5 transistors	12 transistors	10 transistors
Schematic			
Applicable V_{TH}	High V_{TH}	Low V_{TH} (ex. V_{TH}=0.2V)	Extremely low-V_{TH} (ex. <0.1V), Depletion MOS
Outside-rail clock	N/A	Required	N/A
Level shifter	N/A	Required	N/A
Number of clock phases	8	16	8
Additional power supply	N/A	Required	N/A
P-well isolation	N/A	Required	N/A
Oxide stress	Inherently free	Relaxed by stacking	Inherently free
Applicable analog GND	V_{SS} to $1/2V_{DD}$ (NMOS) $1/2V_{DD}$ to V_{DD} (PMOS)	V_{SS} to $1/2V_{DD}$ (NMOS) $1/2V_{DD}$ to V_{DD} (PMOS)	around $1/2V_{DD}$
0.5V sigma-delta ADC Dynamic range*	–	+6.0dB	+4.4dB
0.5V sigma-delta ADC Peak SNDR*	–	+2.3dB	+8.1dB

* Relatively to the conventional ADC

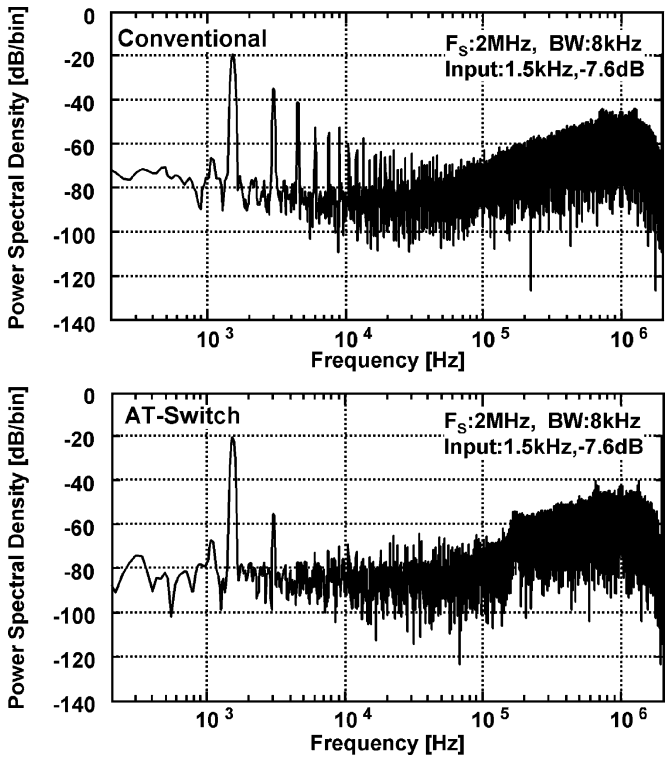


Fig. 11. Measured output power spectra.

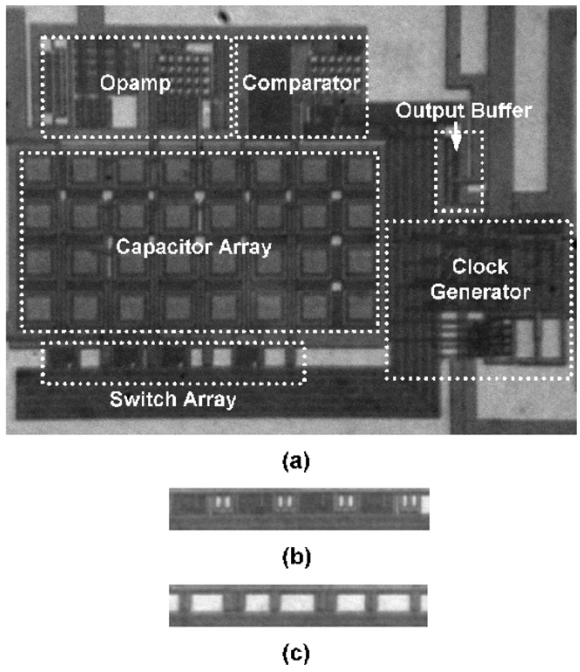


Fig. 12. Chip microphotographs of the sigma-delta modulator. (a) AT-switch. (b) Switch array of the SCCMOS. (c) Switch array of the conventional.

tones are greatly suppressed compared with the conventional circuit.

The chip microphotographs of the sigma-delta modulator using the analog T-switch, SCCMOS, and the conventional scheme are shown in Fig. 12. Area is 130 μm $\times$ 190 μm. Although the switch transistor area of the AT-switch increases to 3.3 times of the switch transistor area of the conventional circuit, the switch array area is almost unchanged. This is because the switch transistors are placed according to the pitch of capacitors and even if the number of switch transistors are more it does not give much area overhead.

Table I summarizes the comparison between two types of leakage-suppressed switch scheme and the conventional scheme. The SCCMOS requires seven additional transistors compared with the conventional scheme, and area overhead is 4%. The drawback is that two transistors are added on the right side of the sampling capacitor that will slightly affect

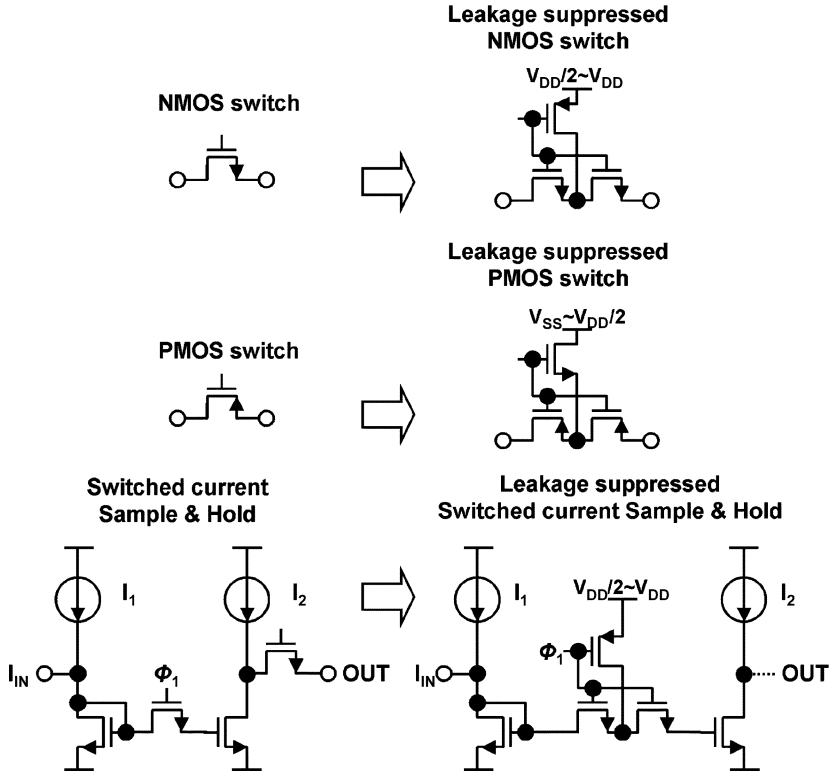


Fig. 13. Leakage suppressed switches using AT-switch scheme.

the operation as a parasitic element. On the other hand, the AT-switch requires five additional transistors, and area overhead is 3%. All of them are, however, only on the left side of sampling capacitor. Therefore, the added parasitic capacitance introduced by the AT-switch does not affect the operation. Although the SCCMOS must handle outside-rail clocks that slightly complicate circuit and layout design, the SCCMOS improves both dynamic range and SNDR comparing with the conventional scheme. Especially, 6-dB increase of the dynamic range is remarkable. On the other hand, the AT-switch does not require outside-rail clock. The drawbacks are that the scheme is applicable to only extremely low threshold voltage such as 0.1-V $V_{\rm TH}$ and analog ground should be set around half $V_{\rm DD}$ that slightly limits the signal dynamic range. Although the increase of dynamic range is below that of the SCCMOS, the AT-switch greatly improves both dynamic range of 4.4 dB and SNDR of 8.1 dB compared with the conventional sigma-delta modulator on the same silicon chip.

The AT-switch must use switch transistors with twice the channel width of the conventional switch transistor in order to maintain the conductance and to achieve the same bandwidth. Since the total charge in the channel is proportional to $W \times L$, the total charge of the AT-switch is four times more than that of the conventional scheme made with low-$V_{\rm TH}$ transistors. The conventional switch made with the low-$V_{\rm TH}$ transistor does not work properly due to the large leakage current as is described previously. Thus, the conventional switch should be implemented with high-$V_{\rm TH}$ transistors and then the channel width should be much more than the channel width of the transistors in the AT-switch. Therefore, the charge-injection problem can be mitigated over the conventional approach. If the channel charge injection problem is still critical in the AT-switch, several charge-injection cancellation techniques can be adopted such as dummy switch addition, CMOS complementary switching (which is shown in Fig. 7), and fully differential sampling circuit [11].

There are two useful circuit configurations in the AT-switch family. One is an nMOS switch substitute and the other is a pMOS switch substitute, as shown in Fig. 13. The AT-switch version of the nMOS and pMOS switches can be considered as leakage-suppressed nMOS and pMOS switches, respectively, for a wide range of applications. One such application is found in a sample-and-hold circuit with switched current configuration. Even though signal frequency is sufficiently low, that is the signal pass-through by capacitive coupling of MOS switches can be ignored, managing subthreshold-leakage current is essential in switched current configuration using low-$V_{\rm TH}$ transistors. SPICE simulation results on the switched current sample-and-hold using the conventional leaky switches and using the analog T-switch scheme are shown in Fig. 14. The device model employed is the aforementioned 0.15-μm FD-SOI. Since the conventional leaky switch cannot sufficiently cut off node TP from IN during a hold phase, TP tends to track the voltage of IN, and the output waveform has voltage error at the end of hold-phase as a result. On the contrary, TP is isolated from the node IN in the implementation with the AT-switches and consequently the voltage error observed in the conventional output is suppressed. This result indicates that the AT-switch concept is considered to be applicable to other charge-based analog circuits.

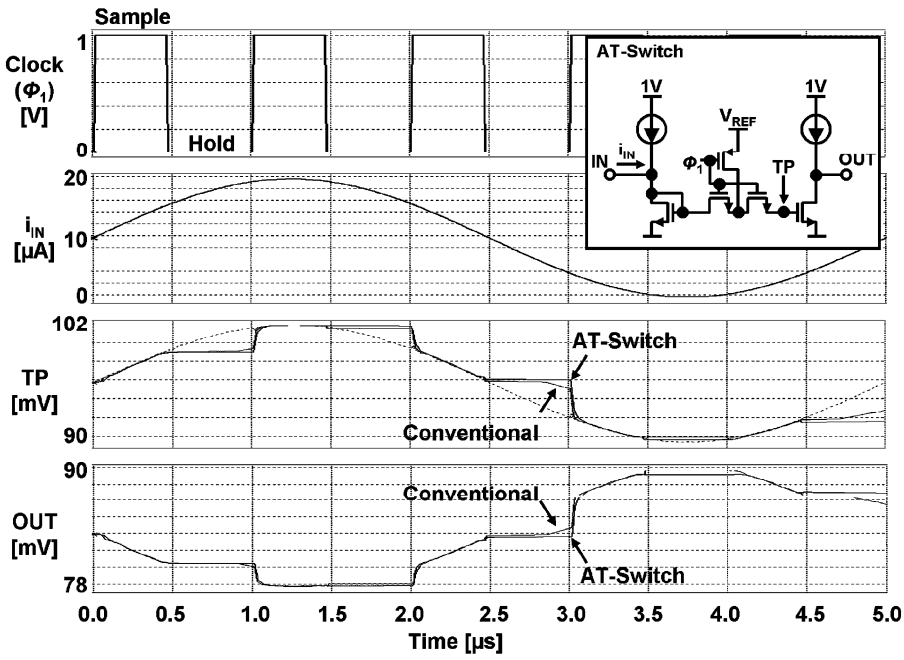


Fig. 14. Simulation results of switched current sample-and-hold.

V. Conclusion

The AT-switch scheme is introduced and applied to a 0.5-V sigma-delta modulator implemented in a 0.1 V-$V_{\rm TH}$ 0.15-μm FD-SOI process and experimentally verified. The AT-switch realizes 6-bit resolution by reducing nonlinear leakage effects caused by the leakage and loss of charge through low-$V_{\rm TH}$ transistors. The performance of the circuit based on the proposed AT-switch exceeds that of the SCCMOS and the conventional scheme. The AT-switch can be applied to extremely low-$V_{\rm TH}$ devices, even to depletion MOS transistors, since reverse $V_{\rm GS}$ is effectively achieved without voltage over-stress to gate oxide.

The AT-switch is shown to be also applicable to other charge-based analog circuit using a sample-and-hold circuit. The proposed AT-switch scheme and the SCCMOS both suppress nonlinear leakage-current effects in charge-based analog circuits and boosts circuit performances in the forthcoming leaky low-$V_{\rm TH}$ transistor generations.

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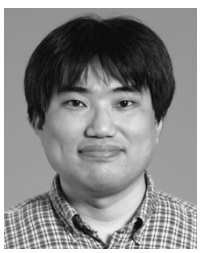

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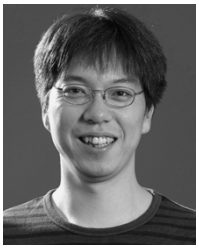

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