An Organic FET SRAM With Back Gate to Increase Static Noise Margin and Its Application to Braille Sheet Display

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***Abstract*—An integrated system of organic FETs (OFETs) and plastic actuators is proposed, and it is applied to a Braille sheet display. Some circuit technologies are presented to enhance the speed and the lifetime for the Braille sheet display. An OFET SRAM is developed to hide the slow transition of the actuators. Developed five-transistor SRAM cell reduces the number of the bit lines by one-half and reduces the SRAM cell area by 20%. Pipelining the write-operation reduced the SRAM write-time by 69%. Threshold voltage control technology using a back gate increased the static noise margin of SRAM and compensated for the chemical degradation of the OFETs after 15 days. The oscillation frequency tuning range from -82% to $+13\%$ in a five-stage ring oscillator is also demonstrated with the threshold voltage control technology. The overdrive techniques for the driver OFETs reduced the transition time of the actuator from 34 s to 2 s.**

These developed circuit technologies achieved the practical 1.75-s operation to change all 144 Braille dots on Braille sheet display and will be essential for the future large area electronics made with OFETs.

***Index Terms*—Actuator, Braille, large-area electronics, organic FET, SRAM.**

I. Introduction

LARGE-AREA electronics is a new frontier in electronics where intelligent electronic devices are distributed on a flexible square, 10 cm to 10 m on a side, for human interface and comfortable daily life. Flexible and low-cost organic FETs (OFETs) are suitable for large-area electronics and have a potential as a supplement of solid and expensive silicon MOSFETs. OFETs have been applied to active-matrix displays [1]–[3], RF-ID transponders [4], [5], and sensors [6]–[10]. They are examples of the large-area electronics except for RF-ID.

Compared with the silicon MOSFETs, however, the operation speed of OFETs is extremely slow and the device lifetime of OFETs is very short, because fabrication technologies for OFETs are not yet mature. Table I shows a comparison between our OFETs and the state-of-the-art 90-nm silicon MOSFETs. The gate delay of the OFETs is 3×10^7 times larger than that of the silicon MOSFETs, because the design rule of the OFETs is 556 times larger than that of the silicon MOSFETs and the drive current of the OFETs is 1/40000 of that of the silicon MOSFETs. The device lifetime of OFETs is several days, while that of the silicon MOSFETs is more than 10 years, because OFETs are chemically degraded by the oxygen and moisture in the atmosphere. In addition, threshold voltage (V_{TH}) control process technology such as an ion implantation is not yet established for OFETs. The cost per area of OFETs is lower than that of the silicon MOSFETs, while the cost per transistor of OFETs is higher than that of the silicon MOSFETs. In order to put the large-area electronics using OFETs into practical use, circuit technologies to assist the slow and unreliable OFETs are important.

TABLE I
Comparison Between The Reported Organic FETs (OFETs) and the State-of-the-Art Silicon MOSFETs

	OFETs	Si MOFETs
Design rule	50 μm	90 nm
Hardness	Flexible	Solid
Drive current	25 nA / μm @ 40 V	1 mA / μm @ 1 V
Gate delay	0.3 ms	10 ps
Cost / area	Low	High
Cost / transistor	High	Low
Lifetime	Days	Years

In this paper, an integrated system of OFETs and actuators is proposed, and a Braille sheet display is demonstrated [11], [12], which shows a new application of the large-area electronics using OFETs. Device and process technology of the OFETs and the plastic actuators are shown in [11] and this paper focuses on circuit technology [12]. A commercially available Braille display uses piezo actuators and displays 16 Braille characters. The usability of the conventional Braille display, however, is limited due to its weight (∼1.0 kg) and thickness (∼4 cm). The developed lightweight (∼5 g [11]) and flexible Braille sheet display expands the application of the Braille. The developed Braille sheet display has an actuator array. When the actuators are sequentially driven, it takes more than 1 hour to change the actuator array, which is impractical. To increase the speed of the actuator, OFET SRAM and overdrive techniques for a driver transistor is proposed. To achieve a reliable and stable SRAM oper-

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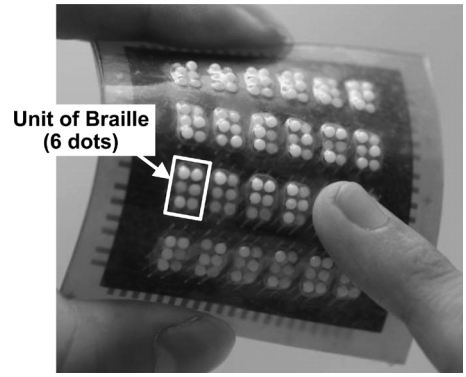


Fig. 1. Braille sheet display.

ation, a $V_{\rm TH}$ control technology using a back gate is developed. A five-transistor SRAM cell is also developed to reduce the number of bit lines and cell area. Section II provides a detailed overview of the Braille sheet display and discusses the meaning of SRAM for the display. Section III describes the developed key circuit technologies for the display. Section IV presents another application of the $V_{\rm TH}$ control technology. Section V summarizes the speed improvement and the power consumption. Finally, some concluding remarks are given in Section VI.

II. Braille Sheet Display

Fig. 1 shows the developed Braille sheet display. Braille characters in a 6×4 array are shown on the 4 cm ×4 cm display. Each Braille character consists of 2×3 dots, and the display has a total of 144 dots. As shown in Fig. 2(a), four films (frame, actuator, OFETs driver, and OFETs SRAM) are stacked in the Braille sheet display. Each Braille dot has an OFET SRAM to compensate for the slow transition of the actuator. The frame is a surface-protecting layer. Pentacene is used as an organic semiconductor and the pentacene achieves pMOS operations. Nafion is used as the actuators, PEN is used as substrates, polyimide is used as the gate dielectric, parylene is used as passivation layers, and gold is used as all electrodes. Nafion is sandwiched between the upper grounded electrode and the lower electrode. OFETs for SRAM have back gates to control $V_{\rm TH}$. As shown in Fig. 2(b), the Braille character is changed by moving the dots up and down by means of the actuator, depending on the input voltage.

Fig. 3 shows the reason why SRAM is embedded in the Braille sheet display. The display has 12 bit-lines and 12 word-lines for a 12×12 Braille dots array. The time to change all Braille dots (T1) is discussed here. Without SRAM, T1 is 408 s, because the 144 actuators are sequentially driven by 12 word lines and it takes 34 s for an actuator to move. T1 more than 1 minute is not practical. In order to reduce T1, SRAM is embedded. When the SRAM is added, T1 is the sum of SRAM write-time and the above 34 s and equals to 34.5 s, because all actuators are a simultaneously driven after the data are written to SRAM. By using SRAM, T1 is reduced from 408 s to 34.5 s, which corresponds to 1/12 of initial T1. In Section V, the 34.5-s operation time will be reduced to 1.75 s by additional techniques.

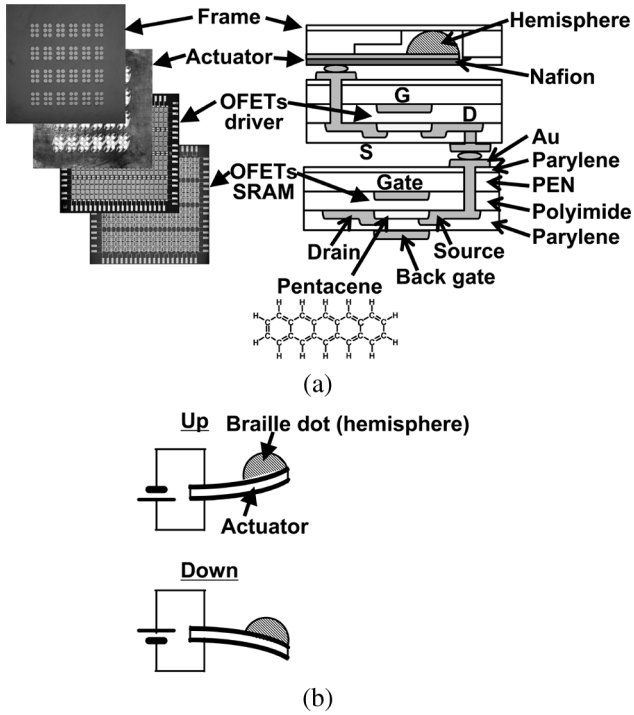


Fig. 2. (a) Device structures for the Braille sheet display. (b) Operation of the actuator.

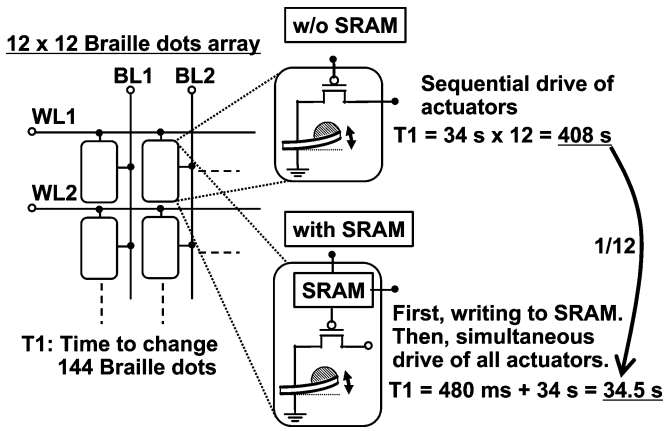


Fig. 3. Significance of SRAM in the Braille sheet display.

III. Key Circuit Technologies

A. Five-Transistor SRAM Cells and Pipelining for Write-Operation

Fig. 4 shows the circuit of the SRAM and the driver for one actuator. Only pMOS OFETs are used, because the performance of nMOS OFETs is commonly worse than pMOS. The OFETs for SRAM have back gates [13] to control $V_{\rm TH}$. A write-only SRAM is enough for our Braille application, because the actuator moves depending on the hold data (DATA, DATAb) and a SRAM read-operation is not required. Therefore, to save the film area, a five-transistor SRAM cell is developed. Compared with a conventional six-transistor SRAM cell, a five-transistor SRAM cell reduces the number of the bit lines by one-half and reduces the SRAM cell area by 20%. Fig. 5 shows a micrograph

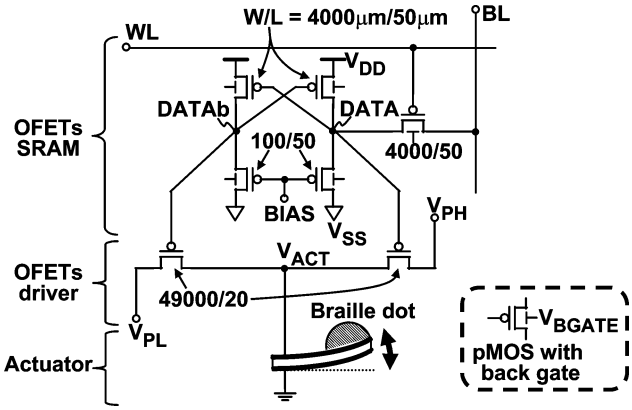


Fig. 4. Circuit of OFETs SRAM and the driver for one actuator.

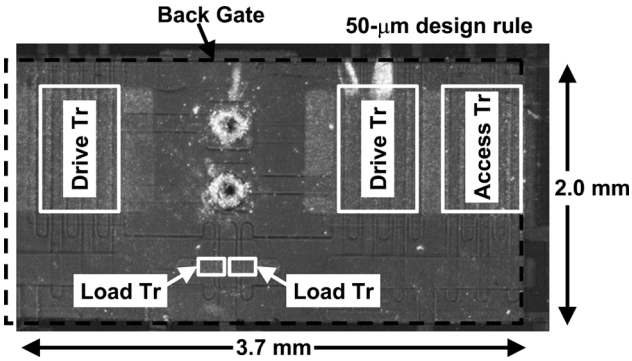


Fig. 5. Micrograph of the five-transistor SRAM cell.

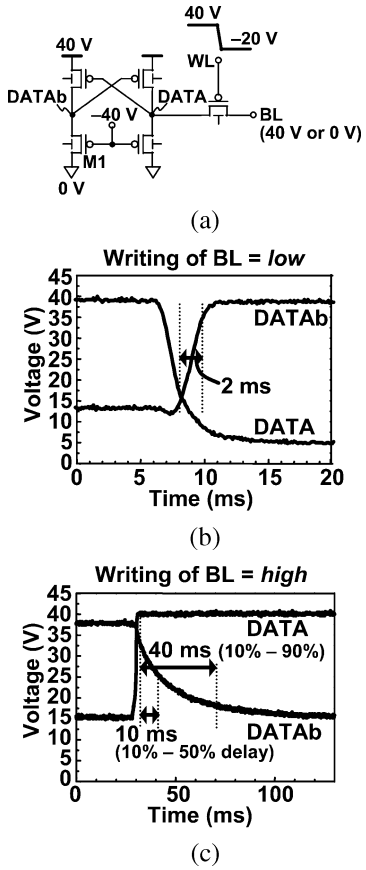


Fig. 6. (a) Measured SRAM circuits. Measured SRAM write-operation when BL is (b) low and (c) high.

of the five-transistor SRAM cell. The cell area is 3.7 mm by 2.0 mm, which fits into the 4.0-mm-by-2.0-mm cell size for the stacked one actuator and the two driver transistors [11]. The whole cell is covered with the common back gate and each SRAM cell has the separate back gate.

In the five-transistor SRAM cell, a foremost concern is the slow write-time of DATAb, because DATAb has no access transistors. Our design target for the write-time of the whole SRAM ($= 144$ cells) is within 0.2 s. Fig. 6(a) shows the measured SRAM circuits and Fig. 6(b) and (c) show the measured waveforms of DATA and DATAb during a write-operation. In Fig. 6(b), BL of low is written to SRAM and the transition time of DATAb is 2 ms. In contrast, in Fig. 6(c), BL of high is written and the transition time of DATAb is 40 ms, because the drive current of M1 in Fig. 6(a) is small. This slow transition time can be hidden in the SRAM system-level by pipelining the write-operation. Fig. 7 shows the timing chart for the pipeline. With the pipelining in Fig. 7(b), the write-operation moves to the next SRAM cell after every 10 ms, because the 10%–50% transition time of DATAb is 10 ms in Fig. 6(c) and DATAb flips from high to low. By pipelining, the total write-time for the 12×12 SRAM cells is reduced from 480 ms ($= 40\ \mathrm{ms} \times 12$) to 150 ms ($= 10\ \mathrm{ms} \times 11 + 40\ \mathrm{ms}$), which achieves 69% delay reduction and satisfies our design target.

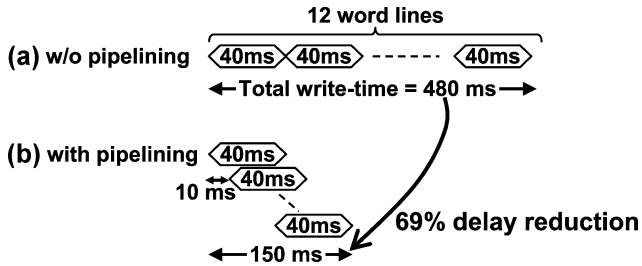


Fig. 7. Timing chart for write-time of SRAM. (a) Without pipelining. (b) With pipelining.

B. Control of SRAM Static Noise Margin With a Back Gate

The V_{TH} control technology using a back gate is shown to compensate for the immature V_{TH} control process technology and to achieve a reliable SRAM operation. Fig. 8 shows the drain current dependence of the gate voltage of a pMOS OFET. Back gate voltage (V_{BGATE}) is varied. By changing V_{BGATE}, V_{TH} can be controlled. Fig. 9(a) shows measured inverters in the SRAM and Fig. 9(b) shows the measured butterfly curves of the SRAM. Back gate voltage (V_{BGATE}) is varied. The static noise margin (SNM) increases as V_{BGATE} increases. The inverter gain is 2.7. It is difficult to obtain a larger inverter gain, because the SRAM uses only pMOS OFETs. Therefore, it is important to control V_{TH} in the OFET SRAM in order to obtain a sufficient SNM by using the low-gain inverters. Fig. 9(c) shows the measured V_{BGATE} dependence of SNM. The power supply voltage (V_{DD}) is varied. When V_{DD} is 40 V, SNM increases as V_{BGATE} increases. In contrast, when V_{DD} is 20 V, an optimum $V_{\mathrm{BGATE}} - V_{\mathrm{DD}}$ of 25 V achieves the maximum SNM, because

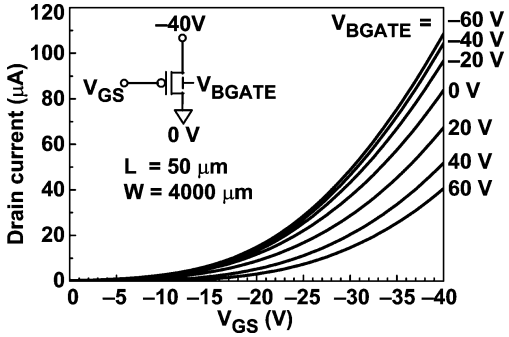
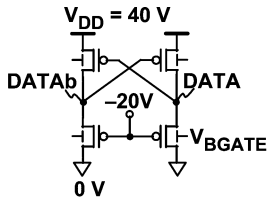
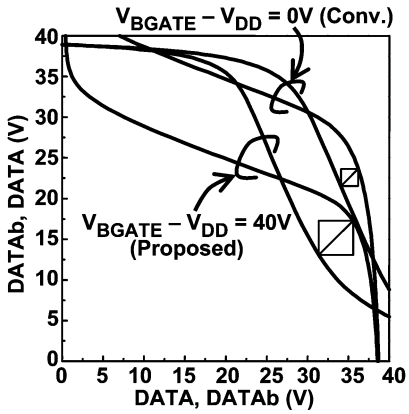


Fig. 8. $I_{\rm D}-V_{\rm GS}$ characteristics of a pMOS OFET with varied $V_{\rm BGATE}$.



(a)



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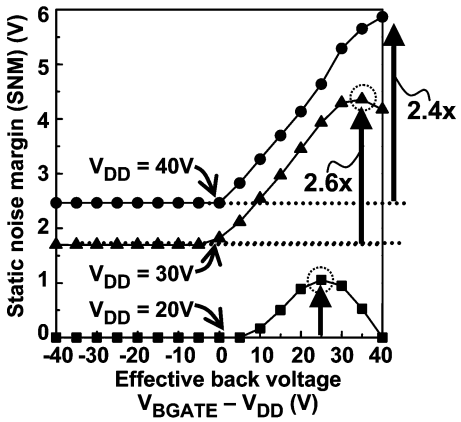

(c)

Fig. 9. (a) Measured inverters in SRAM. (b) Butterfly curves of SRAM with varied $V_{\rm BGATE}$. (c) $V_{\rm BGATE}$ dependence of SNM.

there is an optimum $|V_{\rm TH}|$ of OFETs. Compared with SNM at $V_{\rm BGATE}-V_{\rm DD}=0\,V$, by adjusting $V_{\rm BGATE}$, SNM increases 2.4 and 2.6 times when $V_{\rm DD}$ is 40 V and 30 V, respectively.

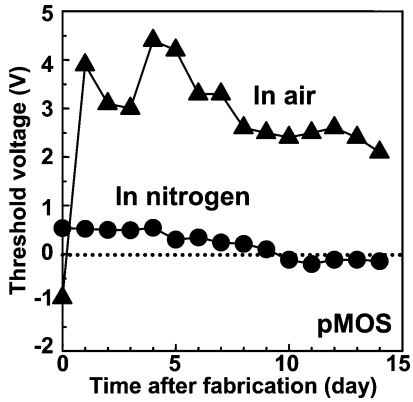

Fig. 10. Dependence of $V_{\rm TH}$ of pMOS OFETs on the time after fabrication.

The chemical degradation is the most serious problem for OFETs. Fig. 10 shows a measured dependence of $V_{\rm TH}$ of pMOS OFETs on the time after fabrication. It should be noted that the OFETs in Fig. 10 is different from the OFETs used in the Braille sheet display and have no correlation with all the other figures. Amplitude of $V_{\rm TH}$ shift during 14 days is 5.3 V and 0.68 V in the air and in nitrogen, respectively. $V_{\rm TH}$ shift in the air is larger than that in nitrogen, because the oxygen and moisture in the air enhances the chemical degradation. Both $V_{\rm TH}$ shifts, however, are too large and are not acceptable for SRAM design. Therefore, the $V_{\rm TH}$ control technology is also applied to compensate for the chemical degradation of OFETs and to achieve a reliable SRAM operation. Fig. 11(a) shows a measured inverter in the SRAM and Fig. 11(b) shows the measured aging characteristics of the inverter without the $V_{\rm TH}$ control technology. The inverter was kept in a nitrogen atmosphere without bias stressing except for the measuring time. As time passes, the inverter characteristics show a rightward shift due to the reduced $|V_{\rm TH}|$ of OFETs. Similar rightward shift of the inverter characteristics after 7800-s bias stressing is reported in [14], which is because of the electrical degradation. Fig. 11(c) compares the measured virgin characteristics of the inverter without the compensation and aging characteristics of the inverter compensated by the back gate. By manually adjusting $V_{\rm BGATE}$, the chemical degradation after 15 days is successfully compensated and the similar inverter characteristics are obtained. Fig. 11(d) shows the aging characteristics of SNM calculated based to Fig. 11(b) and (c). By compensating the reduced $|V_{\rm TH}|$ of OFETs due to the chemical degradation with the back gate, the reduced SNM after 15 days recovers to the initial level. When $V_{\rm BGATE}$ is adaptively controlled, a constant SNM can be achieved. Because the chemical degradation is inherent in OFETs, the proposed compensation technology is essential to OFET applications. Of course, the process technology improvement is also important to extend the device lifetime. Our recent results show little $V_{\rm TH}$ shift after 60 days exposure in air by newly developed passivation layer [15]. However, further process technology improvement is required to put OFETs to practical use. Systematic manufacturing variation within a plastic film for the OFETs can also be compensated by dividing the back gate and adaptively applying different $V_{\rm BGATE}$.

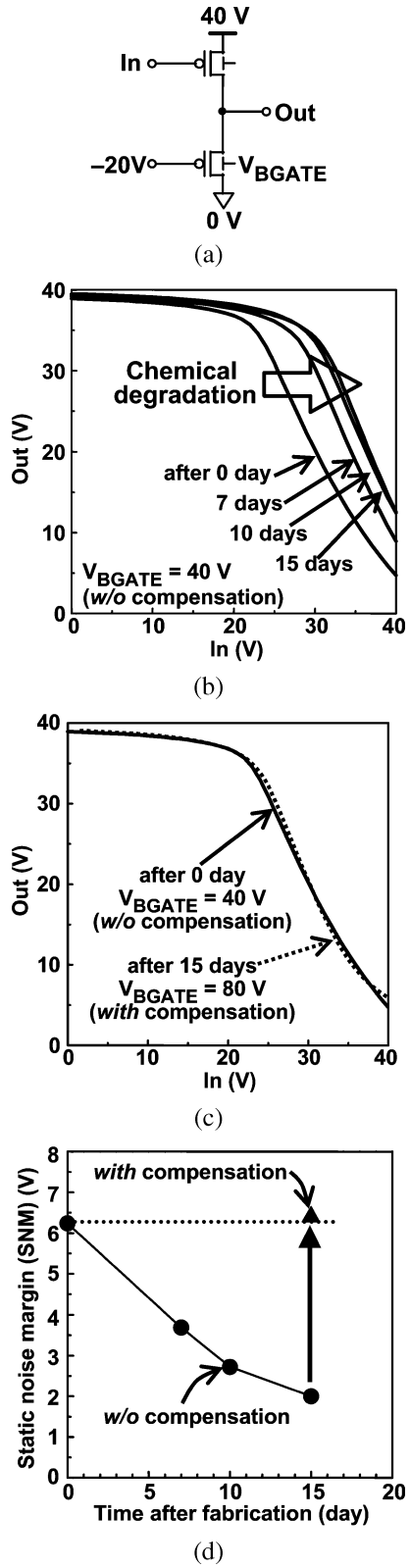

Fig. 11. (a) Measured inverter in SRAM. (b) Aging characteristics of the inverter without the $V_{\rm TH}$ control technology. (c) Virgin characteristics of the inverter without the compensation and aging characteristics of the inverter compensated by the back gate. (d) Aging characteristics of SNM.

C. Overdrive Techniques for Driver Transistors

Our design target for the transition time of the actuator is within 2 s. Fig. 12(a) shows the driver circuits for the actuator to investigate overdrive techniques. An equivalent circuit of actuator is also shown. In order to achieve the fast movement of the actuator, large drive current of the driver transistor is required to quickly charge and discharge the large capacitance (100 μF) of the actuator. As shown in Fig. 4, the gate width of the driver transistor is 49000 μm to obtain large drive current. The breakdown voltage of the actuator is $\pm$3 V. Fig. 12(b) shows the measured waveforms of the actuator voltage ($V_{\rm ACT}$) and the actuator displacement. The step voltage height ($V_{\rm X}$) of $V_{\rm PL}$ is varied. The required displacement by Braille users is 0.2 mm. When $V_{\rm PL}$ is equal to the breakdown voltage of -3 V, the transition time is 34 s, which exceeds our design target. In order to reduce the transition time, $V_{\rm PH}$ and $V_{\rm PL}$ overdrive techniques are proposed. By increasing $V_{\rm X}$ from -3 V to -10 V, the transition time is reduced from 34 s to 2.0 s, which satisfies our design target. In order to avoid the breakdown of the actuator, the overdrive period is determined by the time when $V_{\rm ACT}$ is within $\pm$3 V.

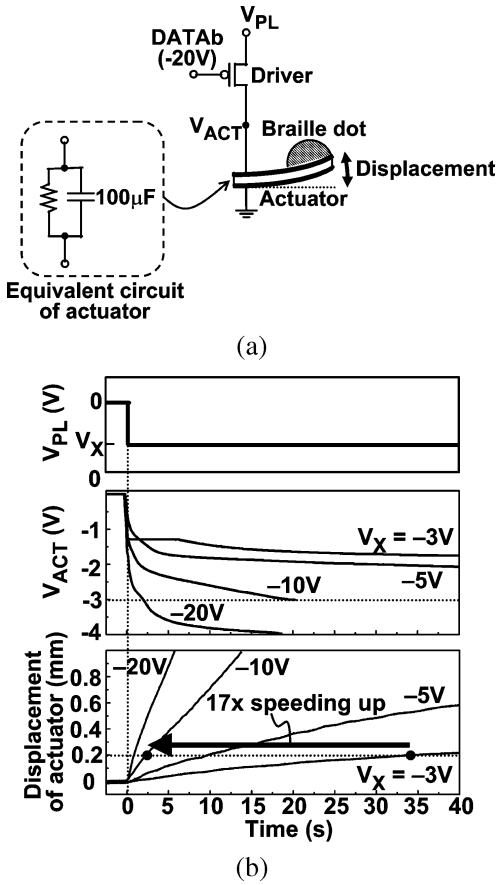

Fig. 12. (a) Measured driver and actuator circuits. (b) Accelerated actuator by overdrive techniques.

Finally, an operation of the Braille sheet display is demonstrated. Fig. 13(a) shows a measured circuits and Fig. 13(b) shows the measured waveforms of the driver and the actuator for a Braille dot. Movement of the Braille dot, both up and down, has been successfully demonstrated. By using $\pm$10-V-overdrive techniques during 2.5 s in $V_{\rm PH}$ and $V_{\rm PL}$, a 1.6-s up-transition time and a 0.74-s down-transition time of the actuator are achieved.

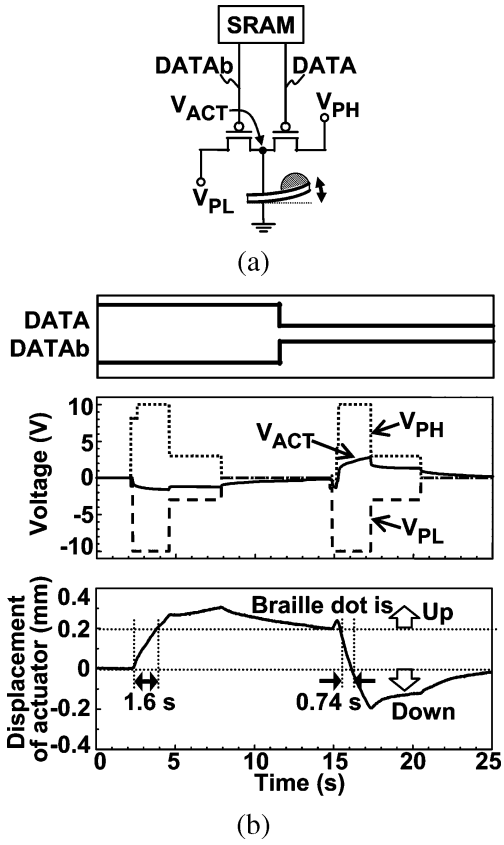

Fig. 13. (a) Measured Braille sheet display circuits. (b) Braille sheet display operation.

IV. Discussions

In the Section III-B, the control of the SRAM static noise margin with the $V_{\rm TH}$ control technology using the back gate was presented. In this section, another application of the $V_{\rm TH}$ control technology is shown. The $V_{\rm TH}$ control technology is applied to an OFET ring oscillator and an oscillation frequency tuning is demonstrated. Fig. 14(a) shows a circuit schematic of a measured five-stage ring oscillator with the back gate. The transistor sizes and the bias conditions for an inverter in the oscillator are identical with those in SRAM. The output waveform was directly measured with an oscilloscope probe with 100-MΩ input impedance and no output buffer for the oscillator is used, because the OFET gate capacitance is larger than the capacitance of a pad and the probe. Fig. 14(b) shows a micrograph of the oscillator. The area for the oscillator is 4.5 mm by 5.0 mm. All OFETs are covered with the common back gate. Fig. 14(c) shows the measured $V_{\rm BGATE}$ dependence of the oscillation frequency. At $V_{\rm BGATE} - V_{\rm DD} = 0\ V$, the center oscillation frequency is 339 Hz which corresponds to the gate delay of 0.3 ms in Table I. The oscillation frequency tuning range from 62 Hz (-82%) to 383 Hz ($+13\%$) is achieved by changing $V_{\rm BGATE}$. The frequency tuning asymmetry derives from the $V_{\rm TH}$ tuning asymmetry shown in Fig. 8 and discussed in [13]. The developed delay tuning method using the back gate enables a post-fabrication tuning of OFET circuits.

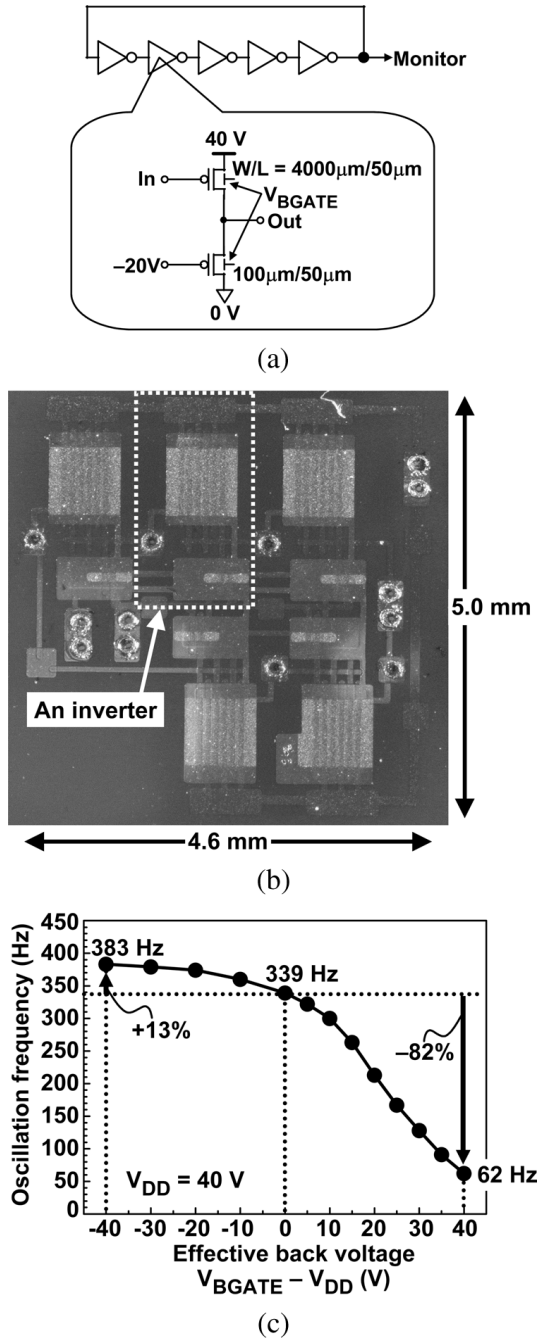

Fig. 14. (a) Measured OFET five-stage ring oscillator with the back gate. (b) Micrograph of the oscillator. (c) $V_{\rm BGATE}$ dependence of the oscillation frequency.

V. Performance Summary

Fig. 15 summarizes the time to change 144 Braille dots and the speeding up by the developed circuit technologies. At an initial design without the SRAM, it takes 408 s, because the 144 actuators are sequentially driven by 12 word lines. When the SRAM is added, it takes 34.5 s, because all actuators are a simultaneously driven after the data are written to SRAM. At a final design, the developed pipelining for SRAM write-operation and overdrive technology for the driver increased the speed

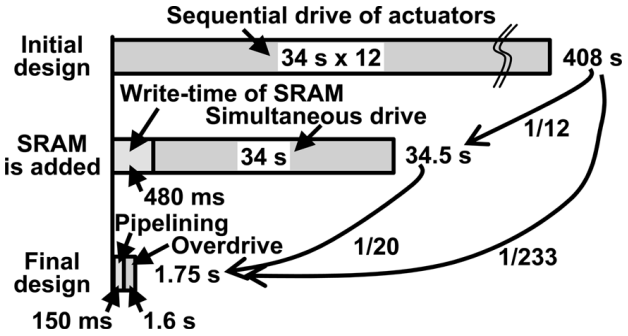

Fig. 15. Summary of speeding up Braille sheet display.

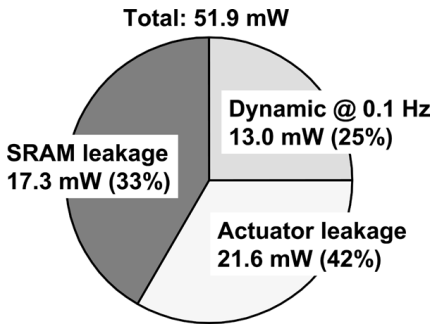

Fig. 16. Power breakdown for the Braille sheet display at 0.1-Hz operation.

of the Braille sheet display 233 times, and achieved the practical 1.75-s operation.

Fig. 16 shows the power consumption for the whole Braille sheet display at 0.1-Hz operation. The total power consumption is 51.9 mW. The dominant component is the leakage power of the actuators $(21.6\,\mathrm{mW} = 50\,\mu\mathrm{A} \times 3\,V \times 144)$. In contrast, the leakage power of piezo actuators used in a commercially available Braille display [16] is 230.4 mW $(= 8\,\mu\mathrm{A} \times 200\,V \times 144)$ which is 10.7 times larger than that of our actuators. Therefore, our plastic actuators contribute to the low power operation for the Braille display.

VI. Conclusion

OFETs were integrated with actuators, and a Braille sheet display was demonstrated. An SRAM made with OFETs is demonstrated for the first time. Pipelining the write-operation reduced the SRAM write-time by 69%. Threshold voltage control technology using a back gate increased the SNM and compensated for the chemical degradation of the OFETs after 15 days. The overdrive techniques for the driver OFETs reduced the transition time of the actuator from 34 s to 2 s.

These developed circuit technologies will be essential for the future large area electronics made with OFETs.

Acknowledgment

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