

Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs

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Abstract—An on-chip buck converter which is implemented by stacking chips and suitable for on-chip distributed power supply systems is proposed. The operation of the converter with 3-D chip stacking is experimentally verified for the first time. The manufactured converter achieves a maximum power efficiency of 62% for an output current of 70 mA and a voltage conversion ratio of 0.7 with a switching frequency of 200 MHz and a 2×2 mm on-chip LC output filter. The active part and the passive LC output filter are implemented on separate chips fabricated in 0.35- μm CMOS and connected with metal bumps. The use of glass epoxy interposer to increase the maximum power efficiency up to 71.3% is also discussed.

Index Terms—Buck converter, distributed power supply, system-in-a-package (SiP), stacked chip.

I. INTRODUCTION

RECENTLY, system-on-a-chip (SoC) and system-in-a-package (SiP) are getting more and more interest as major integration technologies. They are often used to integrate various types of circuit blocks from processors and memories to analog circuits. Each block demonstrates a different optimum supply voltage (V_{DD}) and the difference tends to increase as the technology scales. For example, memory and analog circuits tend to prefer higher voltage compared with logic blocks. Fig. 1 shows the V_{DD} trends for precision analog/RF, performance analog/RF, high-performance logic, and low-power logic with the design rule trends according to the International Technology Roadmap for Semiconductors (ITRS) 2005 [1]. Multiple- V_{DD} implementation is therefore required in low-power and high-performance systems. Moreover, supply voltage is sometimes tuned in time to achieve lower power consumption, which is called dynamic voltage scaling. The supply of many different and dynamically scaled voltages from outside the package gives rise to much overhead in area. The power line integrity, including IR drop and noise, becomes an issue as well. The distributed on-chip power supply circuits are useful for solving these problems. The concept of the distributed power supply is shown in Fig. 2. High voltage is

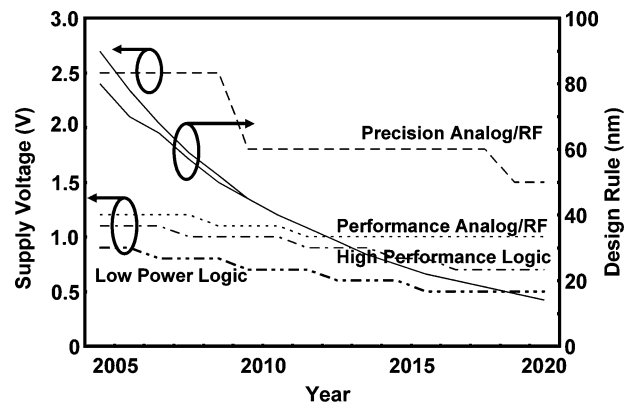


Fig. 1. Supply voltage trend with design rule trend according to ITRS.

distributed by a main power grid and is then converted to the lower voltages at the vicinity of the target blocks by distributed on-chip voltage converters. This approach reduces cost and power integrity issues.

For dc-dc converters, linear regulator, buck converters and switched capacitor converter are well known circuits. A buck converter requires large passive elements of inductance and capacitance (LC) for an output filter but it shows a higher power efficiency than a linear regulator. A switched-capacitor converter also needs large capacitors and one more drawback is that the output voltage levels are limited by the ratios of prepared capacitors. That is not very suitable for low-power dynamic voltage scaling systems.

In case of the buck converter, high switching frequency is preferable for smaller L and C but the power efficiency is degraded by the dynamic power dissipated by switching transistors at high frequency. Low quality factor (Q) of air-core and on-chip inductors also degrades the power efficiency. High inductance is good for high Q but is not easy to obtain on a chip because of the area limitation and, even if high magnetic permeability material is introduced on a chip, high- μ property is usually lost at high frequency.

A couple of integrated buck converters have been reported in recent years. Efficiency of 80%-87% was achieved at a high switching frequency of 233 MHz for voltage conversion ratios of 0.75 and 0.79 with off-chip air-core inductors in 90-nm CMOS process [2]. The air-core and surface-mount inductors whose quality factors are over 20 contribute to higher power efficiency. However, the part cost, the assembly cost and area are

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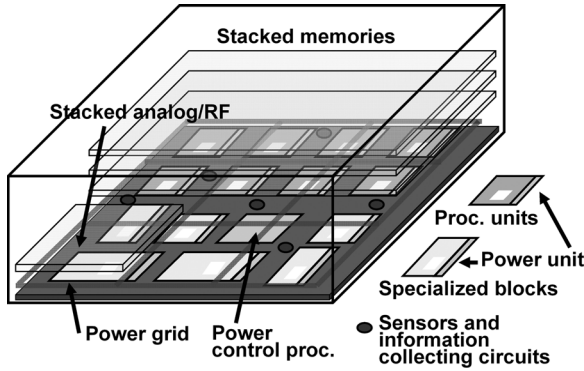


Fig. 2. Concept of distributed power supply system.

problems and the approach is not suitable for on-chip distributed power supplies where many inductors are required nearby.

On the other hand, 50% efficiency without zero voltage switching (ZVS) and 65% with two-stage ZVS, at a switching frequency of 45 MHz with a voltage conversion ratio of 0.64, have been demonstrated in 0.18- μm SiGe process with on-chip integrated output filter [3]. In this implementation, the output filter is costly because it consumes large silicon area in a precious scaled process. Moreover, in this specific implementation, metal thickness is chosen to be 10 μm , which is again costly and which is not usually available.

It is reported that 80% effective efficiency with ZVS implemented with an on-chip integrated output filter was achieved at a very high switching frequency of 3 GHz, with a voltage conversion ratio of 0.52 in 90-nm CMOS [4]. In this implementation, the high effective efficiency is achieved by using clock-tree charge-recycling. The raw efficiency of the converter itself is still 48%.

Therefore, other approaches to implement buck converters for distributed power supply systems are to be sought through focusing on cost issues and package friendliness.

II. BASIC CONCEPT OF STACKED-CHIP IMPLEMENTATION

In order to implement on-chip buck converters for distributed power supply systems, the two following conditions should be met. First, all elements of the converter must be integrated at least in a package. Second, the implementation cost per one voltage domain must be minimized while maintaining high power efficiency.

To maximize the power efficiency, the power loss must be minimized. The major components of power loss are classified into three parts: dynamic switching loss of the switching transistors, resistive loss of the switching transistors, and the resistive loss of the inductor. The total power loss is minimized under the condition that the previous three parts are equal and is given by the following expressions [5]:

$$P_{\text{loss}} = V_{\text{in}} I_L \sqrt[3]{24 \frac{R_0 C_0}{\tau_L} D(1-D)} \propto \sqrt[3]{\frac{R_0 C_0}{\tau_L}} \quad (1)$$

where

$$R_0 C_0 = \left(\sqrt{D R_P C_P} + \sqrt{(1-D) R_N C_N} \right)^2 \quad (2)$$

$$\tau_L = \frac{L}{R_S}. \quad (3)$$

$D (= V_{\text{out}}/V_{\text{in}})$ is the duty cycle where V_{in} and V_{out} are the input and output voltages, which is not a design parameter but is given by the specification, I_L signifies the output current, R_P , R_N , C_P , and C_N denote effective conduction resistances and switched capacitances of pMOS (high-side) and nMOS (low-side) switching transistors, and L and R_S are the filter inductance and its parasitic series resistance. For planar inductors, the maximum τ_L is fixed and given by the technology. The thicker the metal layer is, the smaller the maximum τ_L is.

As seen from (1), smaller $R_0 C_0$ and larger τ_L are better for higher power efficiency. $R_0 C_0$ is shown to be roughly proportional to the product of effective conduction resistance R_T and effective switched capacitance C_{eff} per unit gate width of switching transistors. Here, C_{eff} is expressed as $1.3C_G + C_J$, where C_G and C_J indicate the gate and junction capacitance per unit width. As technology scales, R_T and C_{eff} scale as $1/k^{0.7}$ and $1/k$, where k denotes the scaling factor [6]. k doubles when the technology scales down by half. Therefore, it is better from the power-efficiency point of view to use the more advanced technology.

One may argue, however, that the maximum V_{in} can be lower in the case of transistors with the smallest linewidth. When V_{in} is higher than the maximum V_{DD} for a certain technology, the switching transistors must be cascaded to relax the voltage over-stress. If two transistors are cascaded, R_T increases by a factor of 1.2 and C_{eff} decreases by a factor of 0.4 [5]. As a result, even though we have to use a cascaded structure, $R_0 C_0$ decreases as technology scales. Thus, it can be said that it would be better to use the most scaled transistors for high conversion efficiency.

On the other hand, τ_L is mainly determined by the thickness of the metal wire, as described previously, and its dependence on process technology is small. Thus, the inductor is not necessarily fabricated by using the most advanced technology, which is expensive. In addition to the inductor, the fabrication cost of on-chip MOS capacitor per unit capacitance increases as technology scales. Thus, it is reasonable to implement active elements and output filter on a separate die whose process technologies are different. Fig. 3 shows the basic concept of the stacked-chip implementation of a buck converter. The lower chip fabricated in the advanced technology contains the controller and switching transistors of a buck converter and target circuits. The upper chip fabricated in conventional and cheap process technology contains LC filter elements such as L 's and C 's. By stacking two chips face to face and connecting them via metal bumps, a buck converter for on-chip distributed power supply systems can be fabricated in a well-balanced manner for best cost and power tradeoff.

III. TEST CHIP DESIGN

A. Circuit Topology

To demonstrate the feasibility of the stacked-chip buck converter, an on-chip buck converter is designed in 0.35- μm CMOS for upper and lower chips. The lower chip could be manufactured by 90 nm or more advanced technology for the higher efficiency, but this test chip is to show the feasibility of the stacked-chip approach. Fig. 4 shows the circuit diagram of the

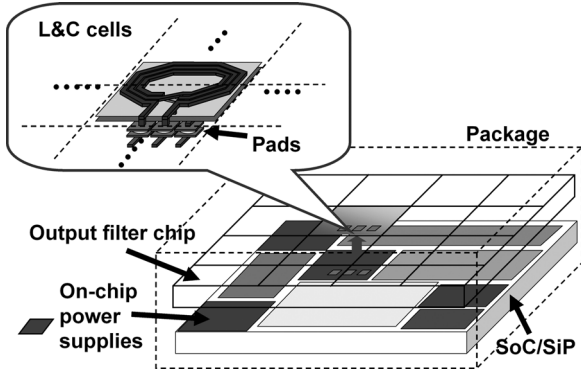


Fig. 3. Basic concept of stacked-chip implementation of on-chip buck converter.

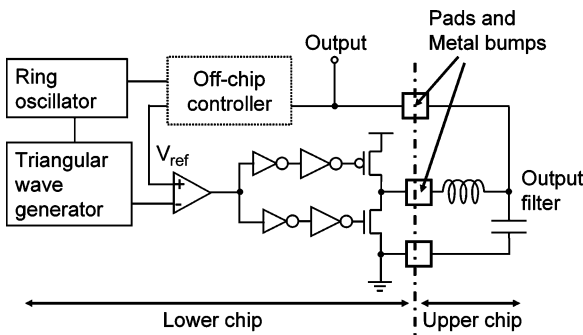


Fig. 4. Test circuit diagram of stacked-chip implementation of buck converter.

buck converter. Parameters are optimized for the power efficiency as described hereinbelow. Drivabilities of the tapered buffers are set high enough and the inverter sizes are calculated to minimize the on-on overlap time of switching transistors. The outer diameter of the filter equals that of the filter inductor d_{out} , which is set at $2 \times 2 \text{ mm}^2$ by assuming that a 10 mm^2 chip can have 25 voltage domains. A $6.8 \times 6.9 \text{ mm}^2$ chip with seven voltage domains has already been presented [7]. τ_L degrades as the outer diameter of the inductor shrinks, however, the power efficiency can be kept high because R_0C_0 decreases as technology scales. The inductance is estimated by a simple formula from [8]. Narrow metal-to-metal spacing and a wide metal wire are preferable in this application. τ_L is a function of the d_{in}/d_{out} ratio, which can be calculated using the inductance formula and the sheet resistance. The inductance and the parasitic resistance are roughly proportional to n^2 for a fixed d_{in}/d_{out} ratio, where n is the number of turns, considering that the space is negligibly narrow compared with the line width. The normalized τ_L curve in Fig. 5 is therefore independent of n . From the calculation result, d_{in} is decided to be about $0.5d_{out}$. Here, n is decided as 3 to maximize the power efficiency. As a result, the calculated inductance of this work is 22 nH when the sheet resistance is about $0.02 \Omega/\square$. The open space at the center of the inductor is filled with a MOS capacitor for the output filter. Area efficiency is more important than linearity for the filter capacitor, because the output voltage does not change dynamically in normal operation. From that aspect, the MOS capacitor is more suitable than any other types of on-chip capacitors like metal-insulator-metal

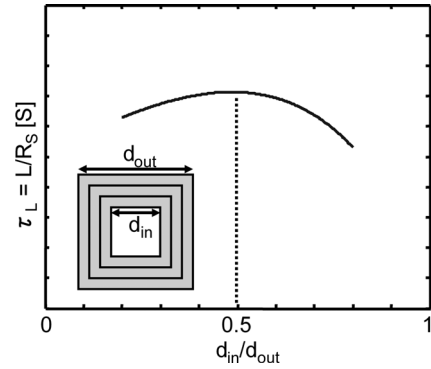


Fig. 5. τ_L dependence on d_{in}/d_{out} for square inductor.

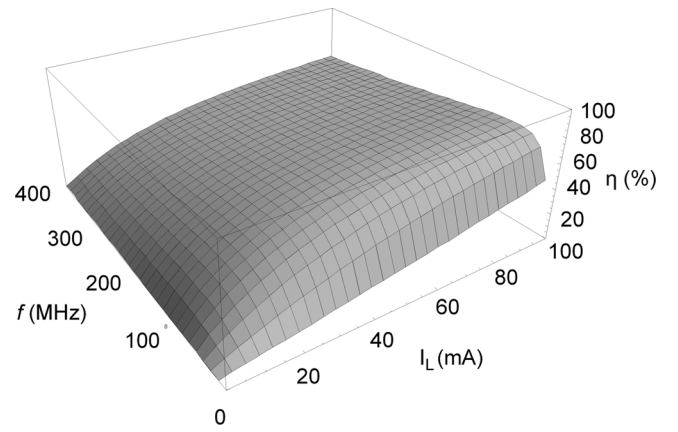


Fig. 6. Estimated power efficiency dependence on load current and switching frequency.

(MIM) capacitor or polysilicon capacitor. The obtained capacitance is about 1 nF. Under those conditions, the power efficiency dependence on the output current and the switching frequency for $V_{in} = 3.3 \text{ V}$ and $V_{out} = 2.3 \text{ V}$ is plotted in Fig. 6 by modifying the duty cycle definition in [11]. D is redefined in this study as follows to take the voltage drop caused by the filter inductor into account, when it is simply set as $D = V_{out}/V_{in}$ in [11]; by doing so, the estimation accuracy of several values is improved:

$$D = \frac{V_{out} + R_S I_L}{V_{in}}. \quad (4)$$

Here, I_L denotes the load current which equals the dc part of the inductor current.

The output voltage ripple ratio is described as follows when f_S and C denote switching frequency and output filter capacitance, respectively:

$$\frac{\Delta V_{out}}{V_{out}} = \frac{1 - D}{16LCf_S}. \quad (5)$$

It is impossible to choose a switching frequency under 100 MHz in this case because the output voltage ripple goes up above 10% for the chosen values. The gate width of the high-side and low-side transistors are designed to be 1000 and 500 μm , respectively, under the load current condition of 60 mA using the optimum gate-width formulas in [11].

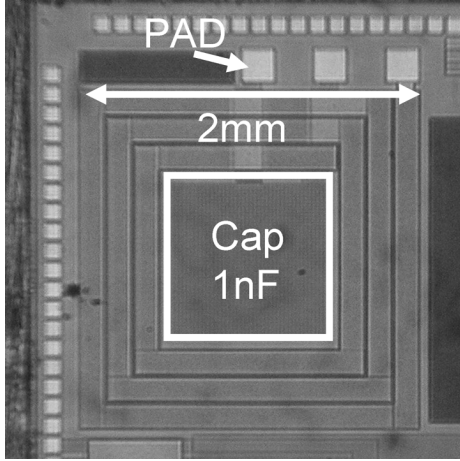


Fig. 7. Chip microphotograph of the output filter.

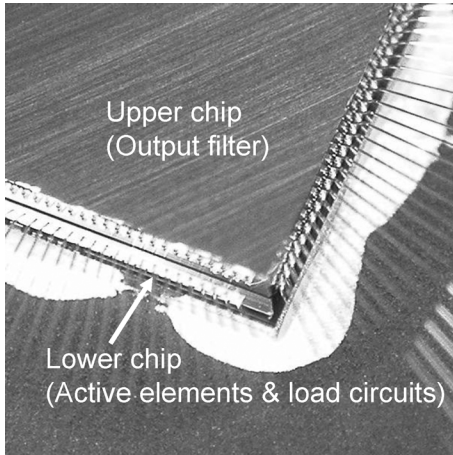


Fig. 8. Measurement setup of the test chip.

B. Simulation and Measurement Results

The test buck converter with the stacked-chip implementation was fabricated and measured. Fig. 7 shows the chip microphotograph of the output filter on the upper chip. Figs. 8 and 9 show the measurement setup and its cross-sectional diagram. The pad size and the effective bump diameter of this experimental setup are $200 \times 200 \mu\text{m}$ and $150 \mu\text{m}$, respectively. Micro bumps with diameter $30 \mu\text{m}$ and whose resistance is as low as $14 \text{ m}\Omega/\text{bump}$ have been realized in industry environments [14] and can be used instead for further smaller area. The output waveform in Fig. 10 shows $V_{\text{out}} = 1.86 \text{ V}$ at $I_L = 60 \text{ mA}$. The measured voltage ripple is smaller than $\pm 10\%$, which is comparable to the result of the more expensive solution in [2]. Fig. 11 shows the simulated and measured power efficiency with $V_{\text{out}} = 2.3 \text{ V}$ for an output current range from 20 to 70 mA. The maximum efficiency of 62% is achieved for 70 mA output current. The measurement results compare well with the HSPICE simulation results. The simulation considers all of the parasitic elements, including the inductor parasitic resistance of 2.5Ω and the inductor input-to-ground capacitance of 25 pF .

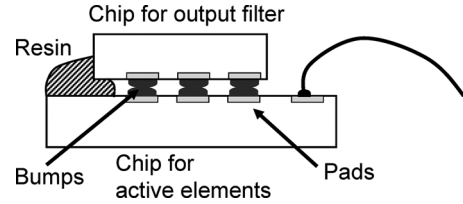
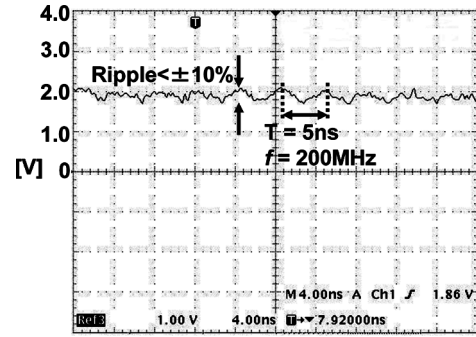
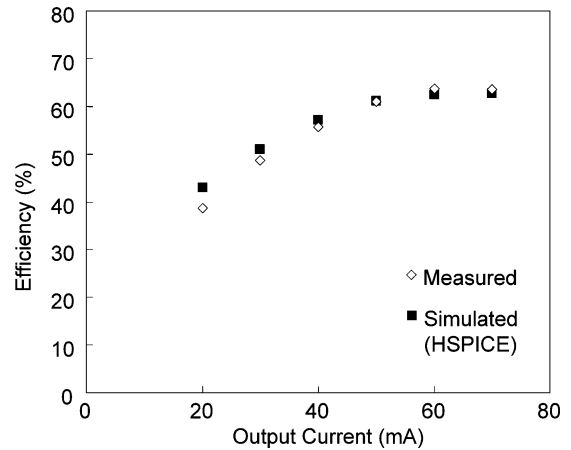


Fig. 9. Cross-sectional diagram of the measurement setup.

Fig. 10. Output voltage waveform for $V_{\text{out}} = 1.86 \text{ V}$ and $I_L = 60 \text{ mA}$.Fig. 11. Simulated and measured power efficiency for $V_{\text{out}} = 2.3 \text{ V}$ and $f = 200 \text{ MHz}$.

IV. IMPLEMENTING FILTER INDUCTOR ON GLASS EPOXY INTERPOSER

In order to further increase the efficiency, it is effective to use inductors whose τ_L is higher than that of the previous inductors. A thin-film inductor surrounded by magnetic core material as proposed in [15] can be a solution but is expensive. Implementing the inductor on a glass epoxy interposer as shown in Fig. 12 is an effective yet inexpensive solution. The thickness of the metal wire on an interposer is generally thicker than $10 \mu\text{m}$, and the inductor on the interposer shows a much lower resistance than that on a silicon chip, where the metal thickness is usually less than $1 \mu\text{m}$. A capacitor on the upper chip made with a conventional technology is connected to the lower chip manufactured by an advanced technology like 90 nm CMOS, through the through-hole vias in the interposer. By this implementation,

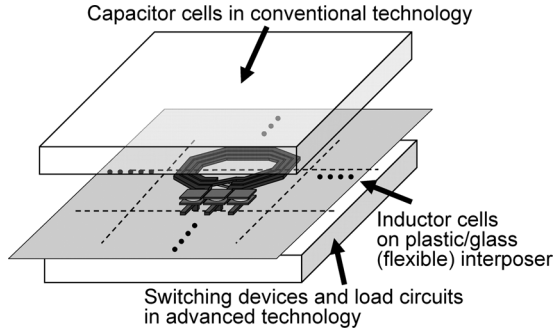


Fig. 12. Another stacked-chip implementation to gain high τ_L .

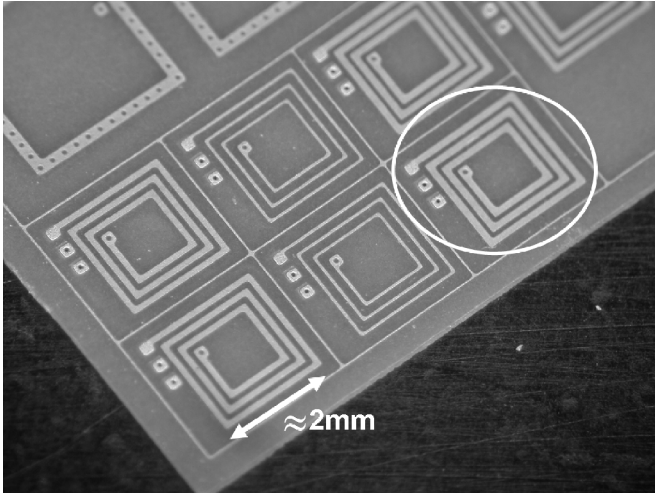


Fig. 13. Manufactured inductor array on glass epoxy interposer.

high efficiency and low cost are achieved at the same time. The maximum power efficiency is derived as follows from (1):

$$\begin{aligned} \eta &= \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \\ &= \frac{V_{\text{in}} D I_L}{V_{\text{in}} D I_L + V_{\text{in}} I_L \sqrt[3]{24 \frac{R_0 C_0}{\tau_L} D (1 - D)}} \\ &= \frac{1}{1 + \alpha \tau_L^{-1/3}}. \end{aligned} \quad (6)$$

Here, P_{out} indicates the output power. α is a function of $R_0 C_0$ and D and can be a constant when the process technology and D are fixed. Therefore, simply higher τ_L directly results in higher power efficiency.

The structure shown in Fig. 12 is assembled using a newly introduced interposer and the same lower and upper chips presented in Section III. In this implementation, only a capacitor is used on the upper chip. Fig. 13 shows an inductor array on generic Flame Resistant 4 (FR-4) glass epoxy interposer with two metal layers. The circled inductor in the array, which achieved the minimum metal spacing in the trial manufacture, is used for the measurement. The metal thickness on the interposer is $30 \mu\text{m}$, the substrate thickness is $100 \mu\text{m}$, and the diameter of the through-hole via is $100 \mu\text{m}$. This implementation increases τ_L by 30 times compared with the case of an on-chip inductor. The outer diameter of the inductor

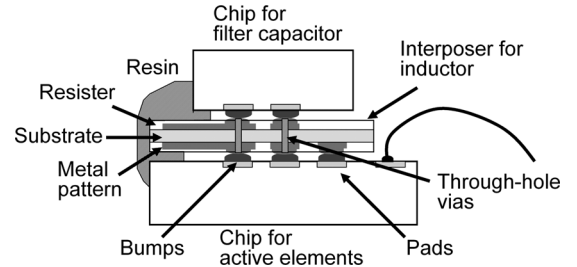


Fig. 14. Cross-sectional diagram of the measurement setup.

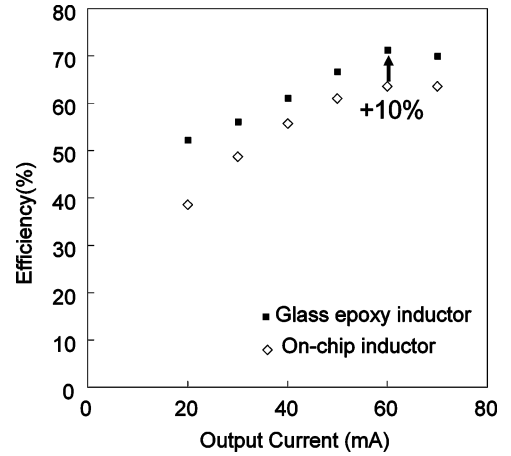


Fig. 15. Measured efficiency comparison between two types of implementations.

is increased by 10% to achieve the same value of on-chip filter inductance because the minimum spacing of metal lands on glass epoxy is larger than that of on-chip interconnects. The permittivity of the glass epoxy is generally more than four times higher than SiO_2 , however, the parasitic capacitance between both sides of the interposer can be negligible. This is because the substrate thickness is sufficiently large compared with the line width. Fig. 14 shows the cross section of the stacked chips. Fig. 15 shows the comparison of measured power efficiency between two types of implementations of “two chips” and “two chips + interposer” for $V_{\text{in}} = 3.3 \text{ V}$ and $V_{\text{out}} = 2.3 \text{ V}$. The power efficiency with the glass epoxy inductor is improved by 5%–14% depending on the output current compared with the on-chip implementation. The maximum power efficiency of 71.3% is achieved at an output current of 60 mA. The possible reason that the efficiency does not improve the most at 60 mA is that the switching transistors are not changed optimally according to the τ_L characteristic of the newly implemented inductor.

V. CONCLUSION

An on-chip buck converter with stacked-chip implementation that is suitable for low-cost low-power distributed power supply systems has been designed and fabricated for the first time. The switching frequency is optimized and chosen to be 200 MHz. A power efficiency of 62% is measured for an output current of 70 mA, which verifies the feasibility of this approach. By utilizing a glass epoxy interposer for a filter inductor, it is shown by experiment that the power efficiency can be increased to 71.3%.

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