Brief Papers

A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction

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Abstract—A reduced clock-swing flip-flop (RCSFF) is proposed, which is composed of a reduced swing clock driver and a special flip-flop which embodies the leak current cutoff mechanism. The RCSFF can reduce the clock system power of a VLSI down to one-third compared to the conventional flip-flop. This power improvement is achieved through the reduced clock swing down to 1 V. The area and the delay of the RCSFF can also be reduced by a factor of about 20% compared to the conventional flip-flop. The RCSFF can also reduce the RC delay of a long RC interconnect to one-half.

Index Terms—Differential circuit, flip-flops, leak current, low-power CMOS circuit, low-voltage CMOS circuit, RC bus, RC delay, RC interconnect.

I. INTRODUCTION

FOUR pie charts in Fig. 1 show power distributions in various very large scale integrations (VLSI's). As seen from the charts, the power distribution of VLSI's differs from product to product. However, it is interesting to note that a clock system and a logic part itself consume almost the same power in various chips, and the clock system consumes 20–45% of the total chip power. In this clock system power, 90% is consumed by the flip-flops themselves and the last branches of the clock distribution network which directly drives the flip-flops [1].

One of the reasons for this large power consumption of the clock system is that the transition probability of the clock is 100% while that of the ordinary logic is about one-third on average. Consequently, in order to achieve low-power designs, it is important to reduce the clock system power. In order to reduce the clock system power, it is effective to reduce a clock voltage swing. This is because the power consumption of the clock system is proportional either to the clock swing or to the square of the clock swing, depending on the circuit configuration, which is described later.

One idea to reduce the clock voltage swing was pursued in [2], but it required four clock lines, which will increase clock interconnection capacitance. Moreover, routing four clock lines is disadvantageous in area, and the skew adjustment is difficult.

This paper describes a new small-swing clocking scheme which requires only one reduced swing clock line. The RCSFF
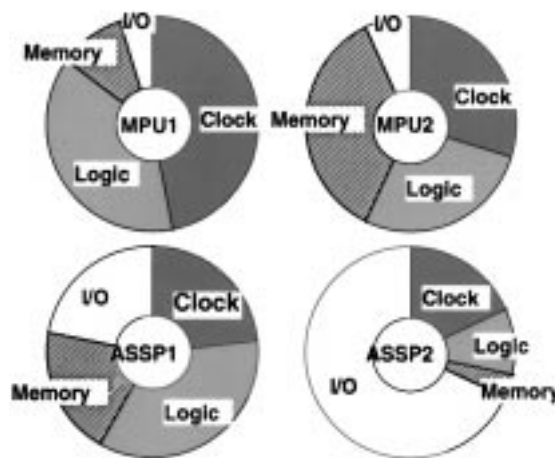
Fig. 1. Power distribution in various VLSI's.

is also beneficial to decrease the capacitance of a clock system by reducing the number of MOSFET's connected to the clock distribution network.

II. REDUCED CLOCK-SWING FLIP-FLOP

Reduced clock-swing flip-flop (RCSFF) is proposed to lower the voltage swing of the clock system. Fig. 2 shows schematic diagrams of the conventional flip-flop and the proposed RCSFF. With the conventional flip-flop, the clock swing cannot be reduced because ϕ and $\overline{\phi}$ are required, and overhead becomes imminent if two clock lines ϕ and $\overline{\phi}$ are to be distributed. On the other hand, if only ϕ is distributed, most of the clock-related MOSFET's operate at full swing, and only minor power improvement is expected.

The RCSFF is composed of a true single-phase master-latch and a cross-coupled NAND slave-latch. The master-latch is a current-latch-type sense-amplifier. The salient feature of the RCSFF is that it can accept a reduced voltage swing due to the single-phase nature of the flip-flop. The voltage swing, V_{Clock}, can be as low as 1 V.

While the MOSFET count of the conventional flip-flop is 24, that of the RCSFF is 20 including an inverter for generating $\overline{D}$. The number of MOSFET's that are related to a clock is also as small as 3, which should be compared to 12, in the conventional flip-flop. Since only three MOSFET's, $P1$, $P2$, and $N1$, are clocked, the capacitance of a clock network can be reduced with the RCSFF, which in turn decreases the power.

The clock swing can be reduced with the RCSFF, but the issue is that when a clock is "high" at the voltage of V_{Clock}, $P1$
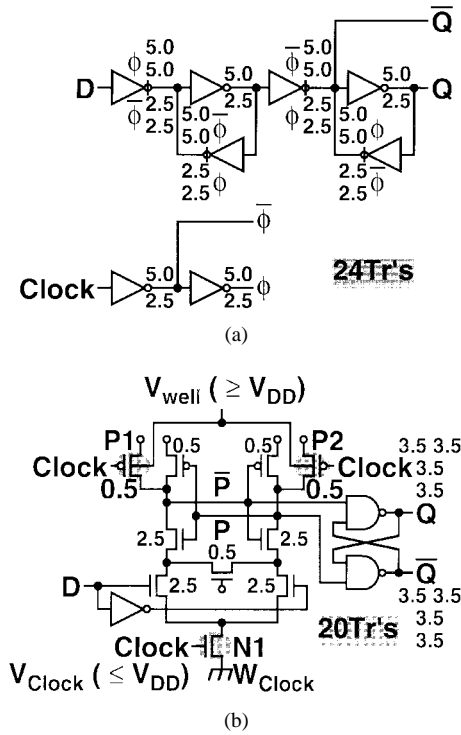
(a)

(b)

Fig. 2. Schematic diagram of (a) the conventional flip-flop and (b) the RCSFF. Numbers in the figure signify MOSFET gate width in microns. Gate length is 0.5 μm for all MOSFET's. W_{Clock} is the gate width of $N1$.

and $P2$ do not switch off completely, leaving leakage current flow through either $P1$ or $P2$. The RCSFF, however, has a leak current cutoff mechanism. By applying backgate bias, V_{well}, to the precharge MOSFET's, $P1$ and $P2$, the threshold voltage of $P1$ and $P2$ can be increased. Then the leakage current can be completely cut off. Although it will be shown afterwards that even without the backgate bias the power can be reduced, the further power improvement is possible by cutting off the leak current. The other way to increase the V_{th} of $P1$ and $P2$ is by an ion-implant, which needs process modification and is usually prohibitive. Thus, this case has not been considered in this paper, but it is one technically promising way if additional ion-implant is allowed. When the clock should be stopped in a standby mode, it should be stopped at V_{SS}. Then there is no leak current even without the backgate bias.

III. REDUCED SWING CLOCK DRIVERS

The RCSFF has a reduced swing clock driver. There are basically two types of clock drivers shown in Fig. 3—type A and type B. In type A, the clock swing, $V_{\text{Clock}} = V_{\text{DD}} - n \cdot V_{th}$ depending on the number of inserted MOSFET's. The power consumption associated with the clock distribution is proportional to V_{Clock} in this case. Type A drivers do not require either dc–dc converters or external voltage supplies, so they are easily implemented.

In type B, on the other hand, V_{Clock} is generated and supplied either from an on-chip dc–dc converter or from an external voltage supply. The power consumption is proportional to the square of V_{Clock}. Thus, it is more efficient than type
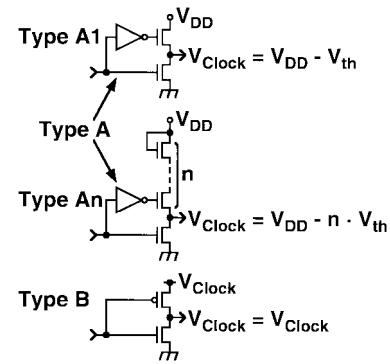

Fig. 3. Types of reduced swing clock drivers. type $A1$ and type An are grouped as type A. In type B, V_{Clock} is supplied externally.
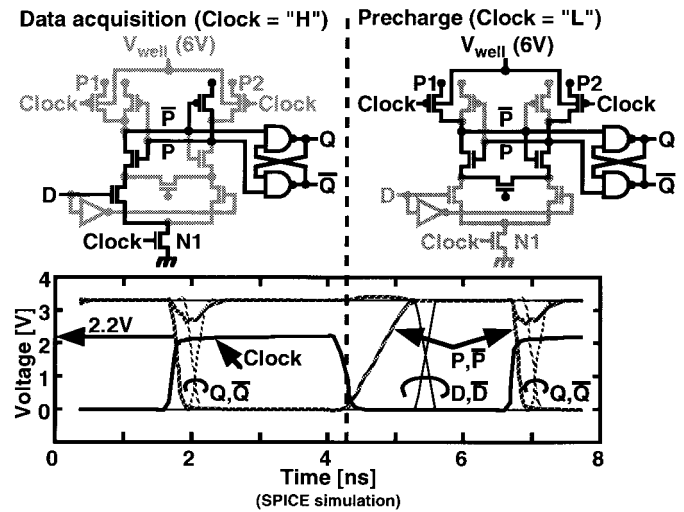

Fig. 4. Operation waveforms of the RCSFF.

A drivers, but more difficult to implement and needs V_{Clock} supply lines to each clock driver.

IV. OPERATION OF RCSFF

Fig. 4 shows the typical behavior of the RCSFF with the type $A1$ driver simulated by SPICE. The left half of the figure is for a data acquisition phase, and the right half shows a precharge phase. It can be seen that the clock goes up only to 2.2 V.

In the figure, the data input D is assumed to be "high" when the clock is asserted. The solid line path turns on and the node $\overline{P}$ goes down to "low" while P remains "high." P and $\overline{P}$ drive a low-active RS flip-flop and an output Q becomes "high." In the precharge phase, MOSFET $P1$ and $P2$ precharge nodes P and $\overline{P}$ to "high." The output Q and $\overline{Q}$ keep the previous state because both P and $\overline{P}$ are "high." The threshold voltage of MOSFET's is 0.6 V, but with the well bias V_{well} of 6 V, the threshold voltage of $P1$ and $P2$ becomes 1.4 V, which is high enough to cut off the leakage path with 2.2 V clock swing.

The RCSFF behaves as an edge-triggered flip-flop because when the clock goes to "high", P and $\overline{P}$ are determined dependent on the input D, and once the data are latched, the change of the input D does not affect P and $\overline{P}$ status thanks to the cross-coupled inverters.

(a)

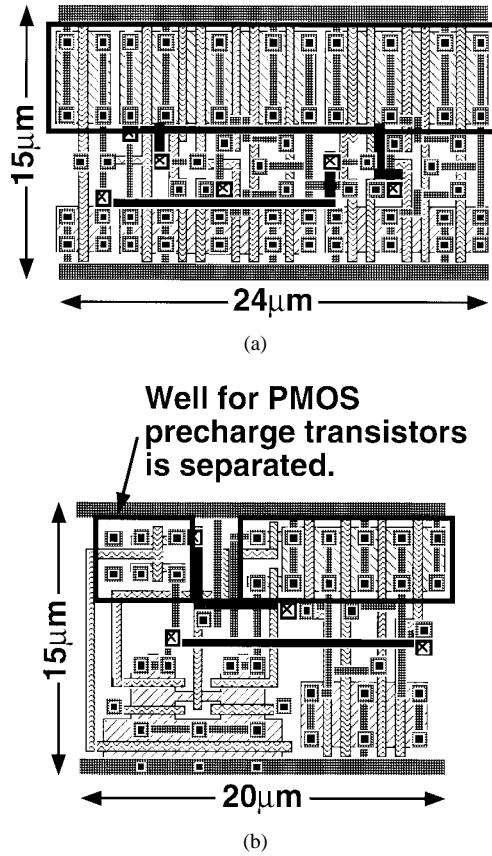**Well for PMOS precharge transistors is separated.**

(b)

Fig. 5. Layout of (a) the conventional flip-flop and (b) the RCSFF. W_{Clock} is assumed to be 10 μm and the other value is the same as in Fig. 2.

Let us consider the sizes of MOSFET's here. Numbers in Fig. 2 signify gate width in microns. The nodes P and $\overline{P}$ can be precharged slowly while the clock is "low." Therefore, the size of the precharge PMOSFET's, $P1$ and $P2$, can be minimum—0.5 μm in this case. The width of $N1$ should be large for a faster Clock-to-Q operation. There is a tradeoff between speed and power in choosing the optimum width for $N1$.

V. PERFORMANCE COMPARISON

A. Area

Fig. 5(a) is a layout example of the conventional flip-flop, and Fig. 5(b) is the RCSFF case. The well for the precharge PMOSFET's, $P1$ and $P2$, is separated from the normal well for applying the backgate bias. Nevertheless, the area can be reduced by a factor of about 20% compared to the conventional flip-flop. In reality, however, the extra bias lines are needed for the RCSFF case, and this 20% reduction is cancelled out by the bias line overhead. If V_{th} of $P1$ and $P2$ was adjusted by ion-implant, the 20% area reduction could be enjoyed.

B. Delay

A SPICE analysis is carried out assuming typical parameters of a generic 0.5-μm double metal CMOS process. The rise time of V_{Clock} is assumed to be 0.2 ns in the simulations; but even if the rise time is changed from 0.2 to 0.6 ns, the
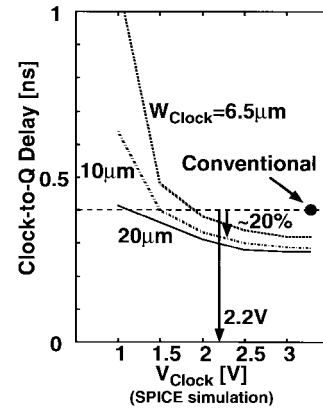

Fig. 6. Clock-to-Q delay characteristic of the RCSFF simulated by SPICE. The delay depends on V_{Clock} but is not affected by V_{well}. The supply voltage is 3.3 V.
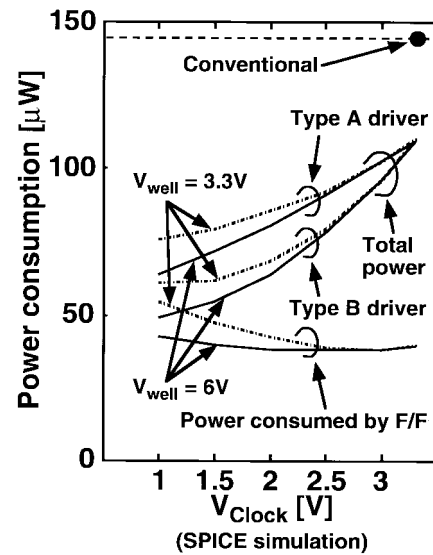

Fig. 7. Power consumption characteristic of the RCSFF simulated by SPICE.

change in Clock-to-Q delay is less than 0.04 ns. Fig. 6 shows Clock-to-Q delay characteristics of RCSFF where the gate width of $N1$, W_{Clock}, is varied as a parameter. Since delay improvement is saturated with W_{Clock} being 10 μm, this value of W_{Clock} is used in the area and power estimation. When V_{Clock} of 2.2 V (type A1 driver) and W_{Clock} of 10 μm are used, the RCSFF is improved by a factor of about 20% over the conventional flip-flops.

Data setup time and hold time in reference to clock are 0.04 and 0 ns, respectively, being independent of V_{Clock}, compared to 0.1 and 0 ns for the conventional flip-flop.

C. Power

Fig. 7 shows power characteristics of the RCSFF. The clock interconnection length is assumed to be 200 μm and transition probability of data is assumed to be 30%. The clock frequency f_{Clock} is assumed to be 100 MHz. These are typical values for low-power processors.

Power consumption per flip-flop is a sum of a clock driver, a flip-flop itself, and interconnection between them. Power

TABLE I
PERFORMANCE COMPARISON

	Driver	V_{Clock} [V]	Power	Delay	Area
Conventional		3.3	100%	100%	100%
RCSFF	**Type A1**	2.2	59%	82%	83%
V_{well} = 6V	**Type A2**	1.3	48%	123%	83%
W_{Clock} = 10μm	**Type B**	2.2	48%	82%	83%
f_{Clock} = 100MHZ	**Type B**	1.3	37%	123%	83%

Fig. 8. An application of the RCSFF to a long RC bus.

Fig. 9. Behavior of the differential RC bus.

Fig. 10. Normalized energy consumption by distributed RC line if the terminal voltage V_2 is reduced.

Fig. 11. Delay improvement of long RC bus. Length of the RC bus is assumed to 10 mm and width is assumed to 0.5 μm. W_{Clock} is 10 μm and a type $A1$ driver is used.
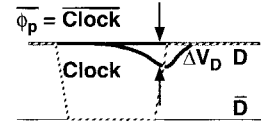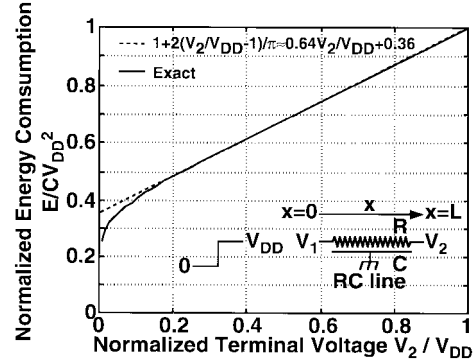
consumption gets smaller as V_{Clock} is decreased. As seen from the figure, with type A drivers, power reduction is less efficient than type B drivers. V_{well} is set to either 3.3 or 6 V. Without the backgate bias to $P1$ and $P2$, that is, in the case that V_{well} is 3.3 V, the power improvement is saturated around V_{Clock} of 1.5 V because the leak current increases as V_{Clock} lowers. On the other hand, in the case that V_{well} is 6 V, improvement in power is not saturated even at V_{Clock} of 1 V. In the best case considered, the power of the clock system can be decreased to one-third of the conventional flip-flops. In Fig. 7, the power consumption by the flip-flop itself is also shown. The slight increase in the power consumption of the flip-flop in the low V_{Clock} region is due to the leakage current through the PMOSFET $P1$ or $P2$ for precharge.

Table I summarizes a performance comparison. When the type $A1$ driver, which is easy to implement, is used, the power is reduced to 59% and the Clock-to-Q delay is reduced to 82%. If a dc–dc converter and a type B driver is used, the power consumption can be reduced to 37%, that is, 63% power saving even if the delay increases by 23%. Considering the improvement level and the delay increase, this type $A1$ driver case and this type B driver case can be practical choices.

VI. APPLICATION TO REDUCED SWING BUS

In Fig. 8, an application of the RCSFF to a long RC bus is considered. Since the RCSFF is a differential amplifier in nature, it can be used to amplify a small voltage signal on a differential RC bus, and at the same time it can latch the data.

Behavior of a differential RC bus is shown in Fig. 9. The differential bus is first precharged to V_{DD}, and then, when the voltage difference of D and $\overline{D}$ reaches ΔV_D, the clock is asserted and the amplifier is activated. Since ΔV_D can be as small as less than 1 V, delay reduction of the long RC bus can be achieved. Furthermore, power reduction of logic system can also be realized because D and $\overline{D}$ do not need to be in full swing. Let us consider what amount of power gain is
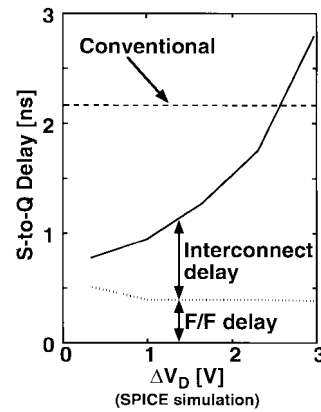
observed when a distributed RC line is driven in full swing at one end and switched off when the other terminal becomes V_2:

$$\frac{V(x,t)}{V_{DD}} = 1 + \frac{2}{\pi} \sum_{k=1}^{\infty} \frac{(-1)^k}{k-\frac{1}{2}} \cos\left[\left(k-\frac{1}{2}\right)\pi\left(1-\frac{x}{L}\right)\right]$$
$$\cdot e^{-(k-1/2)^2 \pi^2 (t/RC)}$$

$$Q = \int_0^L CV(x,t)\,dx$$
$$= CV_{DD}\left[1 - \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{1}{\left(k-\frac{1}{2}\right)^2\pi^2}\right.$$
$$\left.\cdot e^{-(k-1/2)^2\pi^2(t/RC)}\right].$$

Fig. 10 shows the normalized energy consumption $E(= QV_{DD})$ by the RC line. If the energy per cycle, $E(= QV_{DD})$, is expressed in terms of the terminal voltage, $V_2[= V(L,t)]$, $E \approx 0.36 + 0.64V_2$. This means that about 50%

power saving is possible if an RC interconnect is driven when the voltage swing of V_2 is 0.2V_{DD}.

Fig. 11 shows the delay dependence of the long RC bus with the RCSFF. The delay is dependent on ΔV_D. Faster operation is possible as ΔV_D is decreased. Compared to the conventional flip-flop, acceleration by a factor of more than two is possible.

VII. CONCLUSION

The RCSFF, which is compatible with the conventional process, is proposed to save up to 63% of the clock system power. With the RCSFF, area can be reduced to 80%, delay can be decreased to 80%, and the power is reduced to one-third of the conventional flip-flop. Leakage current through precharge MOSFET's can be eliminated by backgate bias. As an application of the RCSFF, RC buses are considered. RC delay and power consumed by the interconnect can be reduced to less than one-half compared to the case where the conventional flip-flops are used.

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