A 3-D-Stack Organic Sheet-Type Scanner with Double-Wordline and Double-Bitline Structure

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***Abstract*—This paper describes a sheet-type scanner and its circuits. The three-dimensional-stacked sheets comprise of two organic-transistor sheets and one organic-photodiode sheet, which enable double-wordline and double-bitline structure. The operation was compared with the conventional single-wordline and single-bitline scheme, and confirmed by measurement. The double-wordline and double-bitline structure reduces the line delay and power by a factor of five and seven, respectively. A new dynamic decoder reduces active leakage current, to which the cut-and-paste customization can be applied.**

***Index Terms*—Area sensor, cut-and-paste customization, double bitline, double wordline, dynamic circuit, organic photodiode, organic transistor, sheet-type scanner.**

I. Introduction

BY USING organic field-effect transistors (OFETs), large-area circuits can be made on a plastic film [1]–[3]. Thanks to the plastic substrate, the organic circuits are mechanically flexible. Besides, fabrication cost of the organic circuits will be as inexpensive as $\$2/\text{in}^2$ even in a full-color flexible display [4] with printing technologies [5]–[9] and roll-to-roll processing [10], which means that low cost per area will be expected in future. These features are also attractive and suitable for a large-area sensor application including the electronic artificial skin (e-skin) [2], which can complement small-area but expensive silicon integrated circuits. However, speed of the organic circuits is slow since the carrier mobility is about 1 $\text{cm}^2/\text{V}\cdot\text{s}$ that is three orders of magnitude lower than that of silicon. Furthermore, the circuit delay quadratically worsens as the sensor area increases.

Recent advancement in the organic large-area sensor is the integration of an OFET and an organic photodiode (OPD) to achieve a sheet-type scanner [3]. In order to improve speed and make the scanner practical, in this paper, we newly implement a double-wordline and double-bitline structure to the scanner. The structure can be applied not only to the scanner but also to other organic large-area sensor, and save power as well as the circuit delay. This paper describes the circuits of the sheet-type scanner, and demonstrates the advantages of the double wordline and double bitline taking the scanner as an example.

The device structure and operation principle of the sheet-type scanner is mentioned in the next section. Section III describes the circuit design of the peripheral circuits including a new decoder, photocurrent-integration scheme, and three-dimensional (3-D)-stack integration that enables the double-wordline and double-bitline structure. The results and future direction follow in Section IV and V, respectively. Finally, the summary of this paper is mentioned in Section VI.

II. Device Structure and Operation Principle

Fig. 1(b) illustrates the cross section of the sheet-type scanner. The two OFET sheets and one OPD sheet are separately fabricated and glued together with silver paste. All base films are transparent polyethylene naphthalate (PEN) that is a kind of plastic and its thickness is 125 μm each, through which light can pass. The aperture (open-area ratio) is 45% of a total pixel area as shown in Fig. 1(a). The light reflects on the surface of the paper under scan to the OPDs. Black and white are discriminated by difference in reflectance, which in turn modulates the photocurrent of the OPD. That is, in the black part, the light does not reflect very much while in the white part, the light reflects to the OFETs. Thus, the sheet-type scanner can capture a black-and-white image on a paper without heavy mechanical components or optical lens.

The OFET structure is called the top-contact geometry and similar to an upside-down silicon MOSFET. On the PEN base film, gold (Au) is deposited as a gate electrode through a metal mask. 630-nm-thick polyimide (PI) is a gate dielectric, which is spin coated and cured at 180 °C. This means low-temperature processing without the plastic film damaged. 50-nm-thick pentacene is a p-type organic semiconductor and channel layer that is deposited by vacuum sublimation. Source and drain electrodes are Au as well as the gate electrode. The minimum channel length is 40 μm. The polymonochloro–paraxylylene (parylene) passivation is made on the OFET *in situ* so as not to be exposed to the air. Parylene protects the OFETs from oxygen and humidity that deteriorate organic devices, and thus it is very useful to enhance durability and reliability of the organic devices. On the parylene passivation and bottom of the

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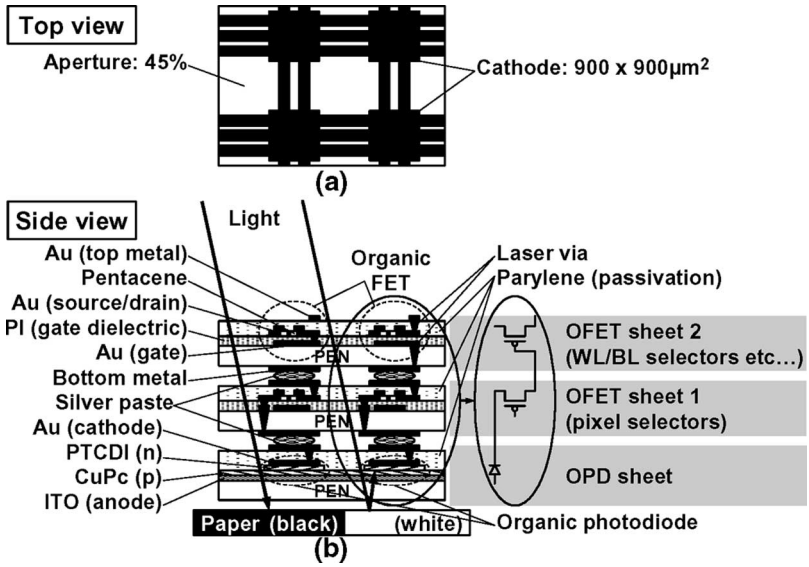

Fig. 1. Device structure. (a) Top view and (b) cross section.

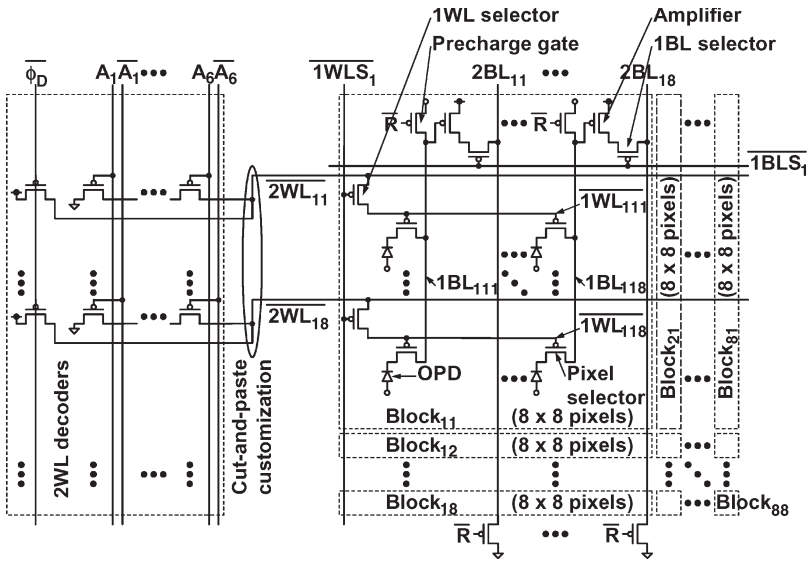

Fig. 2. Double-wordline and double-bitline structure.

PEN base film, there are top and bottom metals, respectively, for interconnections and connectivity to another OFET sheet. If connections through the PEN base film, PI gate dielectric, or parylene passivation is necessary, a CO_2 laser selectively drills a via-hole. This fabrication process is described in [11] and [12] in detail.

Only the p-channel OFETs are used since mobility of an n-channel OFET ever reported is 0.1 $cm^2/V \cdot s$ at best, which is an order of magnitude smaller than that of pentacene. To make matters worse, n-channel materials are much more sensitive to oxygen and humidity, and they deteriorate in a shorter time in the atmosphere.

The OPDs are the basis of the scanner. As a common anode of the OPDs, transparent indium tin oxide (ITO) covers the PEN base film. Copper phthalocyanine (CuPc) is a p-type semiconductor and 3,4,9,10-perylene tetracarboxylic diimide (PTCDI) is n-type one, forming the OPD [13], [14]. As a cathode, Au is deposited onto the OPD. Parylene passivates the OPDs as well as the case of OFET. Additional top metals on the parylene passivation are for connectivity to the OFET sheet 1.

Since the reflection type of operation is adopted as a principle, the direct incident light must be blocked. Otherwise, all pixels become white. The cathode acts as a shield against the direct incident light, which size is 900×900 μm^2 as shown in Fig. 1(a). Only over the cathodes, all OFETs are placed.

The circled structure in Fig. 1(b) corresponds to the right-side circuit schematic, including an OPD, pixel selector, and peripheral OFETs. We discuss the circuit design in the next section.

III. Circuit Design and 3-D-Stack Integration

Fig. 2 shows the circuit schematic of the proposed double-wordline and double-bitline structure in the sheet-type scanner. The supply voltage of the circuit (V_{DD}) is 40 V. An array of

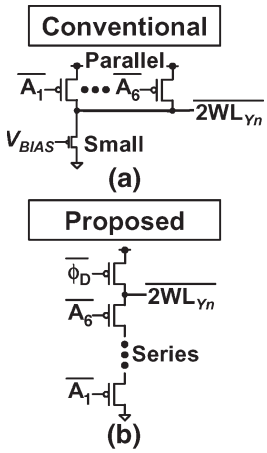

Fig. 3. (a) Conventional and (b) proposed decoders.

64×64 pixels is divided into 8×8 blocks so that each block has 8×8 pixels. Every pixel has an OPD and pixel selector.

A first wordline (1WL) connects to a second wordline (2WL) through a first-wordline selector (1WL selector). A 1WL activates the gates of the pixel selectors to specify a local row address. A 1WL selector selects a 1WL with a first-wordline select signal ($\overline{1\mathrm{WLS}_X}$). A second-wordline decoder (2WL decoder) drives a 2WL, which is mentioned afterward.

The similar notations are used for bitlines. A first bitline (1BL) is a local bitline in a block. A precharge gate precharges a 1BL with the precharge signal ($\overline{\mathrm{R}}$), and this signal predischarges a second bitline (2BL) too before readout operation. An amplifier amplifies a first-bitline voltage. A first-bitline selector (1BL selector) selectively transfers the amplified voltage to a 2BL with a first-bitline select signal ($\overline{1\mathrm{BLS}_X}$). Concerning the readout operation, we adopted a photocurrent-integration scheme, which is described in Section III-C.

A. Decoder and Cut-and-Paste Customization

Fig. 3(a) shows the conventional static decoder used in the e-skin, in which switching OFETs are connected in parallel. The load transistor must be small due to the normally on load, and thus its sizing is required, which results in slow fall time in the output. In addition, bias-voltage adjustment is necessary. A microampere-order active leakage current flows because of the bias voltage (V_{BIAS}) when the output is "H," and unfortunately all but one decoders output "H."

On the other hand, the proposed decoder in Fig. 3(b) does not draw an active leakage current thanks to the dynamic operation. The switching OFETs are connected in series. This decoder is a ratioless circuit without the precharge OFET sized, and thus more tolerant of process, threshold-voltage, and supply-voltage variation/fluctuation than the conventional ratio-type one.

We devised the layout of the proposed decoder so that we can make the cut-and-paste customization [2]. Assume that we now want a one-out-of-eight decoder and need only three switching OFETs, but we have prepared six switching OFETs in advance as shown in Fig. 4(a). This does not matter, and we just cut three switching OFETs out of the prefabricated circuit. Then, we paste them to a 2WL pad as shown in Fig. 4(b). This cut-and-paste customization makes the circuit scalable, and reduces

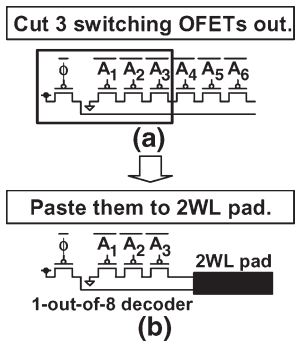

Fig. 4. Cut-and-paste customization. (a) Cut and (b) paste.

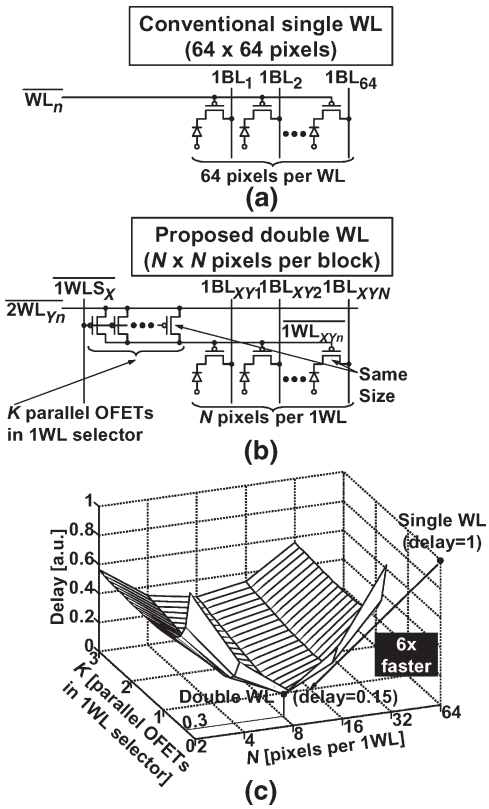

Fig. 5. (a) Single-wordline scheme and (b) double-wordline structure. (c) Simulated wordline delay.

a mask cost and nonrecurring engineering cost as well as design turnaround time because we do not need to design or make new masks for various sizes.

B. Wordline-Delay Optimization

Fig. 5(a) is the conventional single-wordline scheme while Fig. 5(b) is the proposed double-wordline structure. Fig. 5(c) shows the simulated wordline delay in the proposed structure. In the simulation, we assume that the OFET sizes of the pixel selector and 1WL selector are same, and K is the number of parallel OFETs in a 1WL selector driving a 1WL. N is the number of pixels per 1WL. The point of $K = 0$ and $N = 64$ corresponds to the conventional scheme while in the proposed structure, the wordline delay can reduce to 1/6 when $K = 0.3$ and $N = 8$. In the double-wordline structure, delay is optimized when N is about the square root of the total number of columns

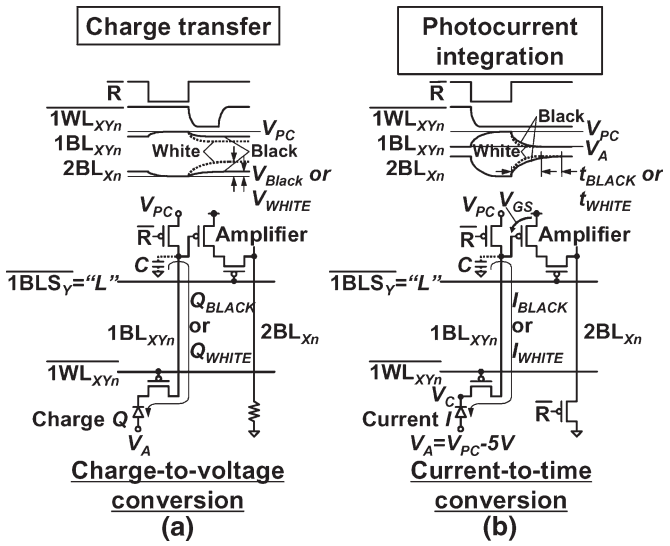

Fig. 6. (a) Photocharge-transfer and (b) photocurrent-integration schemes.

for most cases. When N is large, delay in 1WL becomes large. Alternatively, when N is small, delay of $\overline{\text{1WLS}_X}$ becomes large. Consequently, N has an optimal value, at which the delay is minimized.

The double-wordline structure potentially reduces dynamic power by the same factor as well as the delay since circuits operate on a block-by-block basis, where capacitance associated with the operation is lower than the single-wordline scheme. In particular, this will becomes important when random access is employed for intelligent image capturing in future.

C. Photocurrent-Integration Scheme

In a double-bitline structure in a silicon imager, a charge-transfer scheme illustrated in Fig. 6(a) is exploited to amplify a small charge induced by a silicon photodiode. First, a 1BL is precharged to the precharge voltage ($V_{\rm PC}$) with the precharge signal ($\overline{\rm R}$). Then, after one of the 1WLs is pulsed, a negative charge, $Q_{\rm BLACK}$ or $Q_{\rm WHITE}$, is transferred to a first-bitline capacitance (C) when a corresponding part is black or white. The first-bitline voltage is dropped from $V_{\rm PC}$ to a certain voltage by the negative charge. An amplifier amplifies the static voltage of the 1BL and outputs a static second-bitline voltage. This charge transfer scheme, however, cannot be realized in the organic circuit since a gate capacitance of an OFET is huge. Instead, we applied a photocurrent-integration scheme in Fig. 6(b) to the scanner.

The circuit topology in this scheme is almost same as the charge-transfer scheme, but operation is different. In order to evaluate a photocurrent of an OPD, one of the 1WLs keeps to be activated. The photocurrent $I_{\rm BLACK}$ or $I_{\rm WHITE}$ discharges C and the first-bitline voltage starts decreasing to the anode voltage of an OPD ($V_{\rm A}$). The fall time of the first-bitline voltage depends on the photocurrent integration. An amplifier amplifies the first-bitline voltage and starts to pull up a second-bitline voltage to $V_{\rm DD}$. Since the rise times of the second-bitline voltage $t_{\rm BLACK}$ and $t_{\rm WHITE}$ separately depends on $I_{\rm BLACK}$ and $I_{\rm WHITE}$, we can know if a pixel is either black or white.

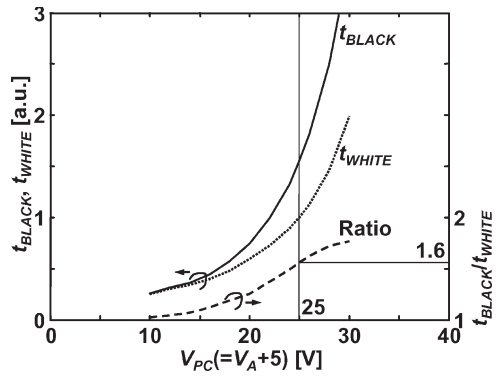

Fig. 7. Simulated rise times of second-bitline voltage when black and white, and ratio of them.

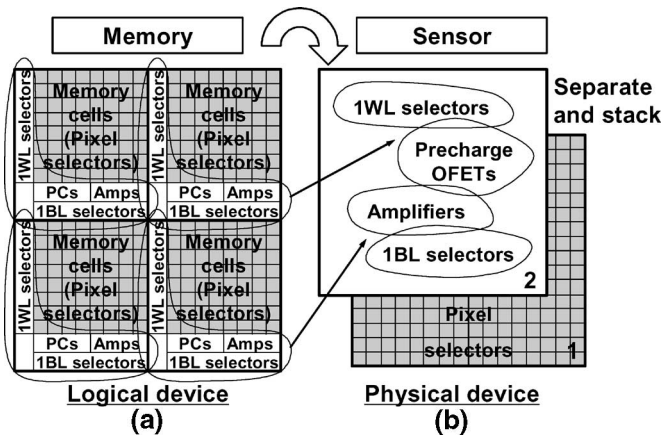

Fig. 8. (a) Memory and (b) sensor designs.

$t_{\rm BLACK}$ and $t_{\rm WHITE}$ are a function of $V_{\rm PC}$, and we simulated them as shown in Fig. 7. They are defined as a time from the $\overline{\rm R}$ negate to when the second-bitline voltage crosses 30 V. In the circuit simulation, a level-1 SPICE MOS model is used as device parameters [2]. $V_{\rm A}$ is restricted to $V_{\rm PC} - 5$ V, which means that a voltage across an OPD is 5 V at most. This voltage is sufficient to avoid the Zener breakdown of the OPD. $t_{\rm BLACK}$ and $t_{\rm WHITE}$ become faster as $V_{\rm PC}$ decreases since a gate bias of an amplifier ($V_{\rm GS}$) is larger. However, the $t_{\rm BLACK}/t_{\rm WHITE}$ ratio that is a kind of a dynamic range turns out to be smaller. We chose 25 V as $V_{\rm PC}$ in the circuit design, at which the $t_{\rm BLACK}/t_{\rm WHITE}$ ratio is 1.6.

D. 3-D-Stack Integration

Although the double-wordline and double-bitline structure finds wide use in memory design [15], [16], a situation and constraints are different in sensor applications. In a memory design, for instance, 1WL selectors and 1BL selectors are laid out on the side of the memory cells, and sense amplifiers are put at the bottom of the memory cells as shown in Fig. 8(a). This does not matter since a memory is a logical device. Logically, any location is all right for memory cells and their peripheral circuits.

On the contrary, a scanner is a physical device, and pixel positions are meaningful. We must arrange uniform distribution of pixels. If we place the peripheral circuits in arbitrary positions, the pixel density becomes irregular and uniform

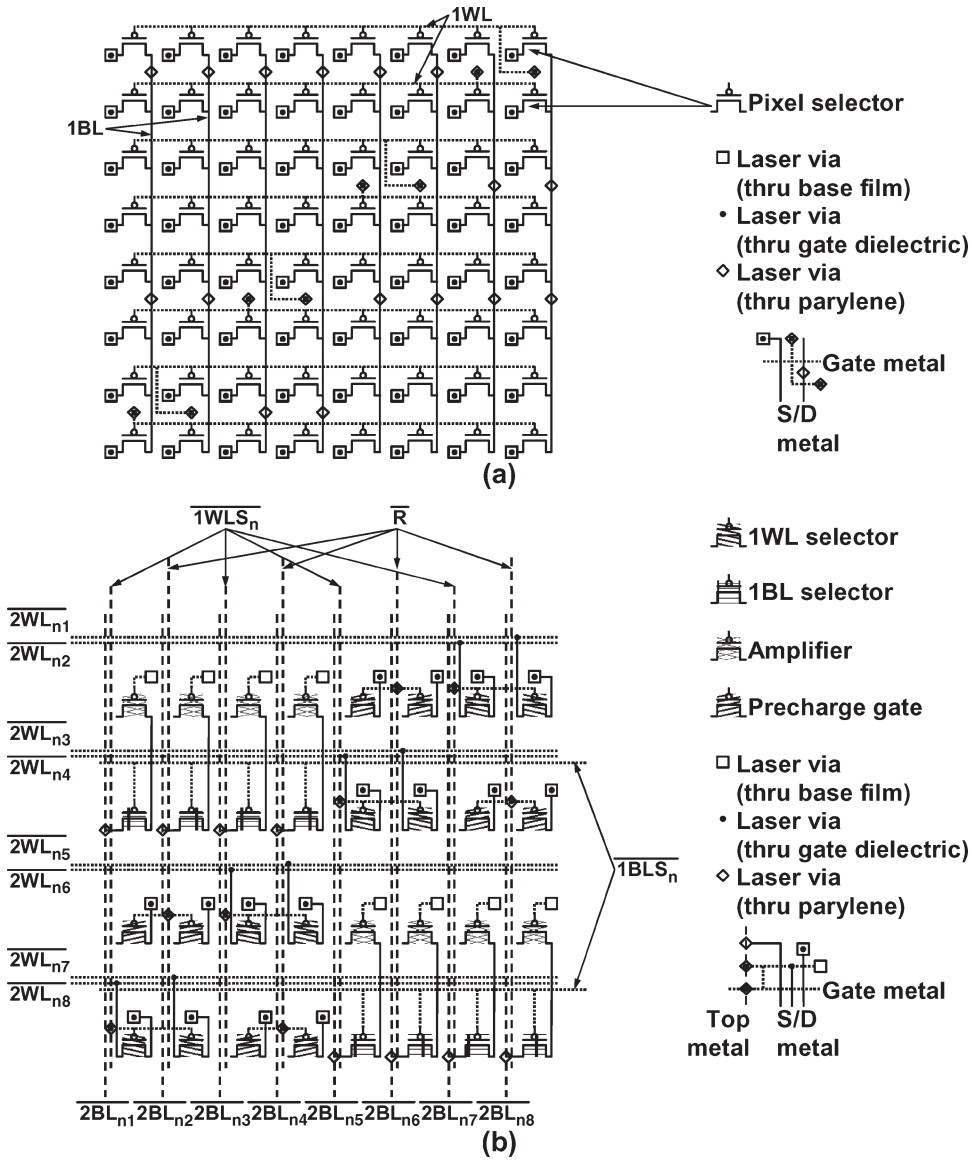

Fig. 9. Layouts on (a) OFET sheet 1 and (b) OFET sheet 2.

sensing is impossible. Moreover, since the OFET is large, only a single OFET per pixel is allowed and there is no room left for the peripheral circuits in the pixel region. As a result, the peripheral circuits of the sheet-type scanner are to be separated and stacked as illustrated in Fig. 8(b). The peripheral circuits are disposed on the separate OFET sheet 2, and stacked on the pixel-selector sheet (OFET sheet 1) with the 3-D-stack integration.

Fig. 9(a) shows the layout of the pixel selectors on the OFET sheet 1. There are 8×8 pixel selectors in a block. Under this sheet, there is the OPD sheet.

The OFET sheet 2 is the peripheral-circuit sheet, on which there are four kinds of OFETs including 1WL selectors, 1BL selectors, amplifiers, and precharge gates. As shown in Fig. 9(b), the checkerboardlike layout fulfills the requirement for connectivity. Between transistor rows, there are interconnection channels since a design rule for laser vias is loose, which reduces the transistor density to a half of the OFET sheet 1.

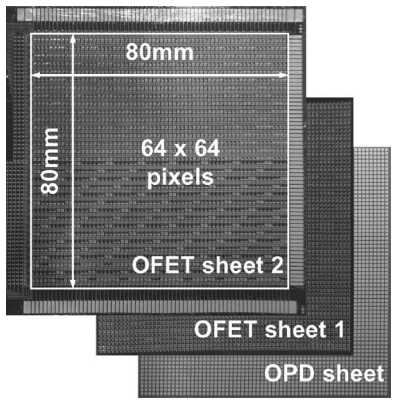

Fig. 10. Photograph of sheet-type scanner.

IV. Results

Fig. 10 shows a photograph of the three organic sheets before being laminated as a sheet-type scanner. A pixel size

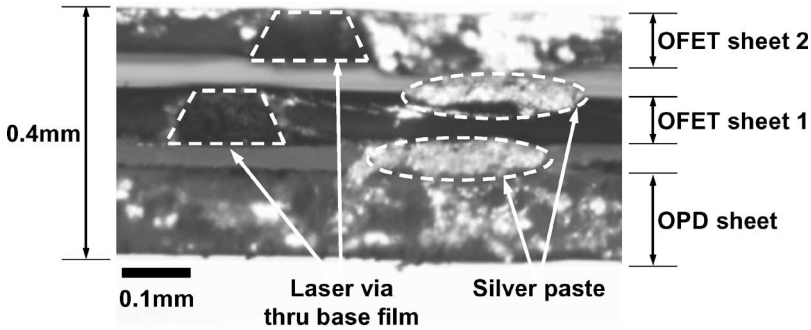

Fig. 11. Cross-sectional photograph of sheet-type scanner.

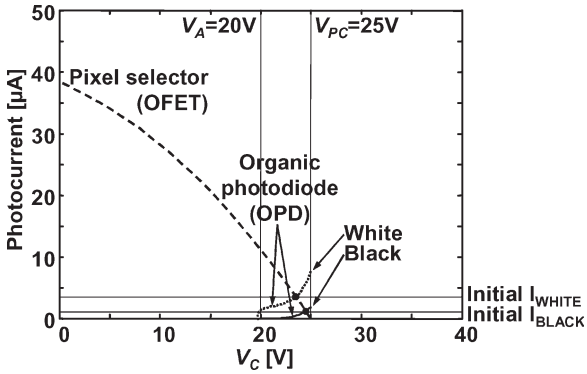

Fig. 12. Measured I–V characteristics on 1BL.

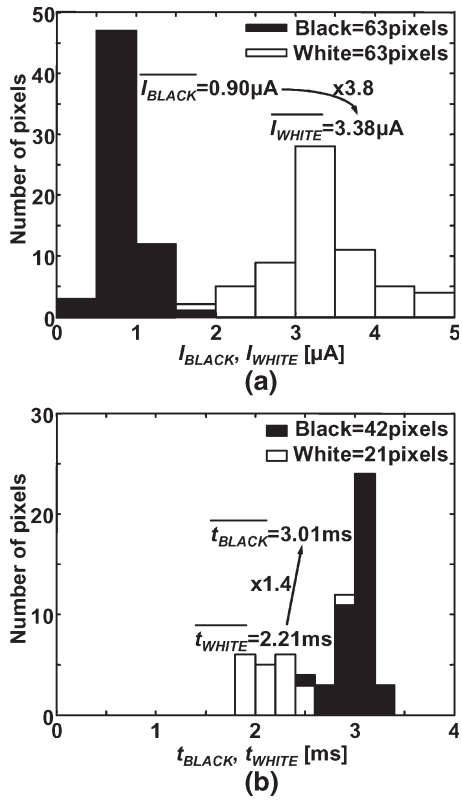

Fig. 13. Measured histograms of (a) photocurrents and (b) rise time of second-bitline voltage.

is 1.27×1.27 mm^2, which corresponds to 20 dpi. Namely, 64×64 pixels occupy 80×80 mm^2 in area. The major obstacle to enhance resolution is the design rule for the laser

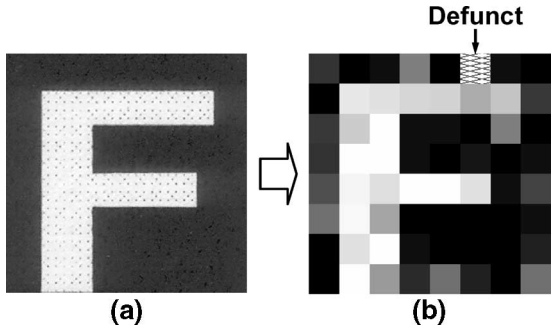

Fig. 14. (a) Original, and (b) scanned image of "F."

vias as aforementioned. The size and enclosure rules of the laser vias are more than 100 μm in our process technology. The total thickness of the sheet-type scanner is 0.4 mm as shown in Fig. 11, and the total weight is 1 g. The sheet-type scanner is so thin and flexible that it can take an image of a round object such as a label on a wine bottle, which is impossible for the conventional commercial scanners. The minimum bending radius is 30 mm, below which an ITO-layer is broken down.

A. Photocurrent

Fig. 12 shows measured I–V characteristics of the pixel selector and OPD on a 1BL when the light intensity is 80 mW/cm^2. $V_{\rm C}$ in Fig. 12 indicates the cathode voltage in Fig. 6(b). The on/off ratio of the OFET achieved is 10^5. A 1BL is precharged to 25 V with the reset signal ($\overline{\rm R}$) and the anode voltage of the OPD ($V_{\rm A}$) is 20 V as discussed in the previous section. After $\overline{\rm R}$ is negated, $I_{\rm BLACK}$ initially flows when a pixel is black through a 1BL. Alternatively, when a pixel is white, $I_{\rm WHITE}$ flows as an initial value.

B. Scanned Image

Fig. 13(a) and (b) shows the measured histogram of the initial $I_{\rm BLACK}$ and $I_{\rm WHITE}$ in a block, and that of the rise times of the second-bitline voltages when the image "F" in Fig. 14(a) is scanned. Since one OPD is defunct, the number of samples in the block is 63 $(= 8 \times 8 - 1)$. The major malfunction mode of the OPD is that a laser via through the parylene passivation on the OPD sheet passes to the common anode of the OPD, which means electrical short. Although the average ratio of $I_{\rm WHITE}/I_{\rm BLACK}$ is 3.8, that of $t_{\rm BLACK}/t_{\rm WHITE}$ results in

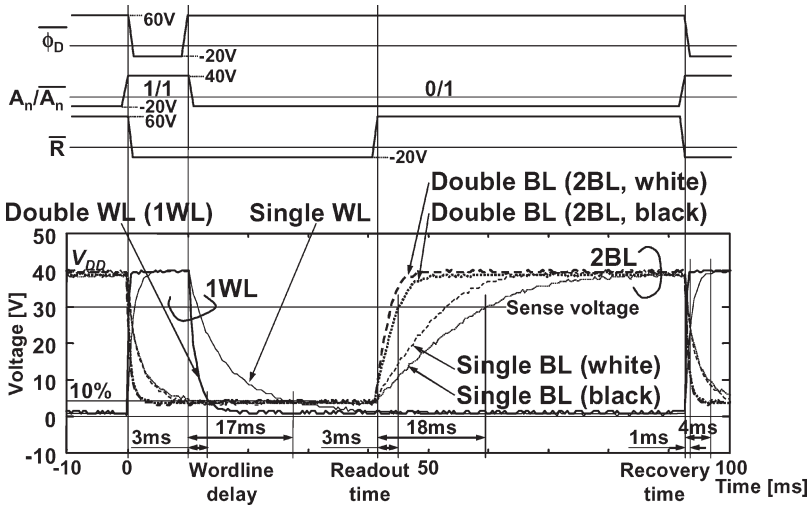

Fig. 15. Measured operational waveforms.

1.4 due to the photocurrent-integration scheme, which almost agrees with the simulation in Fig. 7. In order to compensate this small dynamic range, before scanning an image, pure black paper and pure white paper are both scanned at first. Then, we scan an image, and interpolate every pixel datum between the data of the pure black and white. Fig. 14(b) is the obtained image "F" by the interpolation.

C. Operational Waveforms and Delays

The measured operational waveforms are shown in Fig. 15 together with a sketch of stimulus signals. All inputs are driven with the high-voltage buffers, Toshiba TD62981P, and outputs are observed with the high-voltage probe, Tektronix P6015A, which impedance is 100 MΩ. For comparison, we manufactured both devices of the conventional single-wordline and single-bitline scheme, and the proposed double-wordline and double-bitline structure.

In the proposed structure, the fall time of a 1WL from $V_{\rm DD}$ to 10% of $V_{\rm DD}$ (4 V) is 3 ms while that in the conventional single-wordline scheme is 17 ms. That is, the delay on the wordline is shorten about a factor of six as well as the wordline-delay simulation in Fig. 5.

On a 2BL in the proposed structure, $t_{\rm BLACK}$ is defined as a readout time because $I_{\rm BLACK}$ is smaller than $I_{\rm WHITE}$ and $t_{\rm BLACK}$ is larger than $t_{\rm WHITE}$. When the sense voltage of a 2BL is set to 30 V, the readout time in the conventional scheme is 18 ms while that in the proposed structure is 3 ms, achieving six-fold improvement too.

The cycle time in the conventional scheme is 39 ms (the wordline delay is 17 ms, the readout time is 18 ms, and the recovery time is 4 ms) while that in the proposed structure is 7 ms (the wordline delay is 3 ms, the readout time is 3 ms, and the recovery time is 1 ms). This shows that the cycle time is reduced by a factor of five.

D. Power

In the conventional scheme, the total power measures 2.5 mW at the 39-ms cycle time while that in the proposed structure is 900 μW at the 7-ms cycle time. If the cycle time in the proposed structure is set to 39 ms as long as the cycle time in the conventional scheme, the power reduces to 350 μW, which indicates that the proposed structure saves the power by a factor of seven.

V. Future Direction

In future, we suppose that we will be able to make a scanner with 300-dpi resolution and 2048 $\times$ 2048 pixels in size, which might take thousands of seconds to scan out using the conventional single-wordline and single-bitline scheme. Alternatively, with the proposed double-wordline and double-bitline structure, we can shorten the scan-out time by a factor of 40 even in such a high-resolution and large-area scanner, and make the scan-out time down to tens of seconds. We can save the power by the same factor, too. The proposed approach can be applicable to other types of large-area OFET sensors including the e-skin and solves fundamental issues in large-area sensor electronics. We believe that the proposed structure will be essential for organic large-area sensors in future.

In the measurement, an artificial light source was used, however, it will be potentially replaced to an ambient one. A gate capacitance of an OFET will decrease as scaling is advanced. The hierarchical-bitline structure will divide a bitline into smaller segments, and reduce a bitline capacitance more and more in future. Thanks to the 3-D-stack integration, we can also put an amplifier near the segmented bitline without degrading the aperture. This means that an OPD just draws a charge out of a relatively small capacitance. Consequently, we believe that we will be able to improve the sensitivity of the photocurrent in future, making it possible to use an ambient light as a light source.

VI. Summary

The effectiveness of the double-wordline and double-bitline structure that reduces the delay and power by a factor of five and seven, respectively, was verified through the measurement. In order to implement the proposed structure, one OPD sheet

and two OFET sheets were integrated into a 3-D-stack sheet-type scanner, and the operation principle of the scanner was confirmed.

The new dynamic decoder with low-power capability that does not draw an active leakage current was introduced, while the conventional decoder suffers from a microampere-order active leakage current. Furthermore, it is a ratioless circuit, and thus more tolerant of process, threshold-voltage and supply-voltage variation/fluctuation than the conventional ratio-type one. The cut-and-paste customization can be applied to the proposed decoder as well.

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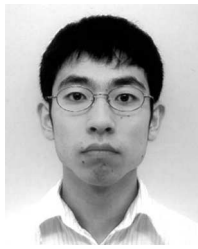

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