TABLE IV
COMPARISON OF DIFFERENT TURBO DECODER CHIP

	Proposed design	[9]	[10]
Coding rate (R)	1/5	1/3	1/3
Block length	20,730	5,114	5,114
Data rate (Mb/s)	4.52 6 iterations	2.048 10 iterations	24 6 iterations
Technology	0.18-μm	0.18-μm	0.18-μm
Chip core size (mm^2)	7.29	9	14.5[1]
Energy efficiency (nJ/b/iter.)	4.46	14.25	10

[1] Without Viterbi decoder

83 mW in decoding a turbo code with the block length of 20 730. The chip is also designed to work reliably with the wider supply voltage range.

ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center for chip measurement assistance.

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Leakage-Suppressed Clock-Gating Circuit With Zigzag Super Cut-Off CMOS (ZSCCMOS) for Leakage-Dominant Sub-70-nm and Sub-1-V-$V_{\rm DD}$ LSIs

Kyeong-Sik Min, Hun-Dae Choi, H.-Y. Choi, Hiroshi Kawaguchi, and Takayasu Sakurai

***Abstract*—As a candidate for the clock-gating scheme, Zigzag Super Cut-off CMOS (ZSCCMOS) has proposed to reduce not only the switching power but also the leakage power. Due to its fast wakeup nature, the ZSCCMOS can be best suited to the clock-gating scheme. The wakeup time of the ZSCCMOS is estimated to be 12 times faster than the conventional Super Cut-off CMOS (SCCMOS) in 70-nm process technology. From the measurement of wakeup time in 0.6-μm technology, it is observed to be eight times faster than the conventional scheme. Layout area, power, and delay overhead of the ZSCCMOS are discussed and analyzed in this paper.**

***Index Terms*—Clock-gating circuit, leakage suppression circuit, low-power circuit, Super Cut-off CMOS (SCCMOS), Zigzag Super Cut-off CMOS (ZSCCMOS).**

I. INTRODUCTION

As CMOS technology is scaled down and the supply voltages ($V_{\rm DD}$s) are further decreased, the threshold voltages ($V_{\rm TH}$s) should also be scaled down to prevent speed degradation. Decreasing $V_{\rm TH}$ by 0.1 V, however, will increase the subthreshold leakage by more than ten times. Assuming a high-performance device and one million gates in a chip, the chip leakage can reach as much as 40 mA, even in the sleep mode [1]. This large leakage is unacceptable in most portable applications [2].

Of the existing leakage reduction schemes, the Super Cut-off CMOS (SCCMOS) can be used below 1 V $V_{\rm DD}$ without severe speed degradation because the power switch is made with a low-$V_{\rm TH}$ MOSFET. For example, the SCCMOS in [3] can suppress the leakage down to a 1 pA-order per gate when $V_{\rm DD} = 0.8$ V. Although the SCCMOS successfully suppresses the sleep-mode leakage, the wakeup time is so long that it cannot be used for the active mode. In the active mode, a fast wakeup time is needed to maintain the normal operating speed. The wakeup time of the SCCMOS, amounts up to several clock cycles. In addition, a high -rush current may arise at this transition. The long wakeup time and high rush current make the SCCMOS difficult to use in the active mode where the wakeup occurs frequently. If the SCCMOS is used in the active mode, the several clock cycles of the wakeup process are stolen many times and the overall performance in the active mode is degraded severely.

To overcome the wakeup issues of the SCCMOS, Zigzag-Super-Cut-off CMOS (ZSCCMOS) scheme with a fast wakeup has been proposed and this scheme successfully realizes the clock-gating scheme that saves both the switching and leakage components of power dissipation [4]. The conventional clock gating saves switching power by turning off the local clock whenever the block is not in use. For example, an MPEG-4 decoder chip reportedly saves 72% of the switching

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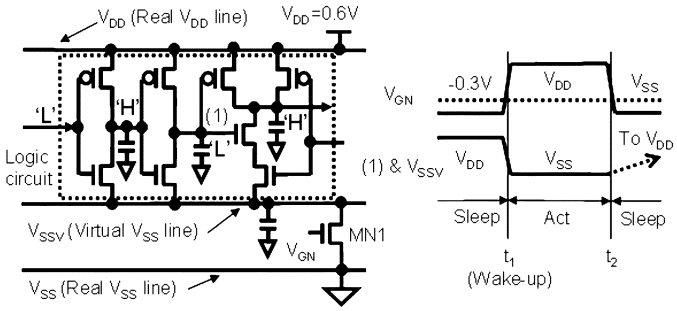

Fig. 1. SCCMOS scheme.

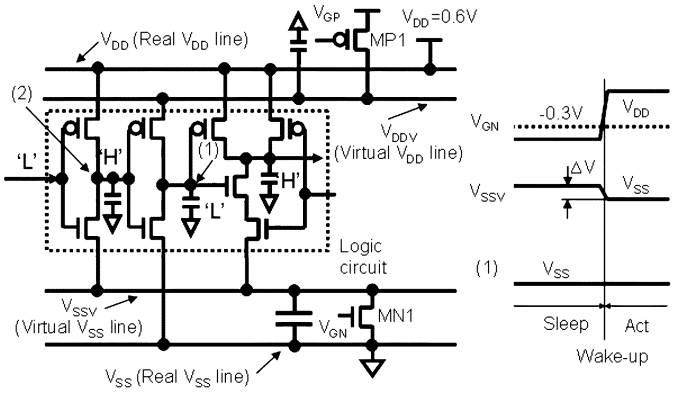

Fig. 2. ZSCCMOS scheme.

power by using the clock gating [5]. In this paper, layout area, power, and delay overhead due to the ZSCCMOS clock-gating scheme are discussed and analyzed.

II. ZSCCMOS

Fig. 1 shows a schematic of the original SCCMOS. Assume that the voltage of node (1) is initially low in the active-to-sleep transition. When the power switch MN1 is turned off by applying a gate voltage $V_{\rm GN} = -0.3$ V at t_2, node (1) and $V_{\rm SSV}$ go gradually to high and are pinned around $V_{\rm DD}$ if the sleep time is long. This phenomenon occurs because the leakage of the power switch is much smaller than the leakage of OFF MOSFETs in the logic block. Here, the gate source voltage of OFF MOSFET is biased by 0 V. Although node (1) and $V_{\rm SSV}$ in Fig. 1 become high in the sleep mode, they should be restored from high to low at the following sleep-to-active transition. In addition, because of the large charges associated with gates nodes and $V_{\rm SSV}$, which are restored at the next transition are large, the wakeup of the SCCMOS takes a long time and its rush current becomes large. Usually, because the logic blocks in the clock gating are activated within one or two clock cycles, the long wakeup time prevents the SCCMOS from being merged with the clock-gating scheme.

Fig. 2 shows the ZSCCMOS, where all the OFF PMOSFETs are connected to a virtual $V_{\rm DD}$ line ($V_{\rm DDV}$). Similarly, all the OFF NMOSFETs are connected to a virtual $V_{\rm SS}$ line ($V_{\rm SSV}$). Because the virtual power lines are connected to real power lines through the power switches of MN1 and MP1, if MN1 is turned off by -0.3 V, the $V_{\rm SSV}$ goes up and applies a negative $V_{\rm GS}$ to the OFF NMOSFETs. The leakage of OFF NMOSFETs, therefore, can be strongly suppressed by using this negative $V_{\rm GS}$ effect. The $V_{\rm SSV}$ goes up and is pinned at ΔV, where, as shown in Fig. 2, the leakage of the OFF NMOSFETs becomes the same with the MN1. In this case, all the gate nodes should be predictable in the sleep mode because the OFF NMOSFETs in the ZSCCMOS are connected to $V_{\rm SSV}$, whereas the OFF PMOSFETs are separately connected $V_{\rm DDV}$.

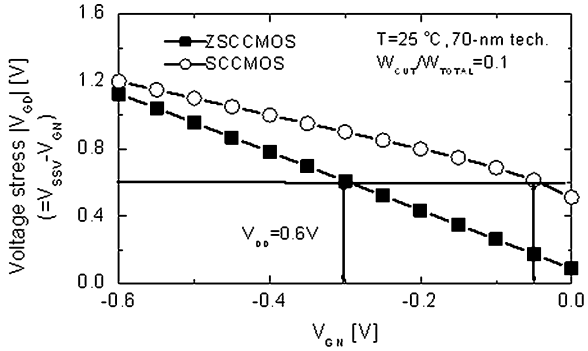

Fig. 3. Voltage stress plot of the power switches of SCCMOS and ZSCCMOS. Here, $V_{\rm GD}$ is the gate-drain voltage of MN1 in Figs. 1 and 2.

The zigzag configuration in Fig. 2 produces the fast wakeup time and the small rush current at the sleep-to-active transition. Assume that nodes (1) and (2) in Fig. 2 are predetermined as low and high in the sleep mode, respectively. To do so, nodes (1) and (2) are forced to be "low" and "high" just before the sleep mode starts. After forcing them, because the voltages on nodes (1) and (2) do not change during the sleep time, they do not need to be restored to high or low at the following sleep-to-active transition.

For the $V_{\rm SSV}$, the $V_{\rm SSV}$ increases and finally saturates at ΔV. In this case, the negative $V_{\rm GS}$ biasing by the $V_{\rm SSV}$ increase is the primary means of determining the value of ΔV, because the leakage current has the strongest dependence on its $V_{\rm GS}$. The drain-induced barrier lowering (DIBL) and body-bias effects can also be considered as secondary means of determining the value of ΔV. By using the 70-nm Berkeley Predictive Technology Model (BPTM), ΔV is estimated to be 0.3 V when $V_{\rm DD} = 0.6$ V and $V_{\rm GN} = -0.3$ V [6].

By comparing amounts of charge to be restored at the sleep-to-active transition between the SCCMOS and the ZSCCMOS, it is found that the capacitance of SCCMOS is 20 times larger than the ZSCCMOS. The comparison is done by SPICE simulation with 70-nm BPTM [6]. It is assumed that the width of a power switch is one tenth of the total logic width. If this ratio becomes smaller than one tenth, the discrepancy in the capacitance increases. Because the ZSCCMOS has a smaller capacitance and less voltage swing (ΔV) than the SCCMOS, the wakeup time is shorter and the rush current is smaller than in the SCCMOS. The zigzag concept was proposed in [7], where its power switch is made with high $V_{\rm TH}$. By doing so, both the wakeup time and operation speed are degraded when $V_{\rm DD}$ drops below 1 V. Its low $V_{\rm TH}$ versions were suggested in [4] and [8].

The MN1 and MP1 in Fig. 2 can be implemented by devices with high $V_{\rm TH}$s and thick oxides. This scheme is named by Zigzag Boosted Gate MOS (ZBGMOS) [4], where the MN1 is turned off by 0 V and on by a voltage higher than $V_{\rm DD}$. This ZBGMOS scheme consumes a voltage-generating power only in the active mode; no power is used in the sleep mode.

Fig. 3 shows a voltage stress plot of the power switches in Figs. 1 and 2. The parameter $W_{\rm CUT}$ is the width of the power switch and $W_{\rm TOTAL}$ is the total channel width of all the devices with the same polarity. This simulation is done by using 70-nm BPTM when $V_{\rm DD} = 0.6$ V, $V_{\rm TH} = 0.06$ V, and $T = 25\,^{\circ}$C. The $V_{\rm TH}$ is defined by a gate-source voltage when $I_{\rm DS} = 100$ nA/μm at $V_{\rm DS} = V_{\rm DD}$. The y-axis in Fig. 3 shows the stressed $|V_{\rm GD}|$ values that are applied to the power switches of Figs. 1 and 2; the maximum stress voltage occurs between the gate and drain of the power switch. Fig. 3 indicates that over-stress voltage higher than $V_{\rm DD}$ does not occur as long as $|V_{\rm GN}|$ value is smaller than 0.3 V in the ZSCCMOS. In this case, $V_{\rm GN}$ is a negative voltage applied to the gate of the power switch. In the conventional SCCMOS, however, $|V_{\rm GD}|$ begins to exceed $V_{\rm DD}$ when

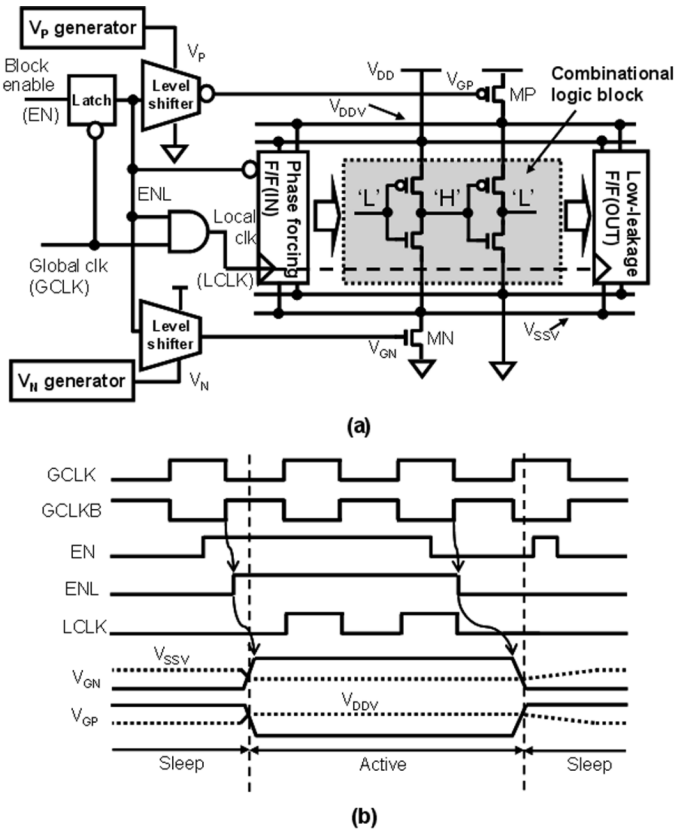

Fig. 4. (a) ZSCCMOS block activation scheme with the combinational logic block, F/Fs, and the control logic of the clock gating. (b) Waveforms of Fig. 4(a).

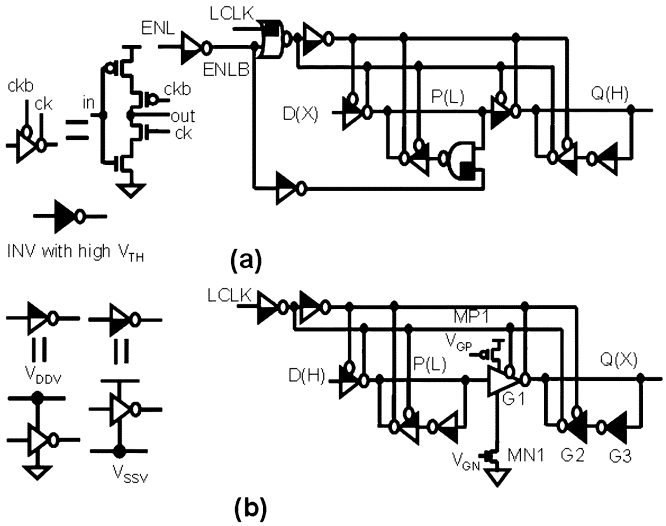

Fig. 5. (a) Schematic of input flip-flop with phase-forcing circuit. (b) Schematic of low-leakage output flip-flop.

$|V_{\rm GN}|$ becomes larger than 0.05 V; at this point, an over-voltage-stress problem can occur. This small allowance of $|V_{\rm GN}|$ limits the cutoff magnitude in the SCCMOS severely. To avoid this small cutoff magnitude, one more power switch in Fig. 1 should be in series with another switch [3]. Two switches in series in the SCCMOS, however, degrade the operating speed in the active mode.

Now, let us discuss the gate leakage issues. Because the gate-oxide tunneling and gate-induced drain leakage (GIDL) currents [8], [9] are not suppressed by inserting the power switches between real and virtual power lines, the effect of ZSCCMOS is alleviated. For example, the leakage saving when the 65-nm BPTM is used, is estimated to be as large as 88% at room temperature and 95% at 100 °C, respectively, assuming $V_{\rm DD} = 0.6$ V. In this case, the 65-nm BPTM includes both GIDL and oxide leakage [6]. The 88% and 95% can be interpreted as the oxide and GIDL components, which comprise as much as 12% and 5% of the total leakage at room temperature and 100 °C, respectively. In the case of the leakage current, the worst case condition always occurs under the highest temperature; hence, the leakage saving of 95% at 100 °C is more meaningful than that of 88% at 25 °C. At sub-50-nm processes, a high-k dielectric is thought to be a good candidate for remedying the oxide leakage problem, though a solution has not yet been provided.

III. Clock-Gating Circuit With ZSCCMOS

With its fast wakeup nature, the ZSCCMOS is well suited to the clock-gating scheme. In this new clock gating substitute with the ZSCCMOS, the leakage power is suppressed by turning off the local power switches of MN and MP in Fig. 4(a) in a blockwise manner, in addition to turning off the local clock. Because the wakeup time at the sleep-to-active transition is within one or two cycles in the ZSCCMOS, the block-wise activation occurs instantaneously. Hence, the clock gating with the ZSCCMOS can reduce the leakage of the active mode.

Fig. 4(a) shows the clock-gating scheme with the ZSCCMOS. The scheme includes a combinational logic block (CLB), input and output F/Fs, and a control circuit that drives the power switches of MN and MP. A local clock (LCLK) is controlled by a block enable signal (EN). The phase-forcing input F/F in Fig. 4(a) makes all internal gate nodes in the logic block predictable in the sleep mode, where OFF NMOSFETs are connected to the NMOS power switch and OFF PMOSFETs to PMOS one. Fig. 4(b) shows the schematic waveforms for Fig. 4(a). The $V_{\rm SSV}$ should be restored to $V_{\rm SS}$ before the LCLK arrives at the input F/Fs; hence, the wakeup in the clock gating must be fast.

To force all the gate nodes to behave in their predetermined states in the sleep mode, a new phase-forcing circuit is added to the input F/Fs as depicted in Fig. 5(a). In this case, nodes "P" and "Q" are forced to be low and high, respectively, even though input "D" is unknown during the sleep time. Without forcing the input phase, the internal gate nodes in the logic block are not predictable in the sleep mode; hence, the $V_{\rm SSV}$ goes to high and the $V_{\rm DDV}$ goes to low. If so, the large rush current and the long wakeup delay ruin the benefits of ZSCCMOS at the subsequent sleep-to-active transition.

Fig. 5(b) shows a leakage-suppressed output F/F. Because node "Q" in the output F/F is connected to the other logic block driven by a different LCLK or a global clock (GCLK), the "Q" should not be forced to be high or low as in the input F/F in Fig. 5(a) and should keep its logic state even during the sleep time. Therefore, the gates G1, G2, and G3 in Fig. 5(b) should not be connected to the virtual power lines. Because the G2 and G3 in Fig. 5(b) are not on the critical path, they can be built with high-$V_{\rm TH}$ devices without severely degrading the operating speed. In Fig. 5(b), the G1 is connected to both the NMOS and PMOS power switches to reduce the leakage. In the sleep mode, the output "Q" in Fig. 5(b) can be retained by the cross-coupled inverter with the G2 and G3 with high $V_{\rm TH}$, not allowing the leakage. Finally, the area overhead due to the power switches in Figs. 5(a) and (b) and MN1 and MP1 in Fig. 5(b) can be estimated by about 15%.

From Fig. 6(a), the clock-to-Q delay of the leakage-suppressed input F/F in Fig. 5(a) seems to be 10% slower than the conventional F/F because of inserted power switches. This 10% degradation is very similar to the delay penalty of the MTCMOS and the SCCMOS [3]. The leakage-suppressed output F/F in Fig. 5(b) has a larger delay penalty than the input F/F in Fig. 5(a). This difference is due to the G1 gate in Fig. 5(b). In this case, the power switches of G1 cannot be shared with the other gates because its output node "Q" is unpredictable in the sleep mode.

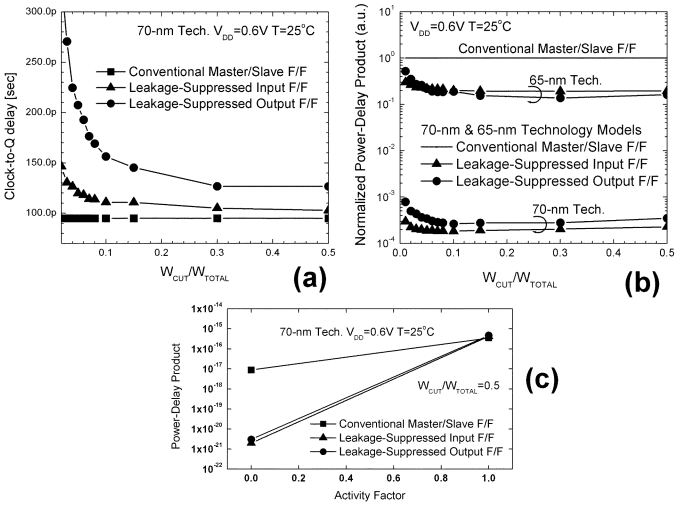

Fig. 6. (a) Clock-to-Q delay simulation of various F/Fs. (b) Power-delay product simulation of various F/Fs. (c) Power-delay product simulation with varying activity ratios. Here, the $V_{\rm TH}$s of 70-nm and 65-nm BPTMs are 0.06 and 0.05 V, respectively, and the temperature is 25 °C.

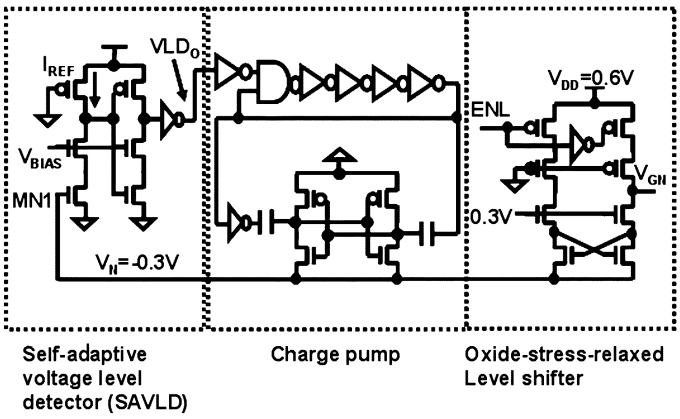

Fig. 7. $V_{\rm N}$ (negative voltage) generator for NMOS power switch.

Fig. 6(b) compares the power-delay products of the conventional, input, and output F/Fs with respect to the 70- and 65-nm BPTMs. Because the leakage components of power dissipation for the input and output F/Fs are suppressed by as much as three orders of magnitude, the power-delay products are improved by three orders as indicated in Fig. 6(b), when the 70-nm BPTM is used. The power-delay products seem to be improved by one order of magnitude because the oxide and GIDL components comprise 12% of the total leakage when the 65-nm BPTM is used. Fig. 7(c) compares the power-delay products with varying the activity factor. When the activity factor is 0, the results are the same as the results shown in with Fig. 6(b). As the activity factor goes to 1, the products become dominated more by the delay than by the leakage power.

Fig. 7 shows a circuit diagram of $V_{\rm N}$ (negative voltage) generator for the NMOS power switch, which is shown in the clock-gating scheme in Fig. 4. The $V_{\rm N}$ generator circuit includes a self-adaptive voltage level detector (SAVLD), a charge pump, and an oxide-stress-relaxed level shifter (OSRLS). A negative voltage lower than $V_{\rm SS}$ can be distributed to $V_{\rm GN}$ without giving rise to any voltage-over-stress problem [10]. In the SAVLD, if $V_{\rm N}$ becomes too close to $V_{\rm SS}$, $\rm VLD_0$ turns on the charge pump to lower the value of the $V_{\rm N}$. It should be noted that the generated $V_{\rm N}$ changes self-adaptively with the leakage variations due to the process, voltage, and temperature fluctuation.

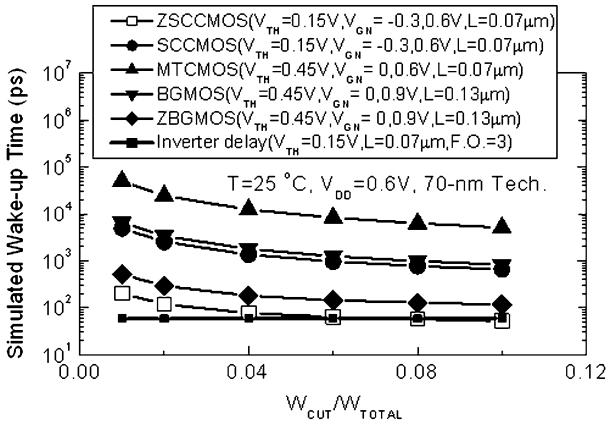

Fig. 8. Simulated wakeup times of ZSCCMOS, SCCMOS, BGMOS, MTCMOS, and ZBGMOS with 70-nm BPTM. The simulation is done with $T = 25$ °C and $V_{\rm DD} = 0.6$ V.

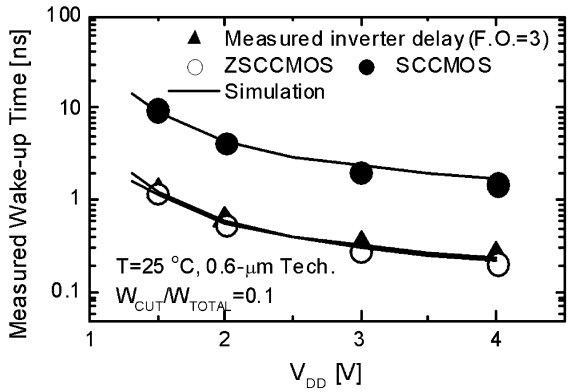

Fig. 9. Measured wakeup times of SCCMOS and ZSCCMOS in 0.6-μm technology.

IV. Simulated and Measured Results

For the 70-nm BPTM, Fig. 8 compares the $V_{\rm SSV}$ wakeup times of various schemes, where the $V_{\rm SSV}$ wakeup time is defined by the time at which $V_{\rm SSV}$ is lowered to 5% of $V_{\rm DD}$. As shown in Fig. 8, the ZSCCMOS with the fast wakeup time can wake up the logic block within one or two cycles. Compared with the SCCMOS, the wakeup time of ZSCCMOS is 12 times faster so that the ZSCCMOS is more suitable for the clock gating than the SCCMOS.

Fig. 9 compares the measured wakeup times of the SCCMOS and the ZSCCMOS, both of which were fabricated in 0.6-μm CMOS technology. This comparison indicates that the wakeup time of the ZSCCMOS is eight times faster than the SCCMOS in 0.6-μm technology.

In the clock gating with the ZSCCMOS, additional switching energy is lost in phase-forcing and driving of the power switches by $V_{\rm N}$ and $V_{\rm P}$. As stated earlier, the internal gate nodes in the ZSCCMOS circuits should be predictable during the sleep time. Hence, all gate nodes should be forced to be low or high according to their predetermined states when the sleep mode starts. Fig. 10(a) compares the energy dissipation between the conventional and the ZSCCMOS by increasing the sleep time. The simulation is done when $V_{\rm DD} = 0.6$ V and $T = 100\,^{\circ}$C, using the 70-nm BPTM. The simulated circuits are chosen among the practical ones; the chosen circuits have 708 NANDs, 456 NORs, and 360 inverters. Here, the phrase "% phase-inverted nodes = 50%" in Fig. 10(a), means that half the gate nodes are inverted at the active-to-sleep transition and the other half remain unchanged. The conventional circuit in Fig. 10(a)

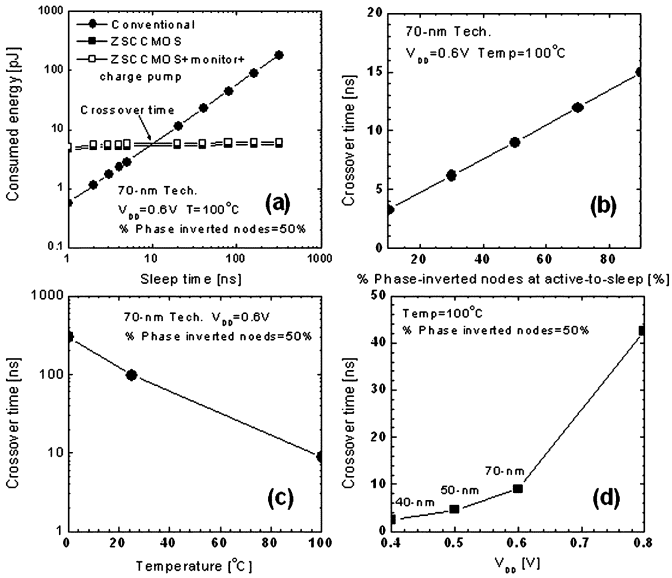

Fig. 10. (a) Energy consumption with increasing sleep time. (b) Crossover time with varying percentage of phase-inverted nodes at the active-to-sleep transition. (c) Crossover time with varying temperature. (d) Crossover time with various process nodes.

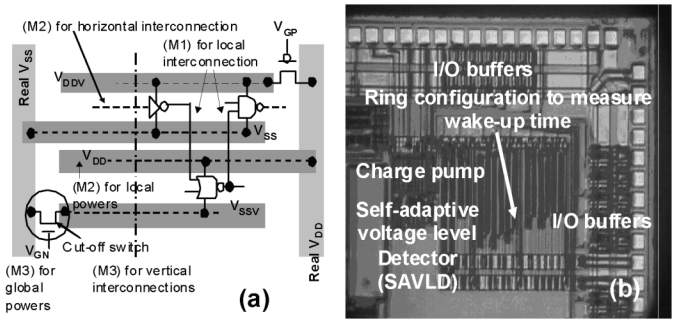

Fig. 11. (a) Layout of ZSCCMOS with power switches and virtual and real power lines. (b) Test chip micrograph with 0.6-μm technology.

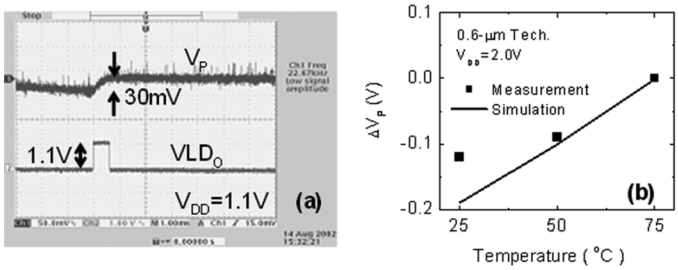

Fig. 12. (a) Measured operating waveforms of $V_{\rm P}$ (positive voltage) generator. (b) Measured $V_{\rm P}$ with varying temperature.

is the logic circuit that uses no leakage suppression schemes such as SCCMOS and ZSCCMOS. Although the ZSCCMOS consumes more energy at the beginning of sleep than the conventional circuit, the leakage saving of the ZSCCMOS compensates the initial loss of switching energy after 10 ns, as shown in Fig. 10(a). The period of 10 ns is defined by the crossover time from when the leakage saving begins to exceed the loss of switching energy.

The crossover time depends on various parameters such as temperature, percentage of phase-inverted nodes at the active-to-sleep transition, and the process technology. Fig. 10(b) shows the crossover time varying the percentage of inverted nodes at the active-to-sleep transition. As the percentage of phase-inverted nodes becomes larger, the crossover time also increases, as shown in Fig. 10(b).

To model the crossover time with varying % phased-inverted nodes, the following simple equation is used:

$$t = (E_0 + \alpha \times E_1)/P_S \tag{1}$$

where t, E_0, α, and P_S are the crossover time, switching energy overhead when % phase-inverted nodes $= 0$, % phase-inverted nodes, and saved power of this leakage-suppressed scheme, respectively. E_1 is the linear coefficient. The linear relationship between the crossover time and the percentage of nodes as shown in Fig. 10(b) means that (1) fits the SPICE simulation results well.

The temperature is another important parameter that affects the crossover time, because the leakage current is very sensitive to the temperature. Fig. 10(c) shows the crossover time with varying temperature. Fig. 10(d) compares the crossover times among various technology nodes.

Now, let us discuss the power overhead that is caused by the $V_{\rm N}$ generator circuit in Fig. 7. In this paper, the power overhead due to the circuits of Fig. 7, is designed to be less than 10% of the total sleep power that is consumed in all logic blocks. This 10% overhead is taken into account in the power overhead analysis done in Fig. 10(a). The crossover time, however, is increased by as little as 1 ns with this additional 10% overhead, as shown in Fig. 10(a).

Fig. 11(a) shows the layout of ZSCCMOS circuit. To minimize the area overhead due to $V_{\rm DDV}$ and $V_{\rm SSV}$ lines, the gates which are connected to $V_{\rm DDV}$ are grouped separately from the gates to $V_{\rm SSV}$, as shown in Fig. 11(a). Three-layer metals are assumed in Fig. 11(a), where M3 stands for global powers and vertical interconnections and M1 stands for local interconnections. M2 stands for the local power lines and horizontal interconnections. Fig. 11 shows that the layout overhead is caused from the power switches, not from the virtual power lines. The overhead due to the additional switches can be minimized by placing the switches under the routing channel. For complex circuits with many I/Os and gates, however, this layout style like Fig. 11(a) may require an additional routing area because the routing between the gates belonging to different groups needs longer metal lines than the routing between the gates in the same group. Generally, assuming that the width of the power switch is $1/10$ of the total logic width, the area overhead of Fig. 11(a) which includes the area of power switches and additional interconnections can be estimated to be about 15%. The test chip micrograph with 0.6-μm technology is shown in Fig. 11(b).

Fig. 12(a) shows the measured waveforms of the $V_{\rm P}$ generator fabricated in the 0.6-μm n-well CMOS technology. If $V_{\rm P}$ goes lower than a target value of 1.2 V, even by as little as 30 mV, the SAVLD turns on the charge pump and increases its $V_{\rm P}$ voltage toward the target value. Once the $V_{\rm P}$ voltage goes larger than the target voltage, the SAVLD turns off the pump. Fig. 12(b) shows the measured $V_{\rm P}$ with varying the temperature from 25 °C to 75 °C. This figure shows that the measurement agrees well with the simulation.

V. Conclusion

The clock-gating scheme is merged with the ZSCCMOS to reduce not only the switching component but also the leakage one in power dissipation. Due to its fast wakeup nature, the ZSCCMOS is well suited to the clock gating which has been developed to reduce the clock switching power. The effectiveness of ZSCCMOS for the clock-gating circuit is verified by the measurement, where the wakeup time is observed to be eight times faster than the conventional SCCMOS.

With the 70-nm BPTM, the wakeup time is expected to be 12 times faster than the conventional SCCMOS. Thus, the new clock-gating circuit with the ZSCCMOS will be able to suppress leakage current in both the sleep and active modes.

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