Novel Video Memory Reduces 45% of Bitline Power Using Majority Logic and Data-Bit Reordering

Hidehiro Fujiwara, *Student Member, IEEE*, Koji Nii, *Member, IEEE*, Hiroki Noguchi, Junichi Miyakoshi, Yuichiro Murachi, Yasuhiro Morita, *Student Member, IEEE*, Hiroshi Kawaguchi, *Member, IEEE*, and Masahiko Yoshimoto, *Member, IEEE*

***Abstract*—We propose a low-power two-port SRAM for real-time video processing that exploits statistical similarity in images. To minimize the discharge power on a read bitline, a majority-logic circuit decides if input data should be inverted in a write cycle, so that "1"s are in the majority. In addition, for further power reduction, write-in data are reordered into digit groups from the most significant bit group to the least significant bit group. The measurement result of a 68-kbit video memory in a 90-nm process demonstrates that a 45% power saving is achieved on the read bitline. The speed and area overheads are 4% and 7%, respectively.**

***Index Terms*—Data-bit reordering, low-power SRAM, majority logic, real-time image processing, two-port SRAM.**

I. Introduction

As THE ITRS Roadmap predicts, memory area is becoming larger [1]. This trend is continuing also for real-time video system-on-chip (SoC); an H.264 encoder for a high-definition television (HDTV) requires at least a 500-kbit memory as a search-window buffer, which consumes 40% of its total power [2]. In addition to a search-window buffer, a large-capacity SRAM will be implemented on a chip as a frame buffer or restructured-image memory in the future. In this paper, we propose a novel low-power two-port SRAM to save the SRAM power in real-time video applications.

A two-port SRAM is suitable for real-time video processing because it can make one read and one write within a single clock cycle [2]–[5]. In general, a read port has a single read bitline for area efficiency; the proposed SRAM also has the same structure as that shown in Fig. 1(a). Two nMOS transistors for a read wordline (RWL) and a read bitline (RBL) are added to a conventional single-port 6T SRAM, which frees a static noise margin (SNM) in a read operation [6], [7]. Therefore, a large β ratio [ratio of a driver transistor (N0 and N1) size to an access transistor (N2 and N3) size] is not required; thereby, the two nMOS driver transistors can be minimized.

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H. Fujiwara, K. Nii, H. Noguchi, J. Miyakoshi, Y. Murachi, and Y. Morita are with the Hidehiro Fujiwara, CS28, the Graduate School of Science and Technology, Kobe University, Kobe, Hyogo 657-8501, Japan (e-mail: fujiwara@cs28.cs.kobe-u.ac.jp).

H. Kawaguchi and M. Yoshimoto are with the Department of Computer and Systems Engineering, Kobe University, Kobe, Hyogo 657-8501, Japan.

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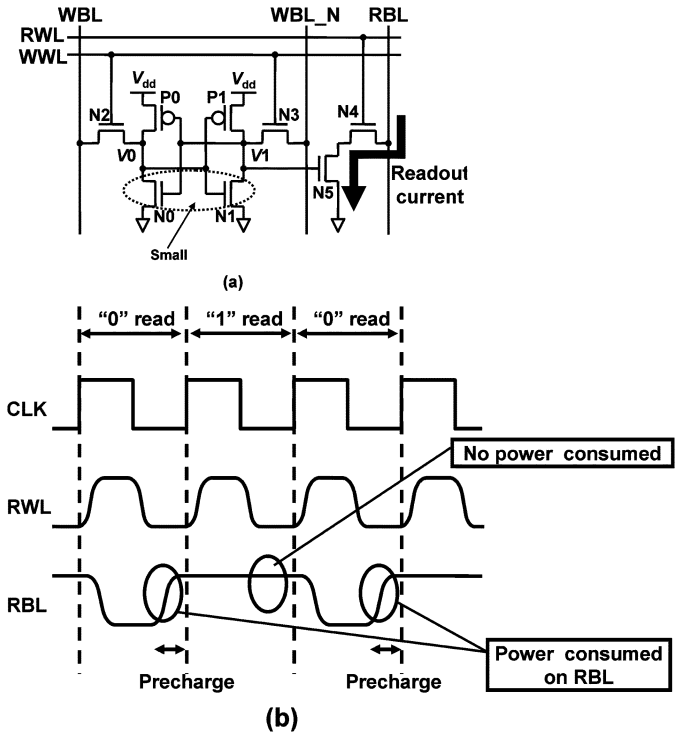


Fig. 1. 8T two-port SRAM cell: (a) schematic and (b) operation waveforms in read cycles.

Fig. 1(b) depicts simplified operation waveforms in read cycles. Since the precharge scheme is adopted and an RBL is precharged to a supply voltage $(V_{\rm dd})$ before the beginning of a clock cycle, the charge and discharge power are dissipated on the RBL when "0" ($V0 =$ "0", and $V1 =$ "1") is read out. In contrast, no power is consumed on the RBL when "1" is read out, which implies that it is better for low-power operation to write as many "1" as possible.

We append a majority-logic circuit to the two-port SRAM to increase the possibility that "1" is read and to reduce the RBL power. Although majority logic has been used on transmission lines to save input/output (I/O) bus power [8], to our knowledge it has not been used in a memory bus. In Section II, we introduce the concept of the proposed SRAM with majority logic.

In addition to majority logic, we exploit statistical similarity in video data for further power reduction. A pixel has strong correlation with adjacent pixels, which means that more significant bits in adjacent pixels are lopsided to either "0" or "1" with higher probability. We reorder the data bits of the adjacent

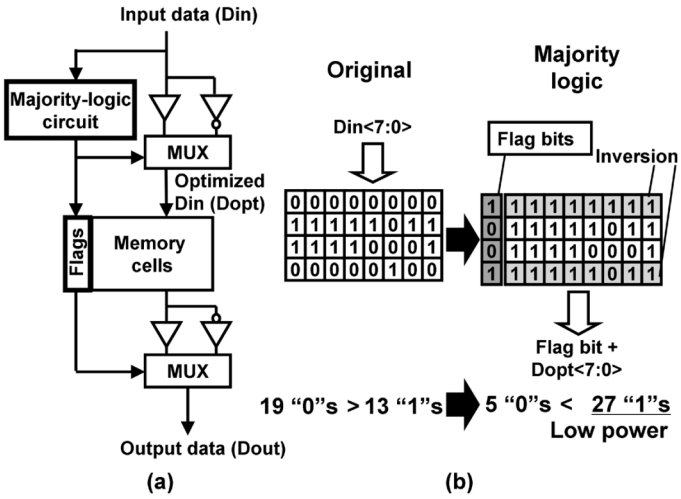


Fig. 2. Majority-logic circuit: (a) block diagram and (b) concept of flag bit.

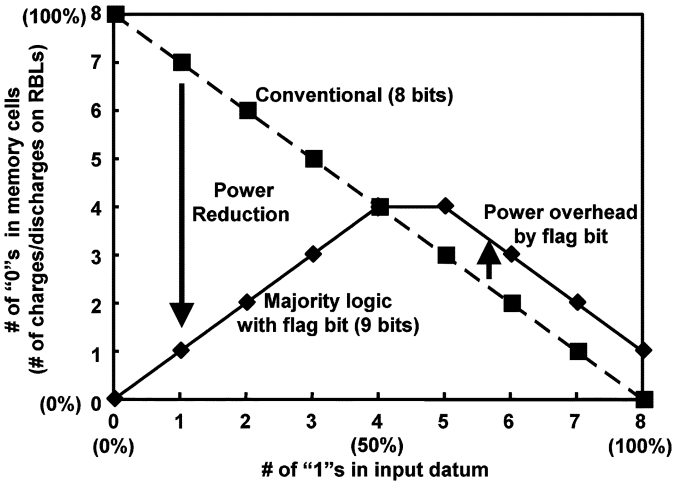


Fig. 3. Numbers of charges/discharges on RBLs in the conventional and proposed SRAM with majority logic.

pixels in each digit group to improve the majority-logic function, as discussed in Section III considering H.264 codec.

In Section IV, we describe the design methodology on a test chip in a 90-nm process. The measurement results are shown in Section V. The final section summarizes this paper.

II. Majority Logic

Fig. 2(a) shows a block diagram of the proposed SRAM with the majority logic. To maximize the number of "1"s, a majority-logic circuit counts the number of "1"s and decides if input data should be inverted in a write cycle, so that "1"s are in the majority. The inversion information ("1" denotes inversion) is stored in an additional flag bit, as depicted in Fig. 2(b). In a read cycle, the procedure is reversed. Output data are inverted if a flag bit is true, so that the original data can be read.

The mechanism on the RBL power reduction is shown simply in Fig. 3. The bit width of data is eight. If the "1"s in input data are eight, the data are not inverted; there are no "0"s in the data themselves. Therefore, one "0" is stored only in a flag bit. This means that one charge/discharge for the flag bit takes place on the read bitlines for the flag bit, which becomes a power overhead. In contrast, if the "1"s are four or fewer, the RBL power can be reduced because the input data are inverted by the majority-logic circuit to maximize the number of "1"s (to minimize the number of "0"s).

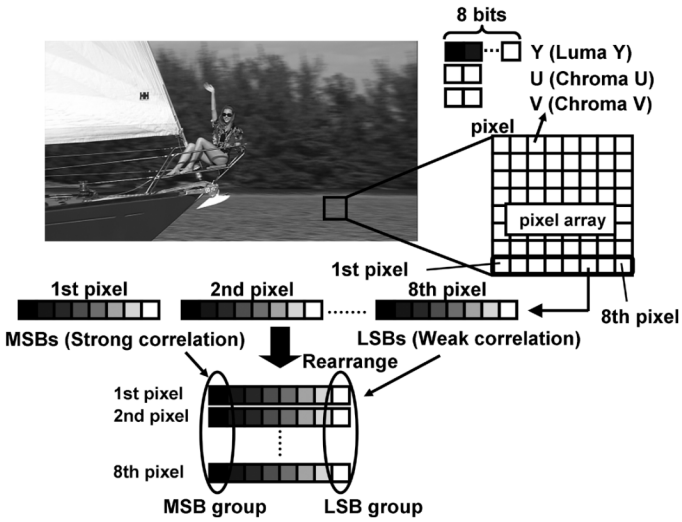


Fig. 4. Example of image data.

The number of charges and discharges is four out of the eight RBLs on average in the conventional two-port SRAM when input data have a random pattern. However, the majority logic reduces the average value to 3.27 even though the number of RBLs is increased to nine, which indicates that the majority logic statistically saves 18% of the RBL power in the random-pattern case if the power for the flag bit is as much as a power on one RBL. For image data, we can expect further power reduction because pixel data have local similarity.

It is important to consider which the inversion information in the flag bit should be, "0" or "1," because the RBL power even on the flag bit depends on its value. The inversion information should be "1" to maximize the number of "1"s if the "0"s in all date are more numerous than "1"s. As described previously, we chose "1" as the inversion flag based on statistical analyses of HDTV test sequences. That is described in greater detail in Section III.

III. Data-Bit Reordering

A. Statistical Characteristics of Video Images

In the H.264 codec, the YUV format is adopted as a pixel datum. An example image is shown in Fig. 4. One pixel is comprised of an 8-bit luma (Y signal) and a 4-bit chroma (U and V signals). In this study, only the luma data are considered. In an image, adjacent pixels are strongly correlated, and the correlation becomes stronger in more significant bits. The most significant bits (MSBs) in contiguous pixels tend to be lopsided to either "0" or "1" with high probability, whereas the values of the least significant bits (LSBs) are random. Consequently, the strength of correlation in each digit is different from others.

The distributions of the numbers of "1"s in different digit groups are represented in Fig. 5, where data of eight pixels (8×8 bits) are rearranged in each digit group. It is apparent that the MSB group (the rearranged MSBs in Fig. 4) and more

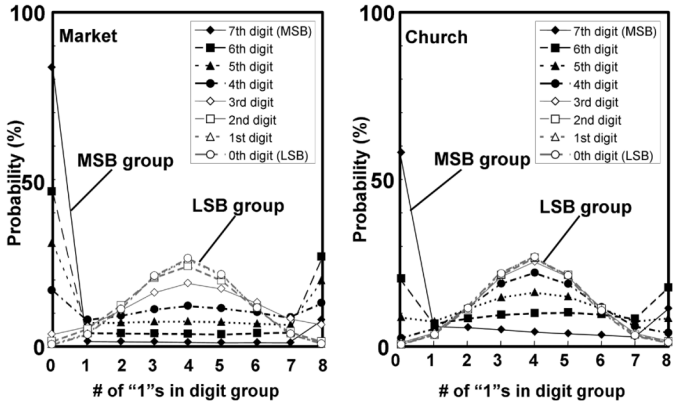


Fig. 5. Distributions of the numbers of "1"s in different digit groups, extracted from the HDTV test sequences "Market" and "Church."

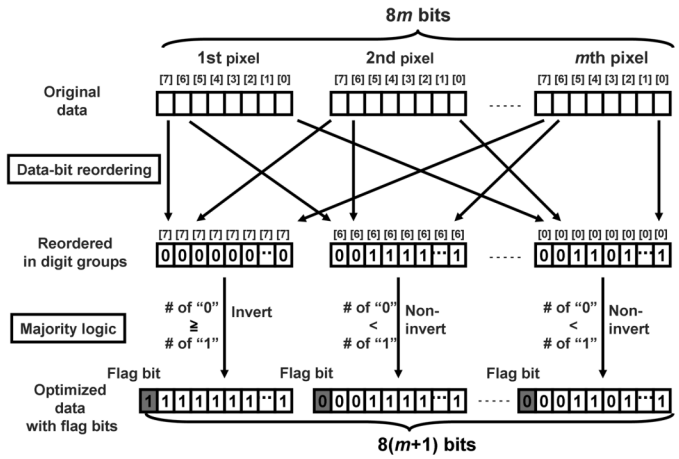


Fig. 6. Combination of data-bit reordering and majority logic.

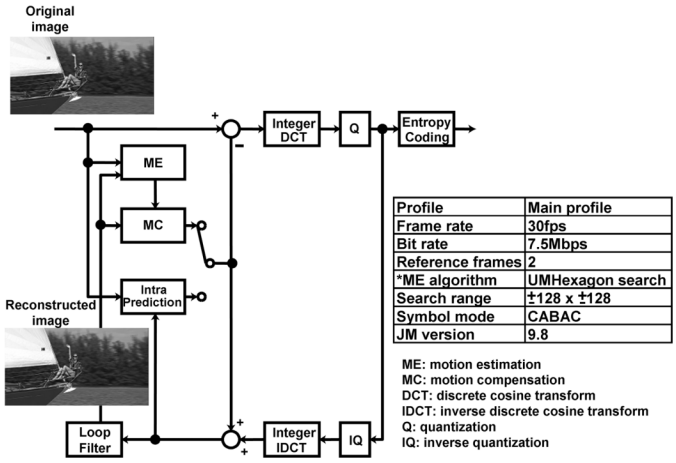


Fig. 7. H.264 encoding process and simulation conditions.

significant bit groups tend to have "0"s, as pointed out in the Section II. For that reason, we chose "1" as a flag bit. The correlation becomes weaker for less significant bits. The distribution in the LSB group (the rearranged LSBs in Fig. 4) is normally distributed (strictly, it is a binominal distribution); similar tendencies are visible even in the first- and second-digit groups.

As discussed in Section II, the power reduction on the RBLs is theoretically expected because of the majority logic even if input data are normally distributed. Besides, further power reduction is promising because the image data are lopsided to "0"s in more significant digit groups, as indicated in Fig. 5. We exploit these features to reduce the RBL power further.

Herein, we designate the rearrangement of the digits "data-bit reordering." Fig. 6 shows the combination of data-bit reordering and the majority logic. In a write cycle, data comprised of m pixels (8 mbits) are reordered in each digit group. The appropriate value of m is discussed in Section III-B. If the number of "0"s in a digit group is equal to or larger than that of "1"s, i.e., if the number of "0"s is equal to or larger than $m/2$, the bits in the digit group are inverted. Alternatively, if the number of "0"s is smaller than that of "1"s, they are not inverted. The majority logic and data-bit reordering maximize the number of "1"s in image data and optimize the RBL power.

In a read cycle, the optimized data are either inverted or not inverted according to a flag bit in a digit group. If a flag bit is "1," the data are inverted; then the reordered bits are put back to the original pixel data.

B. Selection of Value of m

To select the appropriate value of m, we carried out statistical analysis using the original images and reconstructed images extracted from ten H.264 HDTV test sequences: "Bronze with Credit" (Bronze), "Building along the Canal" (Canal), "Church" (Church), "Intersection" (Inters), "Japanese Room" (Jpnroom), "European Market" (Market), "Yachting" (Sail), "Street Car" (Stcar), "Whale Show" (Whale), and "Yacht Harbor" (Yacht). Although pixel data are segmented every m pixels, data-bit reordering does not cause an addressing problem because contiguous pixels are processed simultaneously in a video memory. The original image is encoded, and then a reconstructed image is generated in a local decoding loop. The encoding configuration in H.264 is shown in Fig. 7. The reconstructed image is utilized for motion estimation and motion compensation. For motion estimation, a motion vector between an original and a reconstructed images is calculated. Then the motion vector is used to make another reconstructed image in the motion compensation. The motion estimation requires much computation cost in H.264 real-time encoding, which accounts for 90% or more of the overall workload [3].

Fig. 8 depicts the normalized RBL powers in comparison to those of the conventional two-port SRAM. For these comparisons, it is assumed that the additional power for the flag bit in the proposed SRAM is as much as a power on one RBL. Fig. 8(a) shows a case in which the original image is used as input data. The majority logic is applied only to a set of pixels; data-bit reordering is not applied. The number of pixels to which the majority logic is applied, is varied (one, two, and four pixels). Fig. 8(a) shows that, on average, 20% of the RBL power can be saved using only the majority logic, even though the flag bit is appended.

As presented in Fig. 8(b), the saving factor is further extended to 43% with both the majority logic and data-bit reordering in the case of $m = 16$, which indicates that the statistical characteristics of image data are well exploited. Moreover, as exhibited in Fig. 8(c), maximum power reduction is achieved when the

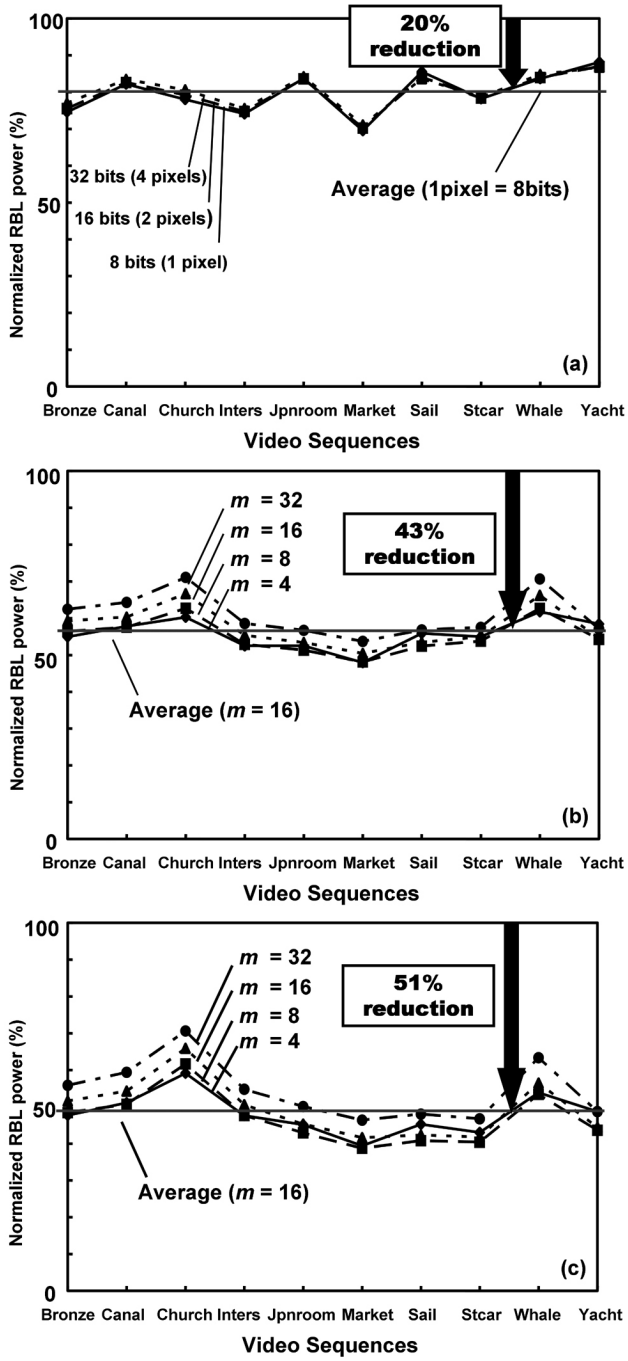


Fig. 8. Normalized RBL powers in (a) the original image only with majority logic, (b) the original image with both majority logic and data-bit reordering, and (c) the reconstructed image with both majority logic and data bit reordering. For this figure, 100% denotes a case of the conventional two-port SRAM.

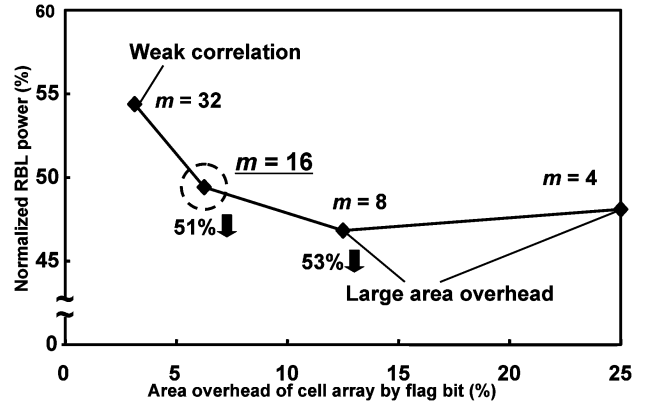


Fig. 9. Normalized RBL power versus area overhead of a memory cell in the proposed SRAM used as a reconstructed-image memory. The area overhead is $1/m$ because the flag bit is appended to every m bits.

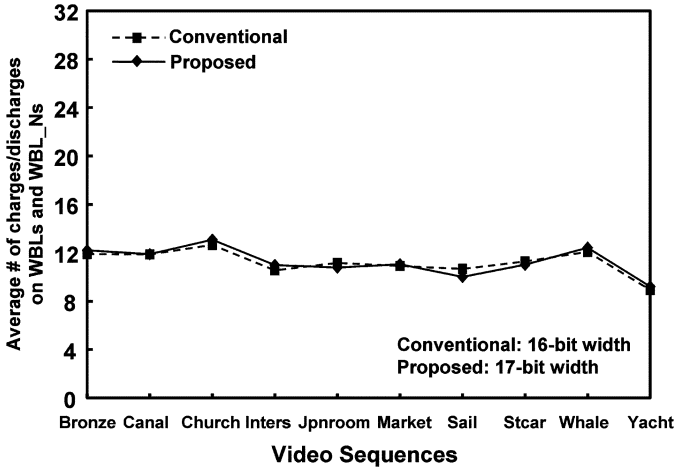
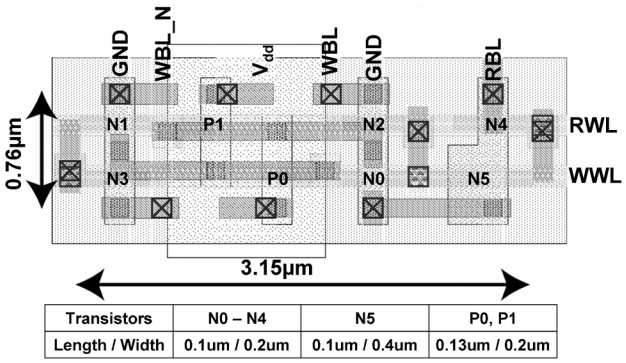


Fig. 10. Number of toggles on WBLs and WBL_Ns in a write cycle.

proposed SRAM is utilized for a reconstructed image that has a stronger correlation than the original image: 51% reduction of the RBL power is achievable. The proposed SRAM is suitable for use as a real-time video encoder such as MPEG2, MPEG4, and H.264, which require a large-capacity reconstructed-image memory for motion estimation. In reality, the power reduction is dependent on test sequences. However, even in the worst-case sequence, "Church," which has weak correlation in data, 35% reduction in the RBL power is achieved when $m = 16$; in the best case, it is possible to reduce 58% of the RBL power in "Market." Even if data have no correlation, i.e., they are totally random, 18% of the RBL power can be saved through use of the majority logic, as described in Section II.

Fig. 9 shows the relationship between the RBL power and the area overhead of a memory cell array caused by the flag bit. In fact, m is a parameter. In both cases of the original image and the reconstructed image, $m = 8$ is optimum in terms of RBL power reduction. The area overhead becomes large if m is small. As m is increased, the area overhead shrinks, but the RBL power increases because the correlation in a digit group becomes weaker for larger m. We choose $m = 16$ as a design choice. The area overhead is 6.3%; it is suppressed to less than 10% when $m = 16$. $m = 4$ and $m = 8$ are obviated as design choices because of their respective large area overheads.

Fig. 10 shows the average number of charges/discharges on write bitlines [refer WBL and WBL_N in Fig. 1(a)] in a write cycle. Since there are no precharge transistors on WBLs and WBL_Ns, they do not consume any power as far as same data are successively written. From this point of view, the statistical characteristic of image data helps to save the write-bitline power. Even though the bit width is increased to 17 by a flag bit, the reduction factor of the write-bitline power in the proposed SRAM is as same as that of the conventional one, thanks



Transistors	N0 – N4	N5	P0, P1
Length / Width	0.1um / 0.2um	0.1um / 0.4um	0.13um / 0.2um

Fig. 11. Memory cell layout.

to the majority logic. Consequently, the proposed SRAM has no power overhead on the write bitlines.

IV. Design in 90-nm Process

A. Memory Cell

Fig. 11 shows a layout of the proposed two-port SRAM cell in a 90-nm process. In addition, the transistor sizes are shown in the figure. The cell area is $3.15 \times 0.76\ \mu\text{m}^2$. The schematic has been already shown in Fig. 1(a). We need not to consider a static noise margin in read operations because of a separate read port and no issue on half selection (half selection means a situation in which a write wordline (WWL) is turned on but WBL and WBL_N are uncertain, which takes place in write operations [8]). Refer WWL in Fig. 1(a) in the proposed SRAM cell. The driver transistor (N0 and N1) widths can be minimized, and the load transistors (P0 and P1) lengths can be increased in order to extend a write margin. Hence, the read and write operating margins are sufficient in our designed SRAM. The divided-wordline structure [9] or transistor resizing is required if the half-selection problem have to be considered.

B. Write/Read Circuitry With Majority Logic

Fig. 12 illustrates a block diagram of the proposed SRAM, where a capacity of memory cells is 68-kbits. As described in Section IV-A, $m = 16$ is chosen in this design. Consequently, 64 kbits are for data themselves; the other 4 kbits are the flag bits. A hierarchical RBL structure [6], [7] is applied to avoid a speed overhead of the single bitline scheme. WBLs and WBL_Ns do not have precharge transistors because they are dedicated for data write-in.

A write circuit should have a majority-logic circuit. However, 70 logic gates would be needed for a 16-bit majority-logic circuits if it was designed with a digital cell library [10], [11], which might result in a large area overhead. Fig. 13 portrays the proposed write circuit with the majority logic. The majority-logic circuit is based on a precharge logic like a domino circuit. The majority logic is evaluated by the pull-down networks connecting to the flip-flops (FFs). Both JL and JL_N are common lines connecting the pull-down networks. The flag bit value is determined by comparing the numbers of sink paths between JL and JL_N. If a straightforward implementation of the 16-bit majority logic was applied, it would require 16 pull-down networks and the voltage difference between JL and JL_N would become smaller. In our proposed circuit, the AND gates reduce the number of pull-down networks to eight and enlarge the voltage difference. Then, the sense amplifier senses the voltage difference between JL and JL_N. For proper timing, the NAND gate for the SE signal is sized carefully. The pMOSs in the NAND gate are widened to achieve the proper timing. Note that, for testing, there is a multiplexer (MUX) just after the sense amplifier to control the flag bit. Arbitrary values can be written to all memory cells, including the flag bits by TEST and Flag_test signals.

If the number of "1"s is seven and the number of "0"s is nine, the number of sink paths on JL is at least one. Fig. 14(a) depicts the operation waveforms in this case at the typical process corner (CC corner) and 25 °C. The number of sink paths on JL_N is zero. Hence, JL_N remains V_{dd}, which is the best condition for the sense amplifier. The sense enable (SE) signal rises gently, and there is a sufficient voltage difference (670 mV) between JL and JL_N at the rising edge. The output signal, Flag, is delayed by the self-timed SE signal, but that is unimportant.

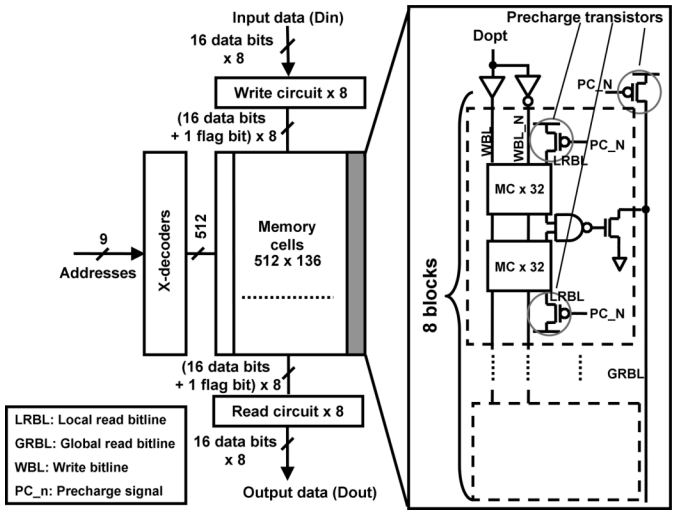


Fig. 12. Block diagram of the proposed 68-kbit SRAM.

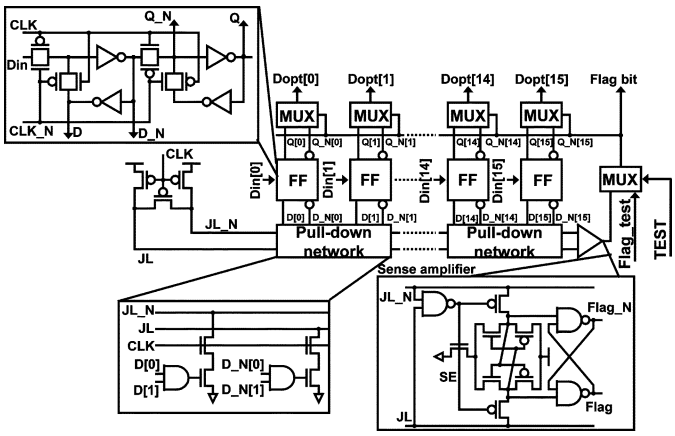


Fig. 13. Write circuit with majority logic.

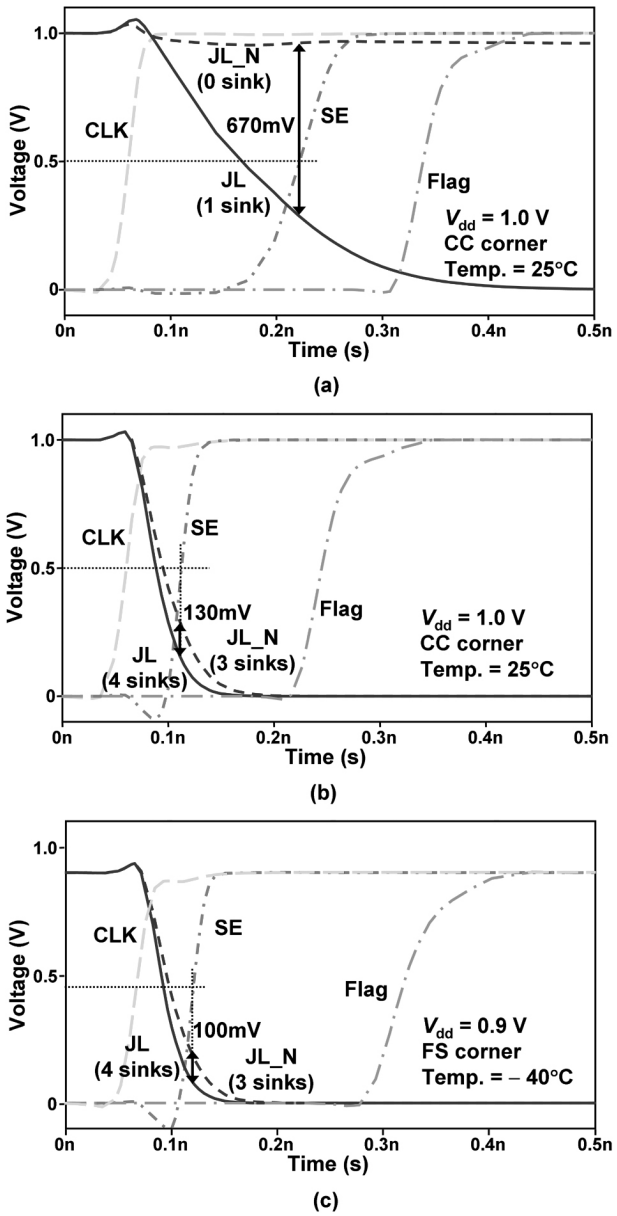


Fig. 14. Operation waveforms in a write circuit for which the numbers of "1"s and "0"s are seven and nine, respectively: (a) the case with one sink path on JL and zero sink path on JL_N; (b) the case with four sink paths on JL and three sink paths on JL_N; (c) the case with four sink paths on JL and three sink paths on JL_N at the worst-case PVT variation.

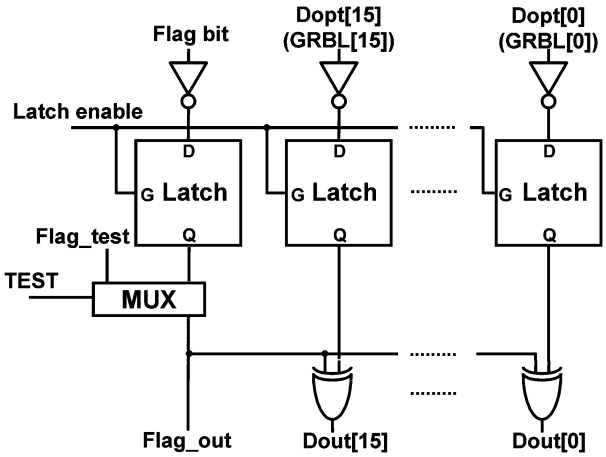


Fig. 15. Read circuit that resumes the original data.

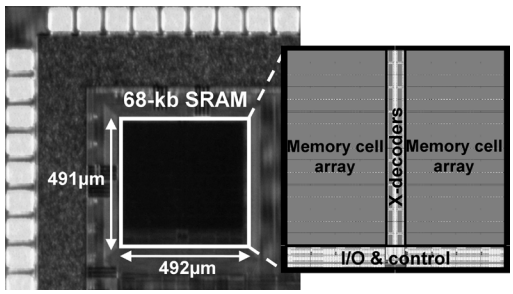


Fig. 16. Chip micrograph and its layout.

The majority-logic circuit, including the testing circuit, is not on the critical path in the write operation. The X-decoder is on the critical path and WWL is slower than Flag.

On the other hand, the worst condition for the sense amplifier is the case in which the numbers of sink paths on JL and JL_N are, respectively, four and three, respectively. Fig. 14(b) corresponds to this case at the CC corner. The SE signal rises steeply, and the voltage difference between JL and JL_N is 130 mV. This voltage difference is, however, sufficient for the sense amplifier to be operated properly. Considering PVT variation, the situation is further worsened. Fig. 14(c) shows the operation waveforms at the FS corner, 0.9 V, and -40 °C. Even in this worst case of the PVT variation, the voltage difference between JL and JL_N is still 100 mV, which is sufficient to be amplified.

If the numbers of "1"s and "0"s are the same, the numbers of sink paths on JL and JL_N become the same. Consequently, the voltage difference is theoretically zero (metastable). In this case, it remains uncertain which is output as Flag, but the flag bit is fixed to either "1" or "0" by the reset-set FF. This uncertainty might degrade the saving factor by the majority logic, although the readout operation is guaranteed in any event.

Fig. 15 is a read circuit that resumes the original data, which inverts data bits depending on a flag bit. The conditional inversion is implemented with EX-ORs. For all-bit testing, Flag_out can be read out as well as $D_{\rm out}$ [15] to $D_{\rm out}$ [0]. It is possible to read out all memory cells including the flag bits by using the test signals (TEST and Flag_test).

V. Measurement Results

Fig. 16 shows a chip micrograph of the proposed 68-kbit SRAM designed in a 90-nm CMOS process. The conventional and proposed SRAMs were both fabricated for comparison. The additional area overhead derived from the flag bits, majority-logic circuit, and EX-ORs in the read circuit is 7%. The measured minimum access time is 3.3 ns at a supply voltage 1.0 V in the proposed SRAM, whereas it is 3.2 ns in the conventional SRAM. The speed overhead of 0.1 ns is caused by the testing MUX and the EX-OR in the read circuit.

Fig. 17 shows the measurement result of leakage current per memory cell. Since a "1" storage cell ($V0 =$ "1" and $V1 =$

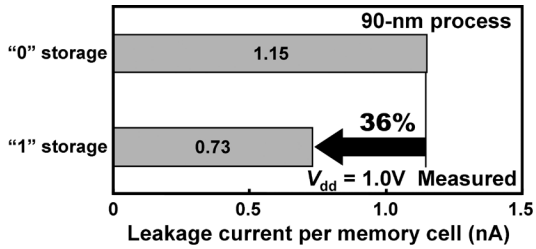


Fig. 17. Measured leakage current per memory cell.

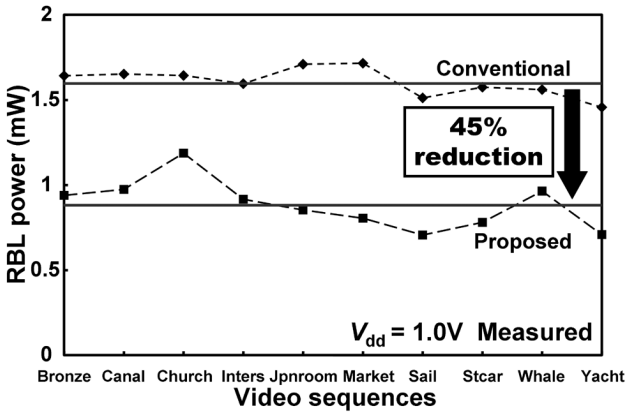


Fig. 18. Measured RBL power in 100-MHz operation.

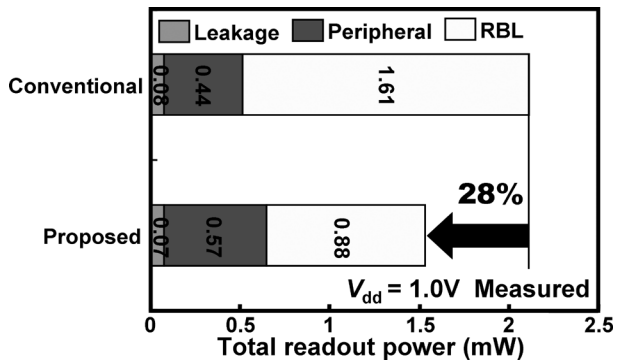


Fig. 19. Total readout power in 100-MHz operation.

"0") reduces the gate leakage at N4 and the bitline leakage from the RBL [see Fig. 1(a)], the total leakage current in a "1" storage cell is 36% smaller than that in a "0" storage cell. We can maximize the number of "1"s using the majority logic. Consequently, the proposed SRAM can reduce the leakage power as well as the charge/discharge power.

Fig. 18 shows the measured RBL powers at the nominal supply voltage of 1.0 V and a frequency of 100 MHz. We verified the 45% of the RBL power is saved on average in the reconstructed images of the ten video sequences. The saving factor differs somewhat from the simulation result in Fig. 8(c) since the additional power for the flag bit is 1.6 times larger than a power on one RBL because of the EX-ORs in the read circuit. In the simulation, it was assumed to be as much as a power on one RBL. Moreover, if the numbers of "1"s and "0"s are equal in the reordered data, the value of the flag bit is uncertain, which possibly degrades the saving factor.

In Fig. 19, the measured readout power in the proposed SRAM, including the power of the peripheral circuits and leakage power, is exhibited along with that of the conventional SRAM case. In a video memory, power reduction in a read operation is technically more important because readouts are made more frequently than write-ins. Even in the total readout power, our proposed SRAM saves 28% over the conventional SRAM.

VI. Conclusion

We proposed a novel two-port SRAM using majority logic and data-bit reordering. The proposed SRAM is suitable for real-time image processing for statistically similar data. The measurement result in a 68-kbit SRAM verifies a power saving of 45% on read bitlines. The total readout power is reduced by 28%. The speed and area overheads are 4% and 7%, respectively.

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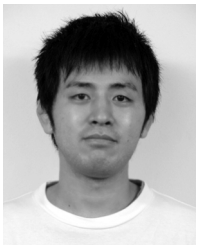
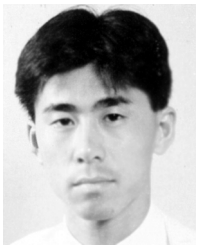


Hidehiro Fujiwara (S'06) received the B.E. and M.E. degrees in computer and systems engineering from Kobe University, Hyogo, Japan, in 2005 and 2006, respectively, where he is currently pursuing the Ph.D. degree in engineering.

His current research interests include high-performance and low-power SRAM designs.



Koji Nii (M'00) received the B.E. and M.E. degrees in electrical engineering from Tokushima University, Tokushima, Japan, in 1988 and 1990, respectively. He is currently pursuing the Ph.D. degree in engineering from Kobe University, Hyogo, Japan.

In 1990, he joined the ASIC Design Engineering Center, Mitsubishi Electric Corporation, Itami, Japan. In 2003, Renesas Technology made start. He currently works on the research and development of 45-nm embedded SRAM in the Design Technology Division, Renesas Technology Corp., Hyogo, Japan.

Mr. Nii is a member of the IEEE Solid-State Circuits Society and IEEE Electron Devices Society.

Hiroki Noguchi received the B.E. degree in computer and systems engineering from Kobe University, Hyogo, Japan, in 2006. He is currently pursuing the M.E. degree in engineering.

His current research interests include high-performance and low-power SRAM designs.

Junichi Miyakoshi received the B.S. and M.S. degrees from Kanazawa University, Ishikawa, Japan, in 2002 and 2004, respectively. He is currently pursuing the Ph.D. degree in engineering from Kobe University, Hyogo, Japan.

His research interests include low-power VLSI techniques for image processing.

Yuichiro Murachi was born on November 1, 1980. He received the B.S. and M.E. degrees from Kanazawa University, Ishikawa, Japan, in 2003 and 2005, respectively. He is currently pursuing the Ph.D. degree in engineering from Kobe University, Hyogo, Japan.

His research interests include VLSI systems and implementation of multimedia communication systems.

Yasuhiro Morita (S'05) received the M.E. degree in electronics and computer science from Kanazawa University, Ishikawa, Japan, in 2005. He is currently pursuing the Ph.D. degree in engineering from Kobe University, Hyogo, Japan.

His current research interests include high-performance and low-power multimedia VLSI designs.

Hiroshi Kawaguchi (M'98) received the B.E. and M.E. degrees in electronic engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and the Ph.D. degree in engineering from the University of Tokyo, Tokyo, Japan, in 2006.

He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to the Institute of Industrial Science, the University of Tokyo, as a Technical Associate in 1996, and was appointed a Research Associate in 2003. In 2005, he moved to the Department of Computer and Systems Engineering, Kobe University, Kobe, Japan, as a Research Associate. Since 2007, he has been an Associate Professor with the Department of Computer Science and Systems Engineering, Kobe University. He is also a Collaborative Researcher with the Institute of Industrial Science, the University of Tokyo. His current research interests include low-power VLSI design, hardware design for wireless sensor network, and recognition processor.

Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Program Committee Member for IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*. He is a member of the ACM.

Masahiko Yoshimoto received the B.S. degree in electronic engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1975, and the M.S. degree in electronic engineering and the Ph.D. degree in electrical engineering from Nagoya University, Nagoya, Japan, in 1977 and 1998, respectively.

He joined the LSI Laboratory, Mitsubishi Electric Corp., Itami, Japan, in April 1977. From 1978 to 1983, he was engaged in the design of nMOS and CMOS static RAM including a 64 K full CMOS RAM with the world's first divided-word-line structure. From 1984, he was involved in research and development of multimedia ULSI systems for digital broadcasting and digital communication systems based on MPEG2 and MPEG4 Codec LSI core technology. Since 2000, he has been a Professor of the Department of Electrical and Electronic Systems Engineering, Kanazawa University, Ishikawa, Japan. Since 2004, he has been a Professor with the Department of Computer and Systems Engineering, Kobe University, Kobe, Japan. His current research activity is focused on research and development of multimedia and ubiquitous media VLSI systems including an ultra-low-power image compression processor and a low power wireless interface circuit. He holds 70 registered patents.

Prof. Yoshimoto was a recipient of the R&D100 Awards from R&D Magazine for development of the DISP and development of a realtime MPEG2 video encoder chipset in 1990 and 1996, respectively. He served on the Program Committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. In addition, he has served as a Guest Editor for special issues on Low-Power System LSI, IP, and Related Technologies of IEICE Transactions in 2004.