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PAPER

Row-by-Row Dynamic Source-Line Voltage Control (RRDSV) Scheme for Two Orders of Magnitude Leakage Current Reduction of Sub-1-V-V_{DD} SRAM's

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SUMMARY A new Row-by-Row Dynamic Source-Line Voltage Control (RRDSV) scheme is proposed to suppress leakage current by two orders of magnitude in the SRAM's for sub-70 nm process technology with sub-1-V V_{DD} [10]. This two-order leakage reduction is caused from the cooperation of reverse body-to-source biasing and Drain Induced Barrier Lowering (DIBL) effects. In addition, metal shields are proposed to be inserted between the cell nodes and the bit lines not to allow the cell nodes to be flipped by the external bit-line coupling noise in this paper. A test chip has been fabricated to verify the effectiveness of the RRDSV scheme with the metal shields by using 0.18-μm CMOS process. The retention voltages of SRAM's with the metal shields are measured to be improved by as much as 40–60 mV without losing the stored data compared to the SRAM's without the shields.

key words: *low-voltage SRAM, low-power SRAM, row-by-row, low-leakage, leakage reduction technique, leakage suppression technique, subthreshold current*

1. Introduction

As the supply voltage (V_{DD}) in the circuit decreases, the threshold voltage (V_{TH}) should also be lowered not to degrade the operating speed of the circuit. Decreasing V_{TH} by as small as 0.1 V increases the subthreshold leakage by more than one order of magnitude. For example, in 70-nm process technology, its subthreshold leakage is expected to reach 40 nA/μm at 25°C [1]. If one million gates in a chip are assumed to be used, total leakage current as much as 40 mA would flow into the ground even though the chip does not consume any dynamic power in the sleep mode. Usually the cache memory which is basically SRAM occupies a largest area among many internal various IP's in the SoC. Moreover, its portion in the chip area is more and more increasing as the number of transistors in the SoC increases [2]. Hence, if this large leakage in the SRAM is not suppressed, this should be a serious energy sink not only in coming sub-70-nm leakage-dominant era but also in the recent 130-nm process technology. In addition, it should also be noted here that the leakage power would be dominant over the dynamic one even in the active mode with sub-70-nm process [3]. For example, in the 70-nm technology, the leakage power consumption is expected to be about 10 times larger than the dynamic one [4].

Many techniques have been proposed to suppress the leakage current in the SRAM's [3]–[7]. Among them, the one technique is dynamically driving the bulk voltage of sleep cells to control their V_{TH}'s [5]. When a memory row is accessed, it is activated by driving V_{DD} and V_{SS} to its n-well and p-well, respectively. When the row becomes sleep, its n-well and p-well are driven by $2V_{DD}$ and $-V_{DD}$ to increase their $|V_{TH}|$'s, respectively. Though this scheme can reduce the leakage current of sleep row, it needs a large area penalty since the well of each row should be separated from another row by at least several microns. In addition, changing voltage of n-well and p-well can cause an issue of speed degradation due to large capacitance of the well.

Another technique of Row-by-Row Dynamic V_{DD} (RRDV) scheme has been proposed in [3], where V_{DD} of each row is dynamically controlled to reduce the cell leakage by exploiting the DIBL effect. When this scheme is applied, however, the negative word line should be used to avoid the faulty read operation due to large bit-line leakage. If so, the bit line should be precharged by V_{DD}-V_{TH} not to impose the high voltage stress across the oxide, which in turn reduces the stability of the cell and the write error may occur.

In this paper, a new Row-by-Row Dynamic Source-line Voltage control (RRDSV) technique is proposed, where the source line shared by neighboring cells is dynamically driven by voltage higher than V_{SS} to reduce the leakage current when the cells are not activated. This source-line voltage higher than V_{SS} can enhance V_{TH}'s of cells by cooperation of the Drain-Induced Barrier Lowering (DIBL) and the reverse body-to-source biasing effects. It should be noted here that this RRDSV scheme is completely different with some other dynamic source-line control schemes. See, for example, Ref. [6], where the cell is made with high-V_{TH} device to reduce its leakage, even if V_{DD} is below 1 V. To compensate the speed degradation in [6], the source line is driven to be negative when its cells become active, while im-

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posing higher voltage stress than V_{DD} across the gate oxide. Another technique called by the gated-ground scheme has also been proposed in [4], where an NMOS is inserted between the real V_{SS} line and the source line of cells. Here the NMOS cut-off switch in [4] is turned off by V_{SS}, when the cells become sleep, resulting in reducing the leakage only by 50% [4]. This amount of leakage reduction is not enough to be used in future CMOS technology, where the leakage power is expected to be dominant over the dynamic one. The leakage power consumption in future 70-nm technology is expected to be ∼10 times larger than its dynamic one [4]. So, the leakage power should be reduced by more than two orders of magnitude than the conventional SRAM without any leakage suppression scheme.

Unlike the gated-ground scheme [4], the source-line driver instead of the simple NMOS switch in [4] is driven by negative voltage in this RRDSV scheme when its cells are sleep. Here the NMOS switch becomes turned off by negative V_{GS} and the 'ON' PMOS switch drives the source line by V_{SSH}, eliminating the situation of high impedance. By doing so, the retention voltage can be reduced to be almost ∼ V_{TH}, achieving the subthreshold current suppression by two orders of magnitude which is much larger than the reduction in [4]. One more thing to note here is that metal shields should be inserted to protect cell nodes which are represented by 'Q' and 'QB' nodes in Fig. 1 from the external bit-line coupling noise in this RRDSV scheme. Lowering the retention voltage to reduce the leakage has also been proposed in [8] and [9], where the subthreshold current could be successfully suppressed to 3.9% compared with the conventional SRAM when V_{DD} =1.5 V [8]. In [8], the source-line voltage is increased from the ground potential at the active mode to 0.5 V at the sleep by inserting the diode-connected MOSFET's between the cells and power lines. Since voltage drops at the diode-connected MOSFET's are very sensitive to the V_{TH} fluctuation, the retention voltage can be much reduced so at to destruct their stored data. This will be more serious as V_{DD} goes smaller with the device scaling, since the V_{TH} fluctuation will not be scaled down but even goes larger with the scaling. Moreover, the stored data with lowered retention voltage are so susceptive to external noise that a shielding method should be accompanied with these low retention-voltage techniques, which has not been discussed in [8] and [9].

An SRAM test chip with 16-k bits has been fabricated in 0.18-μm triple-well CMOS technology to verify the effectiveness of the RRDSV scheme on the leakage reduction and the noise protection. The measured result will be shown at Sect. 4.

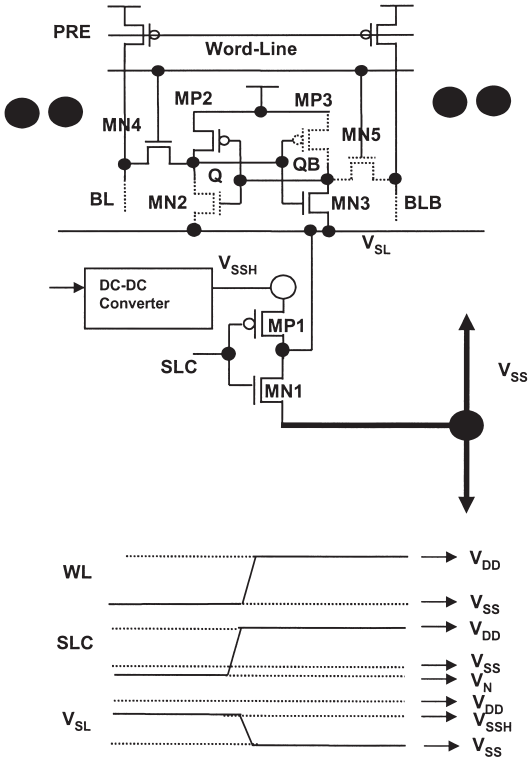


Fig. 1 Schematic diagram of RRDSV scheme with the source line shared by neighboring 4 cells.

2. RRDSV Scheme for Leakage Reduction

Figure 1 shows a schematic diagram of the proposed RRDSV scheme. Here, the V_{SL} represents the source-line voltage. The MN1 and MP1 in Fig. 1 represent the source-line driver for driving the source line according to the input signal of 'SLC.' Here V_{SSH} is a voltage lower than V_{DD} and can be generated by a high-efficiency DC-DC converter. As you can see in Fig. 1, several cells can share one source line which is driven by its source-line driver. In this paper, one source line is designed to be shared by neighboring 4 cells, as shown in Fig. 1. If more cells, for example, 8 or 16 cells, share one source line, the area penalty due to the source-line driver which should be added to the conventional cell array goes better. Simultaneously, however, the V_{SS} current through the shared source line will increase significantly, causing the reliability problem such as the electromigration and large IR drop problems. In addition, read access delay may go longer than the RRDSV scheme with the source-line shared by neighboring 4 cells. In the practical SRAM design, the V_{SS} lines should be perpendicular to word lines and horizontal to bit lines to avoid the electromigration and IR drop problems. Like the practical SRAM design, the V_{SS} line goes vertically here, being switched to the source line via the source-line driver when the cells are accessed, as shown in Fig. 1. And, since the number of cells that share the source line is decided by 4 in this work, the read current is not so much increased as to arouse the reliability issue and to degrade the read access delay severely.

Assume that nodes 'Q' and 'QB' in Fig. 1 are high and low, respectively. If so, MN2, MP3, and MN5 become turned off as shown in Fig. 1. In this figure, the 'OFF' MOSFETs are depicted by the dotted line. When all rows are sleep, all source lines are connected to V_{SSH} via their MP1's. When a row becomes active, its source-line volt-

age is switched to V_{SS} via the MN1, while the other source lines remain connected to V_{SSH} via their MP1's, suppressing the leakage through them. Let us see why the leakage current can be suppressed by driving the source line by V_{SSH}. As stated earlier, there are 3 'OFF' MOSFET's. For the MN2, V_{GS}=0 V, V_{BS}=0 V, and V_{DS}=V_{DD}, when V_{SL}=V_{SS}. If V_{SL} is increased to V_{SSH}, V_{DS} and V_{BS} of MN2 go to V_{DD}-V_{SSH} and $-V_{SSH}$, respectively, increasing the V_{TH} by both the DIBL and reverse-body-biasing effects. For the DIBL effect, it is caused by V_{DS} which modulates the potential barrier between the channel and the source. Large V_{DS} can lower this barrier so that the inversion charge from the source can move into the channel more easily than when small V_{DS}. This phenomenon of DIBL can be modeled by increasing value of V_{TH} with decreasing V_{DS} [10].

For MN5, its V_{GS} goes to $-V_{SSH}$ if V_{SL}=V_{SSH}. It causes that the bit-line leakage through the MN5 is decreased by more than 3 orders. Small bit-line leakage is especially important in sub-1-V operation of SRAMs. In this low V_{DD} regime, the V_{TH} as low as 0.1–0.2 V makes the word-line transistors very leaky. The leaky word-line transistors can cause the faulty read operation when the bit-line leakage through them is larger than the cell read current [11]. For the MP3, its $|V_{DS}|$ is decreased from V_{DD} to V_{DD}-V_{SSH}, exploiting the DIBL effect to increase its V_{TH}.

One more issue to be considered here is the source-line driver is driven by negative voltage of V_N when its cells are in the sleep. Value of V_N should be low enough to reduce the subthreshold leakage via the MN1 in Fig. 1 by two orders of magnitude. The negative voltage of V_N can be easily generated by using the conventional charge pump circuits, since its voltage is slightly below V_{SS}. Though the NMOS switch in the source-line driver is turned off by V_N, since the V_{SSH} is below V_{DD}, the voltage stress across the gate oxide of MP1 and MN1 would not exceed V_{DD}.

At next, the role of MP1 should be discussed here. By turning on the MP1 by V_N, the source line is not in high-impedance state but it is forced by V_{SSH} via MP1, when its cells are sleep. Since the high-impedance state is susceptive to the external noise such as the bit-line coupling and soft error, driving V_{SL} by V_{SSH} is helpful in improving the data retention characteristics when the cells are sleep. Figure 2 compares how V_{SL} varies with V_N between with the MP1 and without the MP1. With the MP1, the retention voltage of sleep cells can be kept as large as $|V_{DD} - V_{SSH}|$. As long as this retention voltage is larger than V_{TH}, the data can be restored when the cell is accessed later. Without the MP1, V_{SL} is strongly dependent on V_N. A slight variation of V_N by as small as 0.1 V can increase or decrease V_{SL} by as large as 0.4 V, possibly destroying the stored data.

Figure 3 shows the simulated subthreshold characteristics of future 70-nm NMOSFET, which is from Berkeley Predictive Technology Model (BPTM) [12]. If V_{SL} is increased from V_{SS}=0 V to V_{SSH}=0.7 V when V_{DD}=0.9 V, the subthreshold leakage current can be reduced by as much as two orders of magnitude, as indicated in Fig. 3. This is due to the cooperation of reverse source-to-body biasing, negative gate-to-source basing, and DIBL caused from the decreased drain-to-source bias, as stated earlier. As the devices go scaled down further below 70-nm technology, however, the other leakage currents such as gate-oxide tunneling and Gate-Induced Drain Leakage (GIDL) currents also are observed in addition to the subthreshold current. Because the gate-oxide and GIDL currents are not suppressed by the reverse source-to-body biasing and DIBL effects, the effect of RRDSV scheme can be alleviated. For example, with 45-nm MOSFET parameters which include both the gate-oxide and GIDL currents, the leakage saving of the RRDSV SRAM is estimated to be as large as 70%. Though this 70% reduction in 45-nm RRDVS SRAM is smaller than 99% in 70-nm one, it still demonstrates the effectiveness of the RRSDV scheme in suppressing leakage. The Spice parameters of this 45-nm technology is also from the BPTM site like 70-nm [12]. This smaller leakage reduction with 45-nm parameters also is caused from smaller V_{DD} than 70-nm parameters, since the reverse source-to-body biasing and DIBL effects will go smaller with decreasing V_{DD}. Suppressing the gate-oxide leakage in future sub-70-nm MOSFET's is being an important issue so that various solutions including finding a high-

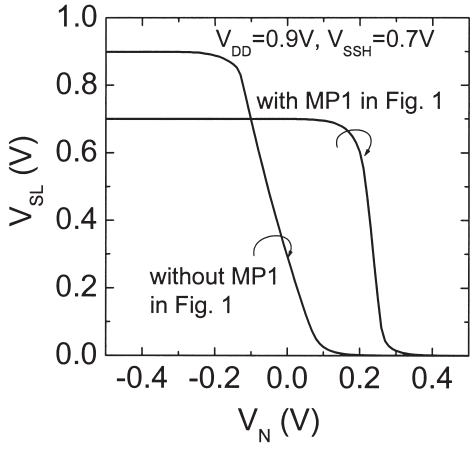


Fig. 2 Plot of V_{SL} with varying V_N with the MP1 in Fig. 1 and without the MP1 in Fig. 1.

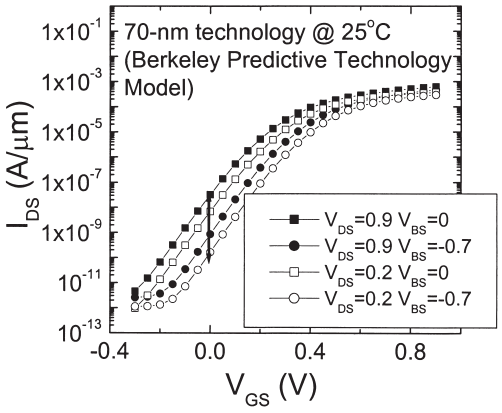


Fig. 3 Subthreshold characteristics of future 70-nm technology predicted in ITRS.

k dielectric are widely being studied not to use a thin and leaky insulator such as SiO_2.

3. Design of SRAM with RRDSV Scheme

Figure 4 shows a voltage level shifter whose output is connected to the source-line driver. This level shifter can drive negative voltage of V_N without arousing a high-voltage stress exceeding V_{DD} in it. Here one level shifter per row is needed to turn off the source-line driver by the negative V_N when the row is sleep. The G1 in Fig. 4 represents the decoder that selects an accessed word line among many word lines according to the input address. The output of G1 is represented by node 'A' in Fig. 4. When a word line is selected, the node 'A' goes to V_{DD} from V_{SS} and the output node 'B' of G2 goes to V_{SS} from V_{SSH}. It should be noted here that the MN in Fig. 4 may be leaky since its V_{GS} is larger than V_{SS} when it is turned off. This leakage current, however, can be neglected because only one row is activated at one time while the others are all sleep. Making MN with high-V_{TH} NMOS in Fig. 4 can eliminate this leaky turn-off problem of the MN. In this case, the speed degradation due to high-V_{TH} MN in Fig. 4 will not occur at the sleep-to-active transition but at the active-to-sleep transition. The active-to-sleep transition does not have an effect on the data access time, even though it takes long. Finally, for the negative voltage of V_N, it can be generated from various charge pumps such as the recently proposed with high pumping efficiency and large output current [13] or it can also be supplied from the external voltage source. In the case of using the internal pumps, only one source-line driver at one time is forced by V_{DD} and the remains all keep V_N so that they act as very large capacitive reservoir which stores negative voltage of V_N. They can minimize the area overhead due to adding the negative voltage generator since a large layout area for the capacitive reservoir can be saved.

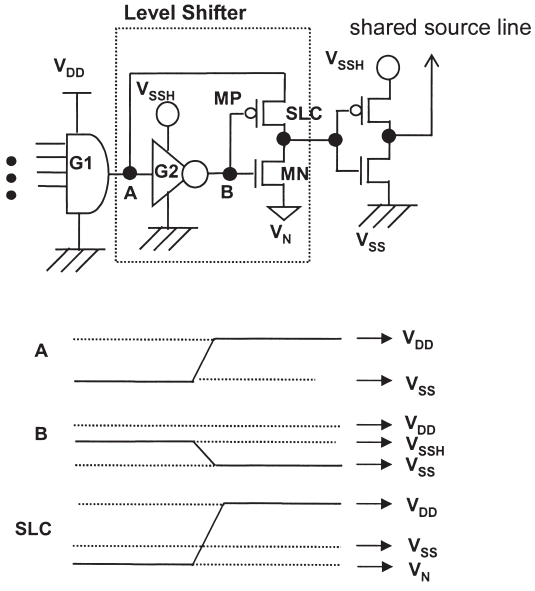


Fig. 4 Level shifter without the high voltage stress.

Figure 5 indicates the normalized read-out delay with varying the size of MN1 in the source-line driver, which is shown in Fig. 1. Here, 'N' in x-axis in Fig. 5 represents the number of cells sharing the source-line driver. W_{MN1} and W_{MN2} are the width of MN1 in the source-line driver and the width of MN2 in Fig. 1, respectively. Here the read-out delay time is defined by the time when the potential difference between BL and BLB (ΔV_{BL}) in Fig. 1 reaches as large as 200 mV. As you can see in Fig. 5, the read-out delay is sharply increasing when $W_{MN1}/(N * W_{MN2})$ decreases below 0.5. When 'N' is 4, $W_{MN1}/(N * W_{MN2})$ can be calculated with 0.5 and this corresponds to 4% overhead in the read-out delay and 25% overhead in the cell area. If this number of 'N' increases to 8, $W_{MN1}/(N * W_{MN2})$ corresponds to 0.25 with 6% of the delay penalty and 12.5% of the area one. To avoid this severe delay degradation as much as 6% in the read access, 'N' is decided by 4 in this paper but this number of cells sharing one source-line driver can be increased or decreased by the trade-offs between the read-out delay and the area penalty. How to decide an optimum value of 'N' strongly depends on the specification of the read speed and allowed chip area. Similarly, value of V_{SSH} can also be determined by the trade-offs between the leakage power saving and switching power overhead. As V_{SSH} becomes higher, larger switching current is consumed to charge the source line to V_{SSH} at the active-to-sleep transition. Simultaneously, however, less leakage current dissipates in the sleep cells as V_{SSH} goes higher.

Figure 6(a) shows the array architecture, where neighboring 4 cells are shown to share one source-line driver [14]. Here the area penalty due to this added source-line driver is estimated by 25% so that the total penalty including the peripheral circuits is thought to be 12.5% since the peripheral circuits usually take the same area with the cell array. Though this penalty can be alleviated as the number of cells sharing one source line increases, the V_{SS} current will increases, introducing the reliability problems such as the electromigration and large IR drop, and the longer read-out delay. To avoid these problems, the number of cells sharing

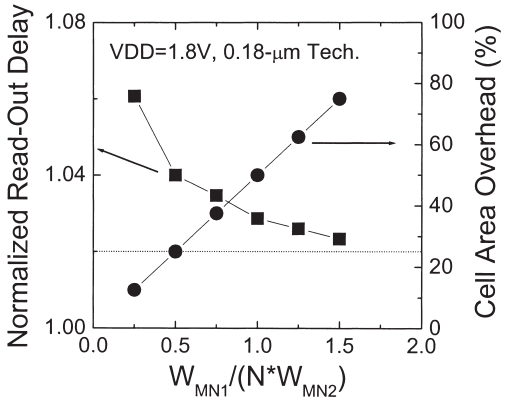
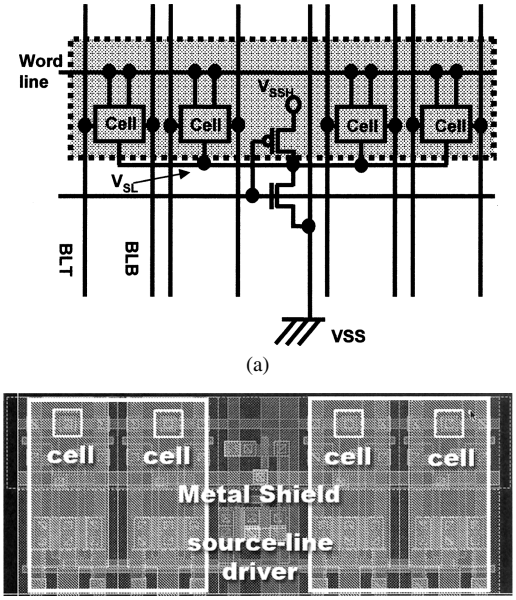


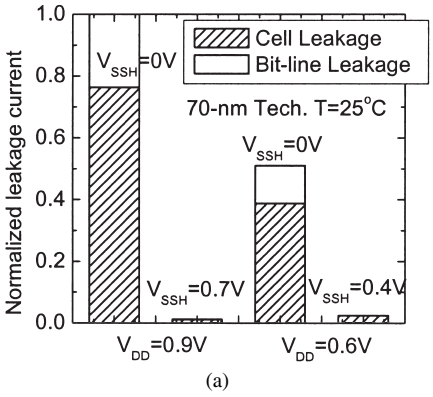
Fig. 5 Normalized read-out delay with varying NMOS size of source-line driver shown in Fig. 1.



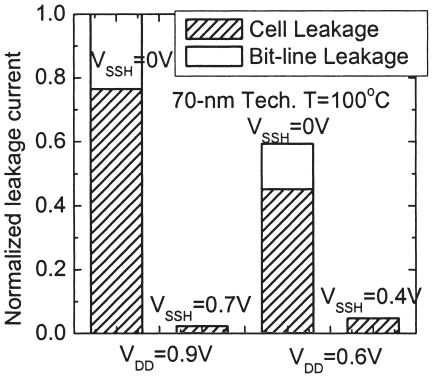
(a)

(b)

Fig. 6 (a) Array configuration of RRDSV scheme, where the dotted region represents that the cells are shielded by the metal layer to protect their cell nodes with small retention voltage from the bit-line coupling noise (b) Layout view of four cells with one source-line driver. Here the shielded area is indicated by white solid line.



(a)



(b)

Fig. 7 (a) Leakage comparison between the conventional SRAM and RRDSV-SRAM at T = 25°C (b) Leakage comparison between the conventional SRAM and RRDSV-SRAM at T = 100°C.

one source-line driver is decided by 4 in this paper as stated earlier. Each source-line driver is connected to its dedicated real V_{SS} line, which is perpendicular to the word lines [9]. Since the word line is activated row by row, each source-line driver which belongs to the selected row draws the read current into its dedicated real V_{SS} lines, respectively.

Another issue that should be considered in the SRAM array design is how to suppress the noise. Since the retention voltage of sleep cells is reduced to be as small as $\sim V_{TH}$, nodes Q and QB in Fig. 1 become very susceptive to the external noise such as the bit-line coupling. To avoid this coupling noise, metal shields are inserted between the cell nodes and the bit lines as shown in the gray region in Fig. 6(a). The layout view of Fig. 6(a) is shown in Fig. 6(b), where the shielded area is drawn by white solid line. There are total four cells and one source-line driver between left-side two cells and right-side two cells in Fig. 6(b). In this figure, total 4 metal layers are used to draw the local interconnections, the metal shields, the bit lines, and the word lines, respectively. Since the shields are drawn by the second-layer metal and in between the cell areas drawn by the first metal and upper bit lines by the third metal, they do not need additional area so that their penalty can be negligible as shown in Fig. 6(b).

4. Simulation and Measurement

Figure 7 shows how much the subthreshold leakage would be reduced by using the RRDSV scheme in future 70-nm technology with sub-1-V V_{DD}. The Spice model parameters used in this estimation are from Berkeley Predictive MOSFET Technology Model (BPTM) [12]. From this figure, it is expected that the leakage with the RRDSV scheme is suppressed to be 1/100 than the conventional SRAM scheme when V_{DD}=0.9 V and V_{SSH}=0.7 V. When V_{DD}=0.6 V and V_{SSH}=0.4 V, the leakage with the RRDSV scheme goes smaller to be 1/20. This is because the reverse source-to-body voltage becomes smaller from 0.7 V to 0.4 V. A drastic leakage reduction can be observed at the bit lines which are represented by BL and BLB in Fig. 1. Since the gate-to-source voltage of the pass transistor of MN5 in Fig. 1 becomes negative by increasing its source-line voltage, its leakage is reduced by more than 3 orders as you can see in Fig. 7. When the temperature is 100°C, the leakage current is shown to be reduced to 1/50 with V_{DD}=0.9 V and V_{SSH}=0.7 V.

One more thing to consider here is that there is a dynamic power overhead in this RRDSV scheme since the additional switching power is consumed in controlling the source-line driver and driving its source line by V_{SSH}. This switching power overhead should be compared with the leakage power saving to verify the effectiveness of the RRDSV scheme. The comparison is done in Fig. 8, where the x axis and y axis represent the frequency of active-to-sleep transition and the power consumption, respectively. In Fig. 8, the conventional SRAM seems to consume the power more than 100 times than the RRDVS SRAM due to its

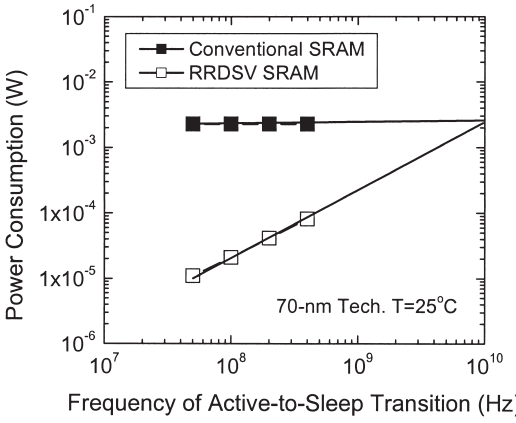


Fig. 8 Power consumption vs. frequency of active-to-sleep transition.

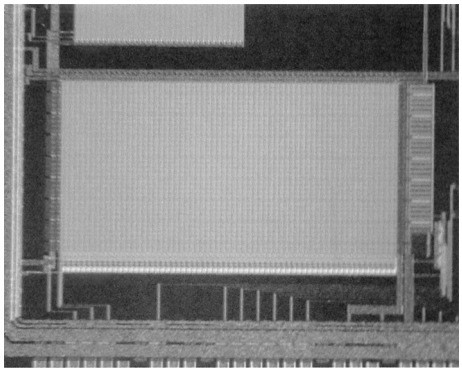


Fig. 9 Chip micrograph of the fabricated 16-K SRAM.

large leakage current with f=100 MHz. This discrepancy goes smaller with increasing the frequency of the active-to-sleep transition, since the switching power overhead becomes larger with increasing this frequency. Two lines for the conventional SRAM and the RRDSV SRAM in Fig. 8 which meet each other near at f=10 GHz indicate that the leakage power saving in the RRDSV scheme still dominates over the switching overhead until 10 GHz of the frequency. Here, it is assumed that 2043 rows are in sleep while one row is accessed. If the number of sleep rows becomes larger than this while only one row is activated, the crossover frequency at which the leakage saving is equal to the switching overhead will go higher, extending the effectiveness of the RRDSV scheme.

The SRAM with this RRDSV scheme was fabricated in 0.18-μm CMOS technology. Figure 9 shows the chip micrograph of the fabricated SRAM array with 128 × 16 × 8 bits. The characteristics of the fabricated SRAMs with this RRDSV scheme are summarized in Table 1, where V_{DD} = 1.8 V, V_{SSH} = 1.5 V, and the macro size with 4 cells and one source-line driver is 16.025 × 9.07 [μm^2]. The dynamic power consumption with the fabricated SRAMs is measured by 4.8 mW with the clock frequency of 100 MHz in Table 1. For the stand-by leakage, the stand-by current is simulated to be decreased from 564.6 pA/cell in the conventional SRAM to 58.6 pA/cell in the RRDSV SRAM in case

Table 1 Characteristics of 0.18-μm CMOS SRAM.

$V_{DD}/V_{SS}/V_{SSH}$	1.8V/0.0V/1.5V
Fabrication process technology	0.18-μm CMOS Triple well
Macro size with 4 cells and 1 source-line driver	16.025×9.07 [μm²]
Simulated stand-by current per cell (Conventional/RRDSV scheme)	28.1 pA/9.9 pA @ 25 °C 564.6 pA/58.6 pA @ 100 °C
Measured dynamic power	4.8 mW @ 100MHz

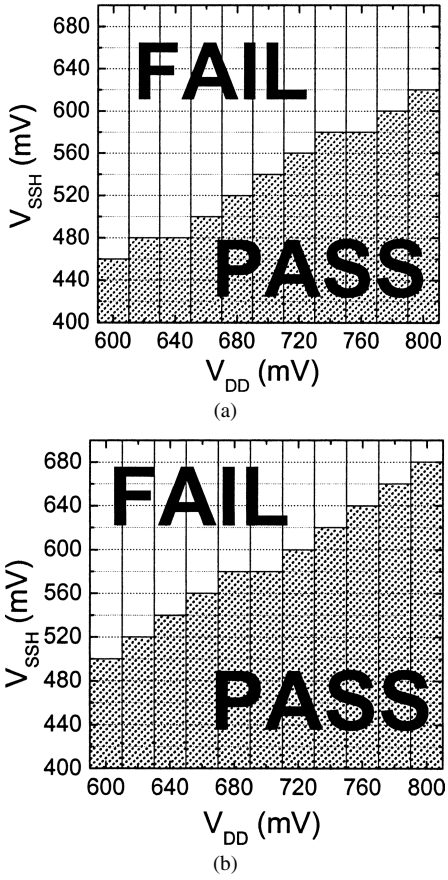


Fig. 10 (a) Measured shmoo plot of SRAM array without bit-line shield when T=25°C (b) Measured shmoo plot of SRAM array with bit-line shield when T=25°C.

of the 0.18-μm technology. Since the amount of subthreshold current in the 0.18-μm technology is much smaller than the 70-nm, its amount of leakage reduction also goes smaller than the 70-nm.

How much the retention voltage can be reduced without losing their stored data is shown in Fig. 10. Here, the x-axis and y-axis represent values of V_{DD} and V_{SSH}, respectively. The shaded region in Fig. 10 indicates that the data can be retained with these V_{DD}'s and V_{SSH}'s while the data on the white region are lost during the sleep time. Here Figs. 10 (a) and (b) are for the RRDSV scheme without the bit-line shield and with the bit-line shield, respectively. The

measurement is done at 25°C. From the measurement, the minimum retention voltage is observed to be in between 100 mV and 200 mV and this value is very comparable to $\sim V_{TH}$. This minimum retention voltage can be more reduced when the metal shield is inserted between cell nodes and bit lines. The inserted metal shield can protect the stored data from being flipped by the external noise. The minimum retention voltage is improved by as much as 60 mV with this metal shield. It can cause the leakage to be more suppressed by another 50% in addition to the two orders of magnitude reduction which was already achieved by the RRDSV scheme.

5. Conclusion

A new RRDSV scheme is proposed to suppress the leakage current by two orders of magnitude in the SRAM for coming sub-70 nm process technology with sub-1-V V_{DD}. By dynamically controlling the source-line voltage of cells row by row, the leakage in sleep cells can be suppressed by two orders without losing their stored data. This two-order leakage reduction is caused from the cooperation of reverse body-to-source biasing and Drain Induced Barrier Lowering (DIBL) effects. In addition, a metal shield is proposed to be inserted between the cell nodes and the bit lines not to allow the cell nodes to be flipped by the external bit-line coupling noise. A test chip has been fabricated to verify the effectiveness of the RRDSV scheme with the metal shield by using 0.18-μm CMOS process. The minimum retention voltage is measured to be improved by as much as 40–60 mV when the metal shield is inserted. It can cause the leakage to be more suppressed by another 50% in addition to the reduction by two orders of magnitude.

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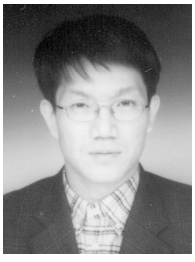
References

[1] International Technology Roadmap for Semiconductors (ITRS99).
[2] T. Sakurai, "Perspectives on power-aware electronics," Digest of IEEE International Solid-State Circuits Conference, pp.26–29, Feb. 2003.
[3] K. Kanda, T. Miyazaki, K. Min, H. Kawaguchi, and T. Sakurai, "Two orders of magnitude reduction of low voltage SRAM's by row-by-row dynamic VDD control (RDDV) scheme," Proc. IEEE International ASIC/SOC Conference, pp.381–385, Rochester, USA, Sept. 2002.
[4] A. Agarwal, H. Li, and K. Roy, "A single V_t low-leakage gated-ground cache for deep submicron," IEEE J. Solid-State Circuits, vol.38, no.2, pp.319–328, 2003.
[5] H. Kawaguchi, Y. Iataka, and T. Sakurai, "Dynamic leakage cut-off scheme for low-voltage SRAM's," Technical Digest of Symposium on VLSI Circuits, pp.140–141, June 1998.
[6] H. Mizuno and T. Nagano, "Driving source-line cell architecture for sub-1-V high-speed low-power applications," IEEE J. Solid-State Circuits, vol.31, no.4, pp.552–557, April 1996.
[7] K. Osada, Y. Saitoh, E. Ibe, and K. Ishibashi, "16.7 fA/cell tunnel-leakage-suppressed 16 Mb SRAM for handling cosmic-ray-induced multi-errors," IEEE International Solid-State Circuits Conference, pp.302–303, 2003.
[8] T. Enomoto, Y. Oka, and H. Shikano, "A self-controllable voltage level (SVL) circuit and its low-power high-speed CMOS circuit applications," IEEE J. Solid-State Circuits, vol.38, no.7, pp.1220–1226, July 2003.
[9] A.J. Bhavnagarwala, et al., "A pico-Joule class, 1 GHz, 32 kbyte ×64b DSP SRAM with self reverse bias," Symp. on VLSI Circuits, pp.251–254, 2003.
[10] S.M. Sze, Semiconductor Devices-Physics and Technology, John Wiley & Sons, New York, 1985.
[11] K. Agawa, H. Hara, T. Takayanagi, and T. Kuroda, "A bit line leakage compensation scheme for low-voltage SRAM's," IEEE J. Solid-State Circuits, vol.36, no.5, pp.726–734, 2001.
[12] Berkeley predictive technology model web site: http://www-device.eecs.berkeley.edu/~ptm
[13] K. Min, Y. Kim, D.J. Kim, D.M. Kim, J.H. Ahn, and J.Y. Chung, "Efficient and large-current-output boosted voltage generators with non-overlapping-clock-driven auxiliary pumps for sub-1-V memory applications," IEICE Trans. Electron., vol.E87-C, no.7, pp.1208–1213, July 2004.
[14] K. Min, K. Kanda, and T. Sakurai, "Row-by-row dynamic source-line voltage control (RRDSV) scheme for two orders of magnitude leakage current reduction of sub-1-V-V_{DD} SRAM's," IEEE/ACM International Symposium on Low Power Electronics and Design, pp.66–71, Seoul, Korea, Aug. 2003.



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