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LETTER *Special Section on VLSI Design Technology in the Sub-100 nm Era*

Trends of On-Chip Interconnects in Deep Sub-Micron VLSI

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SUMMARY This paper discusses propagation delay error, transient response, and power consumption distribution due to inductive effects in optimal buffered on-chip interconnects. Inductive effect is said to be important to consider in deep submicron (DSM) VLSI design. However, study shows that the effect decreases and can be neglected in next technology nodes for such conditions.

key words: *on-chip interconnects, deep sub-micron, inductive effect, signal integrity*

1. Introduction

On-chip interconnects shrink and can be classified into local, semiglobal, and global lines as shown in Fig. 1(A) [1]. In deep sub-micron VLSI's, interconnect inductive effect, which is one of signal integrity issues, is important and needs to study, since it may cause phenomena such as propagation delay error, overshoots, and so on.

This study uses ITRS data [1], and ITRS depicts two important interconnect parameters: 1) wiring pitch, which is two times as big as interconnect minimum width W_0, and 2) aspect ratio, which is ratio of wire thickness T to W_0, is 1.7–2.5. Inductive interconnect in VLSI's can be modeled with model shown in Fig. 1(B). Where, driver transistor is expressed with driver resistance R_T and junction capacitance C_J, while load transistor is expressed with load capacitance C_T. Parameters R, L, and C are wire resistance, inductance, and capacitance, respectively.

As widely known, buffers (repeaters) are usually used in line longer than optimal length to reduce propagation delay. Here, inductive effect is studied for optimal buffered interconnects system, since it suffers from inductive effect more due to the use of big driver and long enough interconnect and the trends of which are easy to grasp.

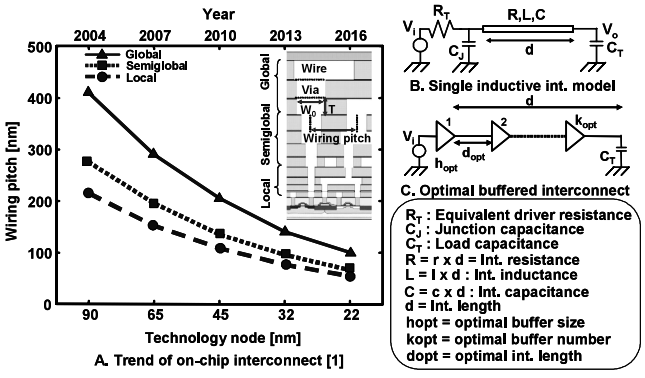

Fig. 1 On-chip interconnects.

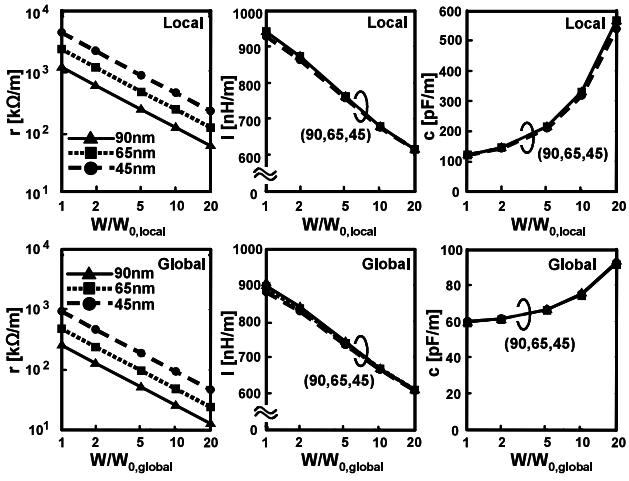

Fig. 2 Int. resistance r, inductance l, and capacitance c (per unit length).

2. Trends of Inductive Interconnects

The concept of optimal buffered interconnect is shown in Fig. 1(C). Buffers are inserted into long interconnect to portion interconnect line into shorter section(s) to reduce propagation delay. Although it neglects C_J, with/without considering L, optimal buffer size h_{opt} and number k_{opt} can be calculated with expressions proposed in [2]. While optimal length d_{opt} can be calculated as follows, $d_{opt} = d/k_{opt}$. Note that d_{opt} is not dependent on d, and determined by technology.

In this paper, local and global lines are assigned for the lowest level of interconnect metal layer and for 10th level of interconnect metal layer, respectively. Also, copper metal is used for calculation in DSM technology.

Figure 2 shows electrical interconnect parameters per unit length ($r = R/d$, $l = L/d$, $c = C/d$) at normalized wire width W/W_0 in various 90 nm-, 65 nm-, and 45 nm-technologies, where W_0 is as aforementioned, minimum in-

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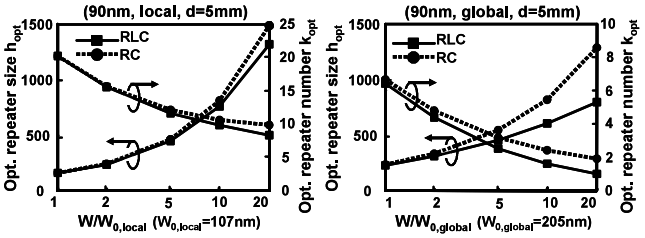

Fig. 3 Optimal repeater size and number in 90 nm-technology.

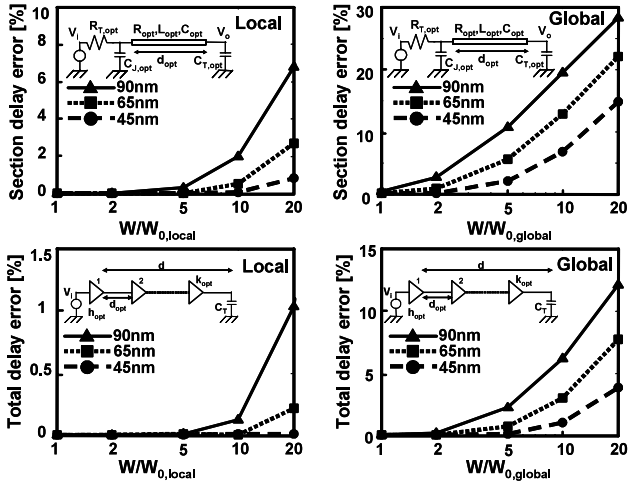

Fig. 4 Propagation delay error in optimally buffered interconnects.

terconnect width. Resistance r is calculated using conventional formula and increases exponentially for next technologies, while c and l are calculated using formulas proposed in [3] and [4] respectively, and almost constant to each technology. Note that inductance is proportional to log of space between lines S, which is assumed as $S=10W_0$ for realistic worst case condition. Note also that, as shown in Fig. 1(A), minimum wire width for global line $W_{0,global}$ is bigger than that of local line $W_{0,local}$.

Figure 3 shows fluctuation of optimal buffer size and number for various W at 90 nm-technology with/without considering L. Considering inductance results in less yet smaller buffer(s) needed for optimization. Long interconnect length d=5 mm is assumed for realistic long line on chips. As an example, for 90 nm global line $W = W_0$=205 nm, $R_{T,opt}$=136 Ω, $C_{T,opt}$=31 fF, h_{opt}=222, k_{opt}=6.4, and d_{opt}=0.78 mm.

Figure 4 shows section delay error and total delay error in local/global buffered interconnects. Section delay error is defined as error in one section of *RLC* buffered interconnects with/without considering L for delay calculation. Note that neglecting inductance results in underestimating propagation delay. Total delay error shows the total error in optimal buffered *RLC* interconnect, where optimal buffer size h_{opt} and number k_{opt} are calculated with/without considering L. The errors increase as W increases since though l decreases and c increases for wider W, however, r decreases exponentially. Also global line suffers from inductance more than

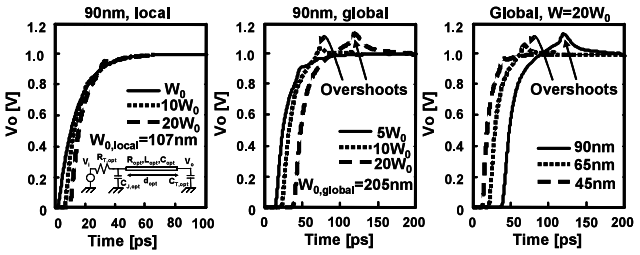

Fig. 5 Output responses of one section *RLC* buffered interconnects.

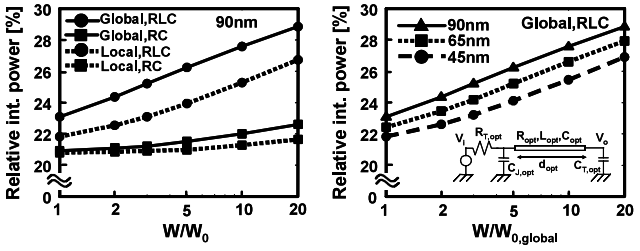

Fig. 6 Relative interconnect power consumption distribution.

local line, since simply r and c in global lines are much smaller that those in local line.

Inductive effect is also known for potential cause of overshoots, and overshoots threaten the reliability of circuits. Figure 5 shows the transient output response of one section of *RLC* buffered interconnects with considering junction capacitance $C_{J,opt} = C_{T,opt}$. Circuit simulation is carried out with single inductive interconnect model. Transmission line element is used for interconnect instead of lumped model for best result. The results show that almost no overshoot occurs in local line even when wide W ($\leq 20W_0$) is used. While overshoots are potential to occur in wide global line and increase as W increases. However, the overshoot decreases as scaling technology continues.

Power consumption distribution in optimal buffered interconnects system can be calculated using method proposed in [5]. Relative interconnect power is defined as ratio of power consumed in interconnect to total power consumption. Where total power consumption is the sum of power consumed in interconnects and in transistor. Trends of relative interconnect power for one section of optimal buffered interconnect is shown in Fig. 6 for various conditions. Considering inductance results in higher power consumption distribution in interconnects.

3. Conclusion

Using ITRS data, study showed that inductive effect results in propagation delay error, overshoots, and fluctuation power consumption distribution. In optimally buffered interconnects on DSM VLSI's, simulation and calculation results showed that inductive effect: 1) increases as wire width W or wire height H increases; 2) decreases for next technologies; and 3) results in about 10% error or less when W is less than $5W_0$.

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