A Self-Alignment Row-by-Row Variable-V_{DD} Scheme Reducing 90% of Active-Leakage Power in SRAM's***

Fayez Robert SALIBA[†*], Hiroshi KAWAGUCHI[††**a)], *Nonmembers*, *and* Takayasu SAKURAI[†††], *Member*

SUMMARY   We report an SRAM with a 90% reduction of active-leakage power achieved by controlling the supply voltage. In our design, the supply voltage of a selected row in the SRAM goes up to 1 V, while that in other memory cells that are not selected is kept at 0.3 V. This suppresses active leakage because of the drain-induced barrier lowering (DIBL) effect. To avoid unexpected flips in the memory cells, the wordline voltage is controlled so that it is always lower than the supply voltage in the proposed SRAM, with a self-alignment timing generator. The additional area overhead of the timing generator is 3.5%.
key words: active leakage, low power, SRAM

1. Introduction

To meet the requirements of battery-operated portable equipment, low-power techniques are demanded. In particular, strategies to lower active leakage are becoming important since the supply voltage (V_{DD}) and threshold voltage (V_{TH}) have been lowered. According to the ITRS prediction [2], 90% of the area of a system LSI will be occupied by memory in 2013, as shown in Fig. 1, and considerably large leakage current will flow through it. Since SRAM compatible with a CMOS process apparently will play a prominent role as a memory even in a future system LSI, it is important to reduce the leakage current through the large-area SRAM, not only in the standby mode but also in the active mode. However, it is not possible merely to apply an existing leakage cutoff scheme such as the MTCMOS [3] to SRAMs, because information stored in the SRAMs would be lost if the power line were cut off. The MTCMOS does not address the active-leakage problem in SRAMs.

Other ways of achieving low standby-power SRAMs have been proposed [4]–[6]. When a row in an SRAM is accessed, the source voltage in the minuscule region becomes grounded. In all other memory cells, the source voltage is kept at a low voltage that just sustains data, which suppresses leakage current, particularly the bitline leakage flowing from bitlines to memory cells. This source-biasing
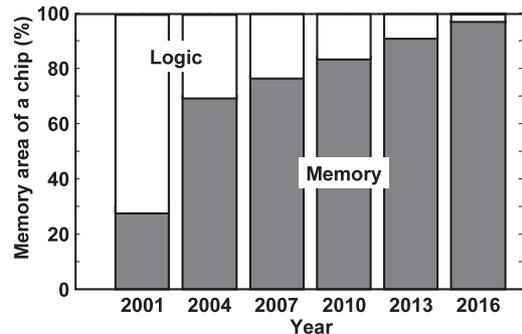
Fig. 1 ITRS prediction of memory area on a system LSI.

technique, however, cannot maintain electromigration reliability [7], when the common source line is long, since the source line draws all sink current flowing from memory cells and heavy-load bitlines. In addition, a gate bias against the substrate in the source-biasing technique is not mitigated, which may potentially lead to gate leakage in future thin-oxide processes. To prevent this kind of gate leakage, well separation between the source and ground lines by adopting a triple-well technology is effective, but this requires more than 10% area overhead even when trench isolation is adopted [8].

The row-by-row dynamic V_{DD} (RRDV) scheme [7] controls the V_{DD} of an accessed row in operation but not the source voltage, and prevents active leakage by the drain-induced barrier lowering (DIBL) effect. The active leakage is exponentially reduced by the DIBL as the supply voltage is lowered [9]. The concept of the RRDV scheme is illustrated in Fig. 2 where a row decoder generates not only a wordline signal but also an additional cell V_{DD}. When a row is activated, the cell V_{DD} is set to a high voltage (V_{DDH}). On the other hand, when a row is not accessed (in a dormant row), the cell V_{DD} is lowered to a standby voltage (V_{DDL}). The RRDV scheme localizes activation only in the accessed cells, and minimizes cell leakage. The cell leakage reduction with the row-by-row activation is less in nature than that with block-by-block activation due to the small activation region. V_{DDL} must be low enough ($< 350\,\text{mV}$) to achieve a one-order-of-magnitude leakage reduction but high enough to preserve stored data.

At the same time, we must pay attention to the timing between the cell V_{DD} and the wordline voltage of an accessed row in the RRDV scheme. Since a pair of bitlines is precharged to V_{DDH} to read a high-supply-voltage memory
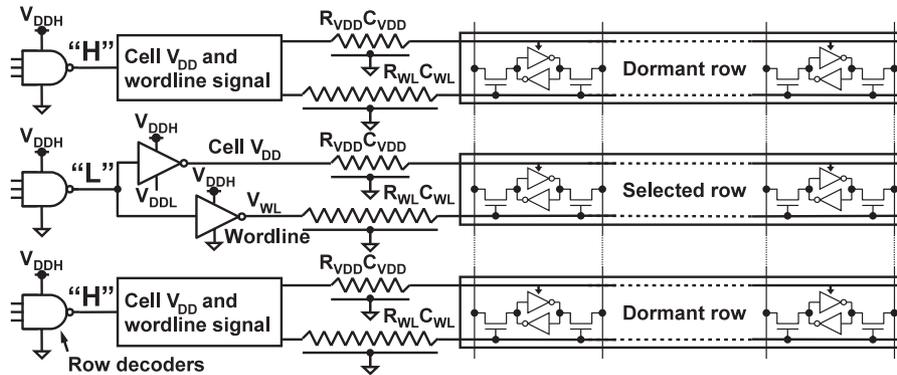
Fig. 2 Row-by-row variable V_{DD} (RRDV) scheme.
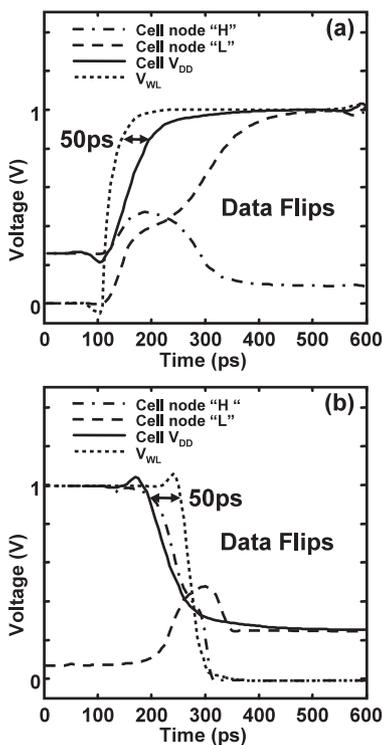
Fig. 3 Unexpected data flips in the RRDV scheme. (a) Rising edge of a wordline voltage is faster than a cell V_{DD} by 50 ps, and (b) falling edge of a wordline voltage is slower than a cell V_{DD} by 50 ps.

cell, the cell V_{DD} is lower than the bitline voltage in a dormant row. At the beginning of the readout, if the wordline voltage becomes high before the cell V_{DD}, the data stored in the cell may be charged from the bitlines. This situation is similar to a write operation, and thus results in the destruction of the stored data. Figure 3 illustrates the data flips when a couple of inverters in a memory cell have a threshold variation. The unexpected data flips are observed, in which a wordline is asserted longer than a cell V_{DD} only by 50 ps. Due to this problem, a straightforward and simple implementation of the RRDV scheme is ineffective. Instead, we propose an improved version of the RRDV scheme, the self-alignment row-by-row variable V_{DD} (SARRVV) scheme, in this paper.

2. Self-Alignment Row-by-Row Variable V_{DD} Scheme

As shown in Fig. 2, a cell V_{DD} line and a wordline have different RC delays. A cell V_{DD} line is more capacitive since a couple of inverters in a memory cell have "H" and "L" outputs, and a cell V_{DD} line has half the total capacitance of memory cells. This means that a cell V_{DD} is usually slower in operation than a wordline voltage. Consequently, the wordline voltage increases faster than the cell V_{DD} at rising edges, at which moment the memory cell exhibits a corrupted butterfly curve, as shown in Fig. 4. There is no static noise margin (SNM) at a cell V_{DD} of 0.25 V when the voltage of a wordline (V_{WL}) is 0.30 V or higher, which is the reason why data stored even in balanced memory cells are corrupted in the RRDV scheme. Figure 5 again illustrates the SNM at the cell V_{DD} of 0.25 V when V_{WL} is changed. The SNM vanishes when V_{WL} is more than 0.30 V.

Even if a cell V_{DD} line is less capacitive than a wordline, the same situation takes place in falling edges where a row is deactivated. In any event, the RRDV scheme does not function unless it has proper timing control, since both a cell V_{DD} line and a wordline are subject to different RC delays that may vary chip by chip. Eventually, self-alignment timing generation will be needed to achieve the goal.

In Fig. 6(b), our proposed SARRVV scheme capable of guaranteeing the timing requirement is illustrated. The SARRVV scheme is based on a feedback mechanism that takes into account the RC delay variation, unlike the conventional scheme in Fig. 6(a). In the proposed SARRVV scheme, there are two feedback signals in each row: V_{SVF} that controls the timing of the falling edge of a cell V_{DD}, and V_{WF} for the rising edge of a wordline. The additional timing generator is split into two parts. The first one is on the decoder side (front circuit) and the second one is at the end of a cell V_{DD} line and a wordline (back circuit). Signal "DEC" is an output of the conventional NAND-type row decoder. In the static situation, all the cell V_{DD}s are V_{DDL}, and V_{WL}s are grounded.

When a row is selected, Node "A" in Fig. 6(b) begins to rise, and at the same time, V_{WL} is cut out of the ground, but still retains its value. Then, the cell V_{DD} increases to V_{DDH}
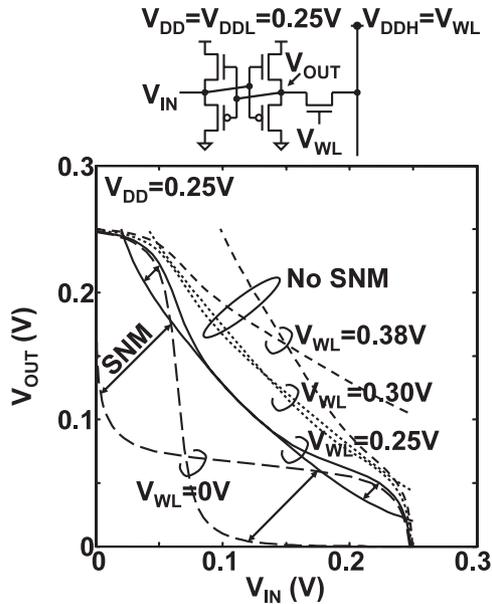
Fig. 4 Butterfly curves in the RRDV scheme.
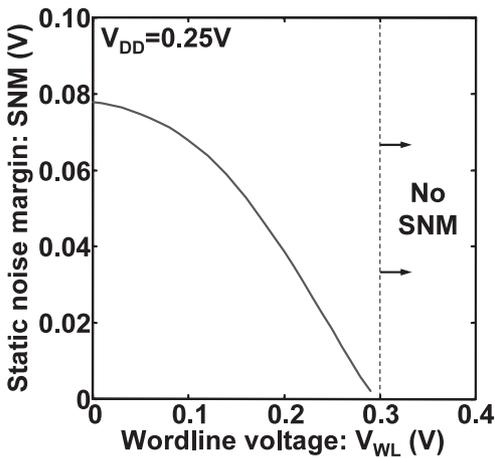
Fig. 5 Static noise margin when V_{WL} is changed.

Fig. 6 (a) Conventional and (b) self-alignment row-by-row variable V_{DD} (SARRVV) schemes.
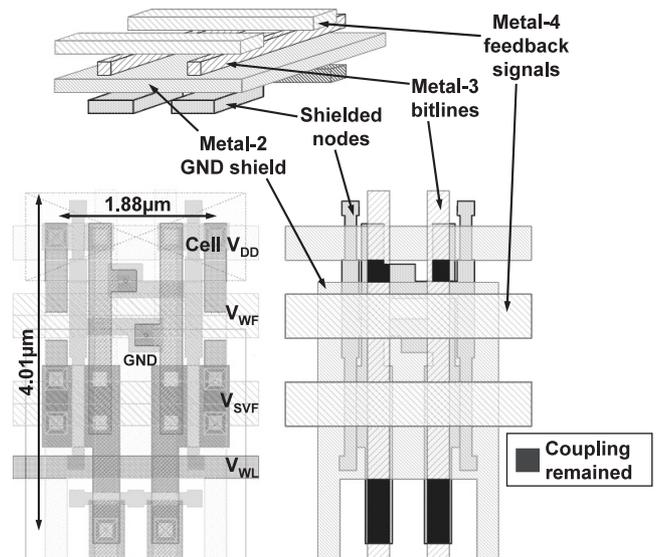
Fig. 7 Memory cell layout in the SARRVV scheme.

after an RC delay of the cell V_{DD} line, and the V_{DDH} signal reaches Node "B." Next, V_{WF} starts falling, and when the transition edge of V_{WF} reaches Node "C," V_{WL} is pulled up to V_{DDH}. In this way, we can ensure that V_{WL} is activated after the cell V_{DD} reaches V_{DDH} for all the cells in the selected row.

In contrast, when the row is deselected, Signal "DEC" increases to V_{DDH}. Node "D" immediately starts discharging from V_{DDH} to the ground. However, Node "A" remains high until the falling Node "E" sets V_{SVF} to be high. Thus in the deselecting process, as well as the selecting process, we can ensure that the wordline is turned off before cell V_{DD} is lowered to V_{DDL}. The same feedback mechanism can be utilized even in the source-biasing schemes to maximize the static noise margin.

Since the cell V_{DD} in a dormant memory cell is a low V_{DDL}, the stored charge in the cell is small and the node data

are more susceptible to coupling noise from bitlines and the feedback signals. In our memory cell layout, we provide a shielding cover of the grounded Metal-2 layer to protect the data-stored nodes from the coupling noise, as illustrated in Fig. 7. Bitlines are made of the Metal-3 layer, and the Metal-

4 layer is used for the feedback signals. Therefore, the cell area overhead for the proposed SARRVV scheme is zero.

3. Simulation and Measurement Results

To estimate the delay overhead added by the SARRVV scheme, we carried out a SPICE simulation on a readout time difference, as depicted in Fig. 8. The delay in both the conventional scheme and SARRVV schemes is defined as the time from the "DEC" assertions to the half V_{DD}s on the bitlines. In the conventional scheme, a wordline driver in Fig. 6(a) drives a wordline as soon as Signal "DEC" is asserted. In contrast, in the SARRVV scheme, a wordline driver, as shown in Fig. 6(b), drives a wordline after the arrival of a feedback signal from Inverter I. Hence, there is some delay overhead on a wordline in the SARRVV scheme, which, in turn, causes the bitline delay in Fig. 8. The delay overhead on the bitline is 260 ps in the simulation (V_{DDH}=1 V, V_{DDL}=270 mV), which corresponds to a 1.5-fold delay of a fanout-4 2NAND and 9% of a 3-ns clock cycle. Note that, in the figure, the wordline voltage never surpasses the cell V_{DD} at either the rising or falling edge thanks to the self-alignment timing control.

A 16-kb (256 columns × 64 rows) SARRVV SRAM test chip was manufactured in a 0.15-μm FD-SOI process technology with five metal layers. Figure 9 illustrates the measured waveforms output from one of the data buffers at V_{DD} of 1 V and a clock frequency of 1 MHz. Seven write-in accesses to different addresses followed by seven readout accesses from the same addresses were obtained. The written and read data match.

The measured Shmoo plots are shown in Fig. 10. In the test, all addresses are verified by a logic tester with multi-

ple read and write operations using random data. Since the nominal supply voltage in the process used is 1 V, V_{DDH} was set between 0.8 V and 1.1 V in steps of 0.05 V. We changed V_{DDL} between 200 mV and 800 mV in steps of 10 mV. We tested the proposed SARRVV SRAM at the typical (CC: $V_{TH-NMOS}$ = 0.155 V, $V_{TH-PMOS}$ = −0.254 V) and fast (FF: $V_{TH-NMOS}$ = 0.110 V, $V_{TH-PMOS}$ = −0.208 V) corners. The lower boundary of V_{DDL} is due to the V_{TH} variation inside the memory cells, and corresponds to the minimum retention voltage.

At the nominal supply voltage of 1 V, the minimum retention voltages at the typical and fast corners are 260 mV and 250 mV, respectively. We infer that the random variation at the fast corner is smaller than that at the typical corner since the implanted dopant concentration is lower at the fast corner [10]. Unfortunately, the minimum retention voltage at the slow (SS) corner was not measured because we were not able to obtain test chips at that corner. The reten-
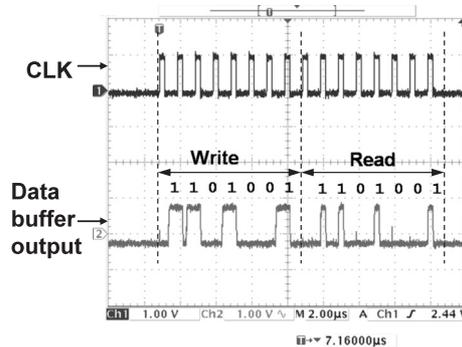
Fig. 9 Output waveforms.
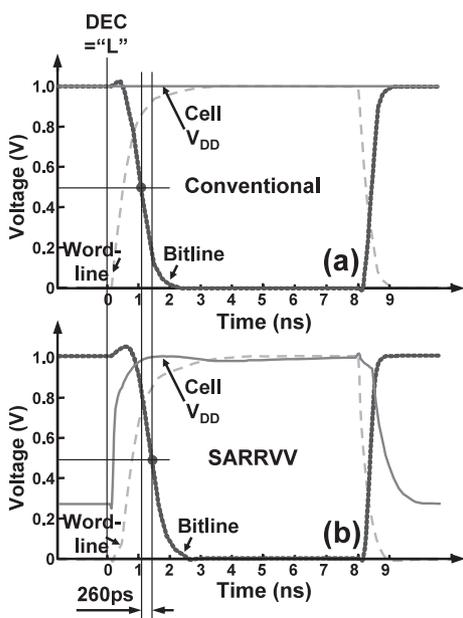
Fig. 8 Operating waveforms in (a) the conventional scheme, and (b) the SARRVV scheme.
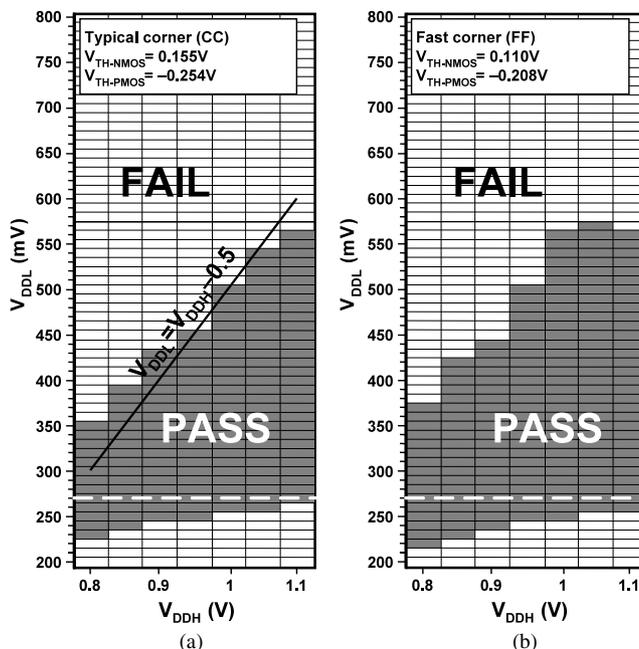
Fig. 10 Shmoo plots. (a) The typical (CC) corner and (b) the fast (FF) corner.

Measured cell leakage power (nW)								
	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
Measured cell leakage power (nW)		5.1	12.2	22	34.6	50.7	72.4	97.6	120.5

V_{DDL} (V)
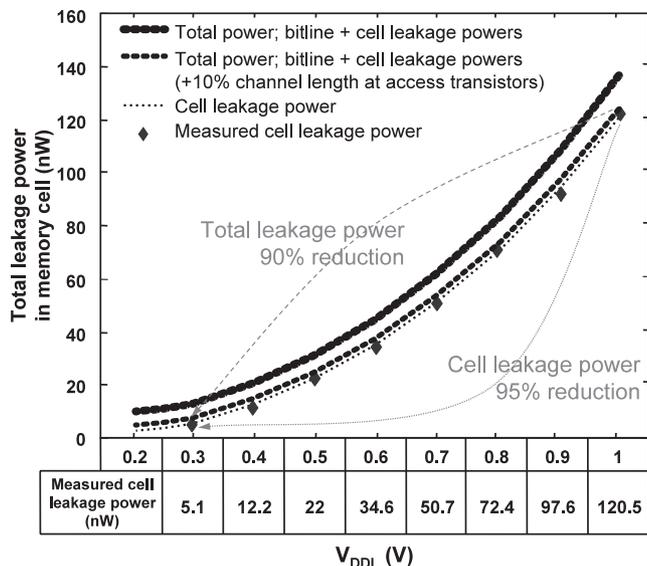
Fig. 11 Leakage power characteristics in the SARRVV SRAM.

tion voltage at the slow corner is inferred to be higher than the 260 mV at the typical corner since the implanted dopant concentration is higher and the random variation is larger at the SS corner.

The upper bounds of the Shmoo plots are roughly expressed as $V_{DDL} = V_{DDH} - 0.5$ V, which indicates the functional limit of the feedback inverter that drives V_{WF} (Inverter I in Fig. 6(b)). This implies that the feedback inverter does not operate when $V_{DDH} - V_{DDL}$ is less than 0.5 V.

Figure 11 shows the simulated and measured leakage power of the cell array as a function of V_{DDL}. The leakage power has two components: bitline leakage and cell leakage. The SARRVV can reduce the cell leakage power by 95% at V_{DDL} of 0.3 V by exploiting the DIBL effect. Even though the bitline leakage component is much less affected by V_{DDL}, it can be reduced by making the channel length of the access transistor longer. Even when the channel length is expanded by only 10%, the bitline leakage is dramatically reduced since the long channel suppresses the short-channel effect (V_{TH} roll off), and keeps V_{TH} higher than that of the minimum-length transistor. In total, a 90% reduction of the active-leakage power is achievable.

Note that the SARRVV scheme will potentially reduce the gate leakage in a future thin-oxide process, as mentioned in Sect. 1. In practice, the reduction of cell leakage was achieved because of the DIBL effect in the fabrication process we utilized. This is because the subthreshold current is dominant and the gate leakage is completely negligible in the 0.15-μm process technology. However, the gate leakage is much larger in the 65-nm process technology, and will become prominent beyond the 45-nm process technology. The SARRVV scheme can suppress the gate leakage as well as the subthreshold leakage in future processes since gate leakage in a memory cell is exponentially proportional to the cell V_{DD}.

The chip micrograph of the SARRVV 16-kb SRAM
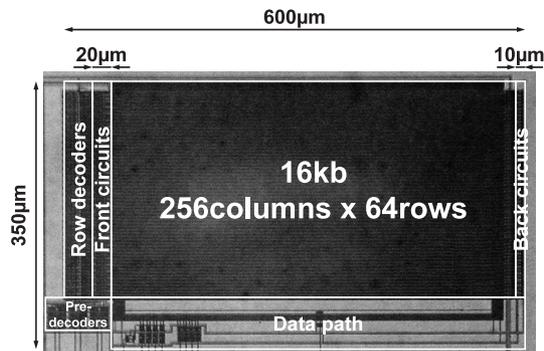
Fig. 12 Chip micrograph of the SARRVV SRAM.

is shown in Fig. 12. The total area is $600 \times 350 \, \mu$m^2. Although there is no area overhead in memory cells, the self-alignment timing generator (front and back circuits) gives rise to a 5% overhead of additional area. In the figure, the additional lengths in the lateral direction are $20 \, \mu$m and $10 \, \mu$m for the front and back circuits, respectively. As shown in Fig. 6(b), the cell V_{DD} driver and wordline driver in the front circuit must be large enough to drive the heavy loads, while the inverters in the back circuit are used merely to feed signals back. Therefore, the area occupied by the front circuits is larger than that occupied by the back circuits. Since the cell array efficiency is typically 0.7 according to the ITRS Roadmap [2], the area overhead in the SARRVV scheme is reduced to 3.5% (= 5% × 0.7) in the entire SRAM including peripheral circuits. For a larger capacity SRAM, the area overhead will be lowered to less than 3%.

4. Conclusion

We proposed the self-alignment row-by-row variable V_{DD} (SARRVV) scheme for a low-active-leakage SRAM. The SARRVV scheme always maintains the cell V_{DD} higher than the wordline voltage to avoid any unexpected flip in the memory cell. We have verified that a retention voltage of 0.3 V reduces the cell leakage power by 95% and the total active-leakage power by 90% in a 0.15-μm SOI process technology. The additional area overhead is 3.5% in a 16-kb SRAM.

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Fayez Robert Saliba   received the B.E. degree in electrical engineering from Saint Joseph University, Beirut, Lebanon, in 2000. He received the M.E. degree in electronic engineering from the University of Tokyo, Tokyo, Japan, in 2004, where he researched low-power, low-voltage VLSI circuits. Since 2004, he has been working for Takumi Technology Corporation, Sunnyvale, CA, as a Software Application Engineer on solutions for design for manufacturing (DFM) aimed at improving yield, and minimizing the total cost of technology ownership. His main interests include, other than these, 2D layout optimization and automatic repair, multiple yield loss mechanisms detection, analysis and rating.

Hiroshi Kawaguchi   received the B.E. and M.E. degrees in electronic engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and the Ph.D. degree in engineering from the University of Tokyo, Tokyo, Japan, in 2006. He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to the Institute of Industrial Science, the University of Tokyo, as a Technical Associate in 1996, and was appointed a Research Associate in 2003. Since 2005, he has been a Research Associate with the Department of Computer and Systems Engineering, Kobe University, Kobe, Japan. He is also a Collaborative Researcher with the Institute of Industrial Science, the University of Tokyo. His current research interests include low-power VLSI design, hardware design for wireless sensor network, and recognition processor. Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Award for Outstanding Far-East Paper. He has served as a Program Committee Member for IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences. He is a member of the IEEE and ACM.

Takayasu Sakurai   received the Ph.D. degree in EE from the University of Tokyo, Tokyo, Japan, in 1981. In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a visiting researcher at the University of California Berkeley, where he conducted research in the field of VLSI CAD. From 1996, he has been a Professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic IC's and large-area electronics. He has published more than 350 technical publications including 70 invited publications and several books and filed more than 100 patents. He served as a conference chair for the Symposium on VLSI Circuits, and ICICDT, a vice chair for ASPDAC, a TPC chair for the first A-SSCC, and VLSI Symposium and a program committee member for ISSCC, CICC, DAC, ESSCIRC, ICCAD, FPGA workshop, ISLPED, TAU, and other international conferences. He is a plenary speaker for the 2003 ISSCC. He is a recipient of 2005 IEEE ICICDT award, 2005 IEEE ISSCC Takuo Sugano award and 2005 P&I patent of the year award. He is an IEEE Fellow, a STARC Fellow, an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS distinguished lecturer.