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# Area Optimization in 6T and 8T SRAM Cells Considering $V_{th}$ Variation in Future Processes

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**SUMMARY** This paper shows that an 8T SRAM cell is superior to a 6T cell in terms of cell area in a future process. At a 65-nm node and later, the 6T cell comprised of the minimum-channel-length transistors cannot make the minimum area because of threshold-voltage variation. In contrast, the 8T cell can employ the optimized transistors and achieves the minimum area even if it is used as a single-port SRAM. In a 32-nm process, the 8T-cell area is smaller than the 6T cell by 14.6% at a supply voltage of 0.8 V. We also discuss the area and access time comparisons between the 6T-SRAM and 8T-SRAM macros.

***key words:*** *6T SRAM cell, 8T SRAM cell,* $V_{th}$ *variation*

## 1. Introduction

According to the ITRS Roadmap, memories will occupy 80% of an SoC's area in 2013 [1]. For the large-capacity memory, SRAMs will be utilized, as well as these days, since SRAMs are compatible with a CMOS process. Hence, in the future, SRAMs will dominate a chip cost. An SRAM area should be as small as possible for the manufacturing cost and a yield.

On the other hand, a large-size transistor is preferable to suppress a threshold-voltage ($V_{th}$) variation. A standard deviation of $V_{th}$ ($\sigma_{Vth}$) is given as follows [2]:

$$\sigma_{Vth} \propto T_{OX} \cdot \frac{\sqrt[4]{N \cdot T \cdot \ln(N/n_i)}}{\sqrt{L_{eff} \cdot W_{eff}}},$$

where $T_{OX}$ is a gate oxide thickness, $N$ is a channel dopant concentration, $T$ is a absolute temperature, $n_i$ is an intrinsic carrier concentration, $L_{eff}$ and $W_{eff}$ are an effective channel length and width of a transistor. A long channel, wide channel, and thin gate oxide make $\sigma_{Vth}$ small, and thus improve a yield. However, $\sigma_{Vth}$ is becoming larger, generation by generation, although the gate oxide is gradually thinned. This is because the channel area ($L_{eff} \cdot W_{eff}$) are shrunk as a manufacturing process is advanced, which situation is illustrated in Fig. 1 by means of Pelgrom plots.

To cope with the increasing $V_{th}$ variation, a $\beta$ ratio (a size ratio of a driver transistor to an access transistor) must be enlarged along with generations in the conventional six-transistor (6T) SRAM cell. On the other hand, in an eight-transistor (8T) cell, the $\beta$ ratio does not need to be considered because the 8T cell has a separate read port. In this paper, we report the area optimization of the 8T cells for a high-density low-cost SRAM. We compare the areas of the 6T and 8T cells in a 90-nm to 32-nm processes, and demonstrate that the 8T cell can be an alternative design to the 6T cell in terms of cell area. Even if the 8T cell with the extra read port is used as a single-port SRAM, the area of the 8T cell will be smaller in the future process with the large $V_{th}$ variation.

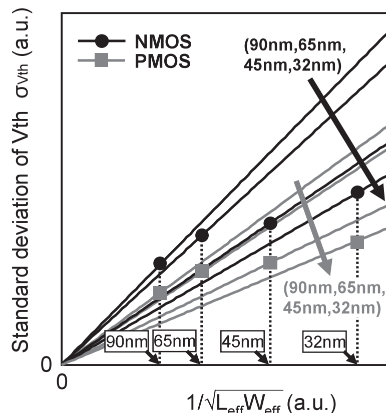


**Fig. 1** Pelgrom plots in different processes. $\sigma_{Vth}$ becomes larger as a manufacturing process is advanced.

The rest of this paper is organized as follows. The next section describes the characteristics of the 6T and 8T cells from a viewpoint of operating margins. In Sect. 3, we make an area comparison, and show that the area of the 8T cell can be smaller in the future process. In addition, the relation between an SRAM macro area and access time in the 6T and 8T cases is discussed in Sect. 4. Section 5 concludes this paper.

## 2. Characteristics of 6T and 8T SRAM Cells

### 2.1 6T SRAM Cell

Figures 2(a) and (b) show a schematic and layout of the conventional 6T SRAM cell comprised of six transistors: access transistors (Na1 and Na2), driver transistors (Nd1 and Nd2), and load transistors (Pl1 and Pl2). A wordline (WL) opens the access transistors and activates a cell. A pair of bitlines (BL and BL_N) are for reading and writing a datum.

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In the 6T cell, we have to pay attention to both read and write margins as illustrated in Fig. 3 [3]. The schematics in the figure signify the assignments of the local $V_{\mathrm{th}}$ variations on the worst-case read and write conditions. The four transistors in the 6T cell (Na1, Nd1, Nd2 and Pl2 for read; Na1, Pl1, Nd2 and Pl2 for write) affect the operating margins [4], [5]. $n$ is a coefficient, and for instance, $n = 3$ indicates that a local $V_{\mathrm{th}}$ variation of $6\sigma_{Vth}$ is considered in the 6T cell. The asymmetrical assignment of the local $V_{\mathrm{th}}$ variation makes the butterfly plots asymmetrical on the read condition (see Fig. 3(a)), and worsens the read margin.

The read margin in the 6T cell correlates with a logical $V_{\mathrm{th}}$ of an inverter (Nd2 and Pl2), and is inversely related to a minimum output voltage of the inverter latch ($V_{\mathrm{RO}}$ in Fig. 3(a)) [3]. If the width of the access transistor ($W_{\mathrm{a}}$) is increased, that is, if the $\beta$ ratio is decreased, $V_{\mathrm{RO}}$ becomes larger. This means a smaller read margin.

As for the write margin, it also correlates to the logical $V_{\mathrm{th}}$ of the inverter and is inversely related to $V_{\mathrm{WO}}$ in Fig. 3(b) [3]. In this paper, we define the size ratio of the access transistor to the load transistor, as the $\gamma$ ratio. As $W_{\mathrm{a}}$ or the $\gamma$ ratio is decreased, $V_{\mathrm{WO}}$ becomes larger, which hinders write operation.

The read and write margins in the 6T cell are illustrated in Fig. 4 by means of milky-way plots [6], according to which we define the read and write margins. The diamond shape in the figure indicates the process corners (FF, FS, SF, SS, and CC corners; "F" means the fast corner, "S" means the slow corner, and "C" means the center corner; for example, FS means that the current-drive performance

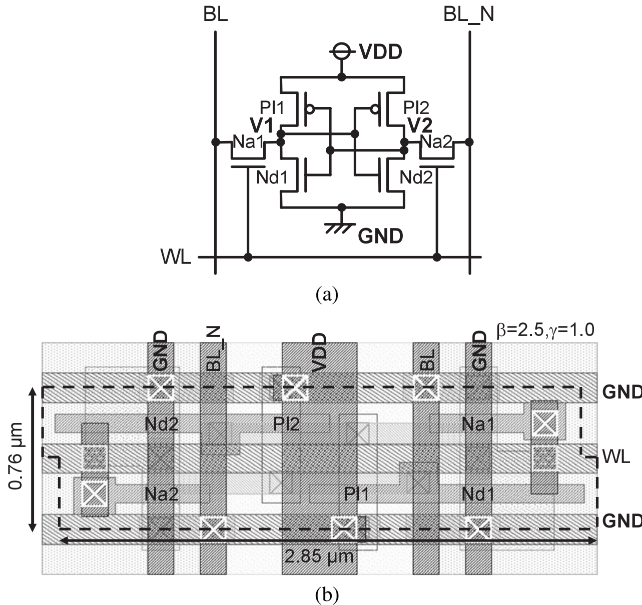
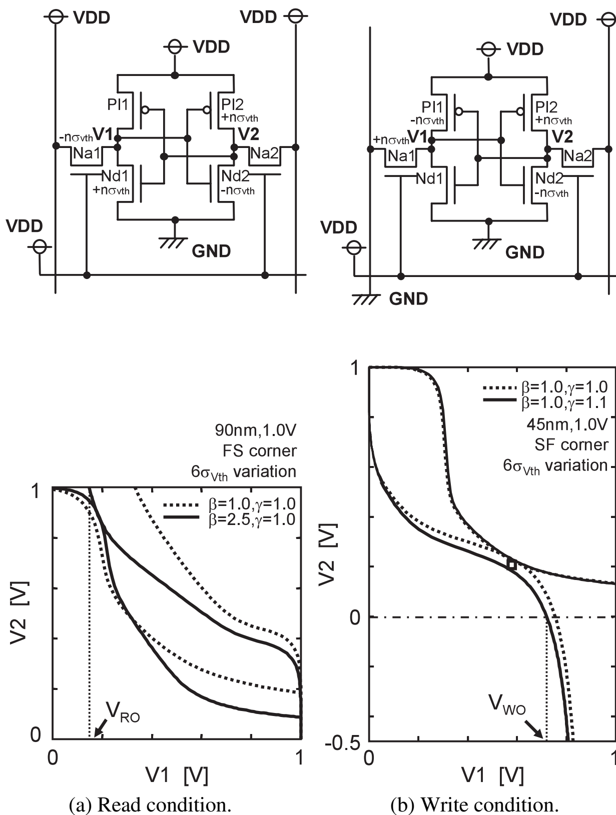



**Fig. 2** (a) A schematic and (b) layout of a 6T SRAM cell designed with a 90-nm logic rule.




(a) Read condition. (b) Write condition.

**Fig. 3** The worst-case conditions of local $V_{\mathrm{th}}$ variations and operating margins in a 6T cell. (a) Read condition (butterfly plot) and (b) write condition [3].

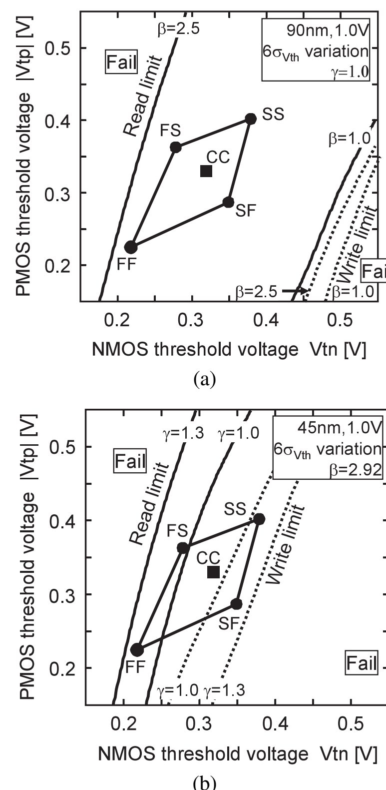



**Fig. 4** Operating margin dependencies in a 6T cell, (a) when the $\beta$ ratio is varied at a 90-nm node, and (b) when the $\gamma$ ratio is varied at a 45-nm node.

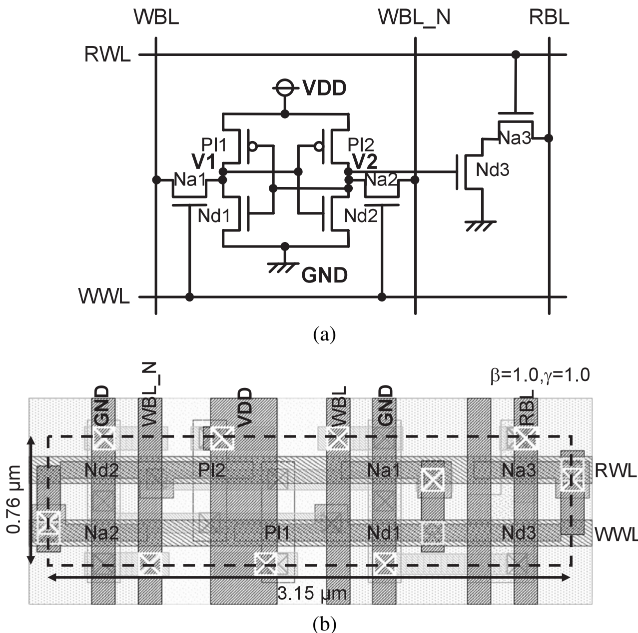



**Fig. 5** (a) A schematic and (b) layout of an 8T SRAM cell designed by the same rule as Fig. 2(b).

of a n-channel transistor is "Fast" and that of a p-channel transistor is "Slow"), where a global (wafer-to-wafer/lot-to-lot) $V_{\rm th}$ variation is reflected. In other words, the size of the diamond shape signifies the global $V_{\rm th}$ variation, while the position of the CC corner means a nominal $V_{\rm th}$ setting. As for the random variation, a $V_{\rm th}$ variation of $6\sigma_{Vth}$ is considered.

In the region between the read and write limit curves, both read and write margins are obtained and thus the 6T cell works correctly under the $V_{\rm th}$ variation. In other words, outside of the read limit, a stored datum in the 6T cell is flipped even by precharging of the bitlines. On the other hand, outside of the write limit, we cannot flip the datum by the write operation.

Figure 4(a) shows the case that the $\beta$ ratio is varied, but the $\gamma$ ratio is fixed to 1.0. The conductance ratio of the access transistor to that of the load transistor is 2.29. Although a large $\beta$ ratio satisfies the read margin, it makes the write margin smaller since the $\gamma$ ratio remains constant and the logical $V_{\rm th}$ of the inverter is lowered. To compensate the write margin, a large $\gamma$ ratio (large $W_{\rm a}$) is required. As exhibited in Fig. 4(b), a large $\gamma$ ratio expands both the read and write margins, but it turns out to a large size of the driver transistor to obtain a certain $\beta$ ratio. The large $\beta$ and $\gamma$ ratios lower memory capacity, and thus raise a chip cost.

### 2.2 8T SRAM Cell

In an 8T SRAM cell, we may merely consider a write margin [7], [8]. The 8T cell illustrated in Fig. 5(a) has a separate read port comprised of two transistors (Na3 and Nd3). WWL is a wordline for a write port. WBL and WBL_N are write bitlines. RWL and RBL are the dedicated wordline and bitline, respectively, for the read port. This structure of the 8T cell enables a stable read operation without sizing of the additional transistors and the driver transistors (Nd1 and Nd2), since the read operation does not disturb stored information [7], [8]. We can minimize the transistors at the read port and the driver transistors. However, in a 90-nm process, there is still an area overhead left in the 8T cell due to the additional transistors. The layout in Fig. 5(b) is larger than that in Fig. 2(b) by 10%. In the next section, we will point out that the standpoint is reversed in a future process with large $V_{\rm th}$ variation.

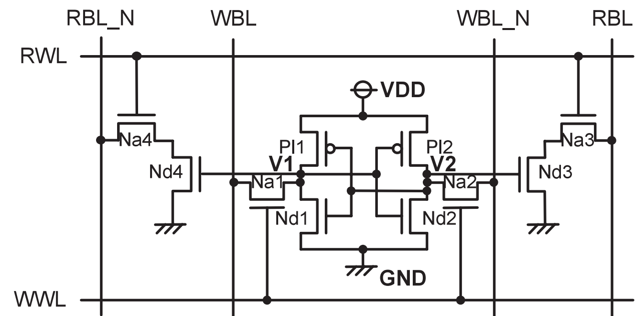



**Fig. 6** A schematic of a 10T cell [9].

We would like to mention another extended version of the 8T cell here. The 10T cell with the differential read bitlines has been proposed as shown in Fig. 6 [9]. The 10T cell combines the stable operation of the 8T cell and a fast access time of the 6T cell. However, the two transistors further appended (Na4 and Nd4) becomes an extra area overhead compared with the 8T cell. Therefore, we do not cover the 10T cell in this paper.

### 2.3 Operating Margins

Figure 7 again depicts milky-way plots that demonstrate operating limits in a 90-nm, 65-nm, and 45-nm processes [3]. Figure 7(a) corresponds to the 6T-cell case, and Fig. 7(b) is the 8T-cell case. The minimum channel length (= design rule, $L_{\rm min}$) and the minimum channel width ($W_{\rm min}$) are scaled by 0.7 time per generation. In this paper, we assume that the global $V_{\rm th}$ variation remains constant over the manufacturing processes since the global $V_{\rm th}$ is determined by manufacturing equipments and environments. The nominal $V_{\rm th}$ setting (CC corner) is also assumed to be constant over the manufacturing process, because $V_{\rm th}$ cannot be lowered in order to suppress sub-threshold leakage [1].

In the 6T cell, the read and write margins must be both guaranteed at all the process corners. We estimate the worst-case read margin at the FS corner and a temperature of 125°C. The write margin is estimated at the SF corner and −40°C. If the $\beta$ and $\gamma$ ratios are kept constant, the read and write margins are both degraded in the 6T cell, generation by generation, which is illustrated in Fig. 7(a). There is neither read nor write margin at the 45-nm node.

On the other hand, in the 8T cell, the read margin does not need to be considered as shown in Fig. 7(b). The write

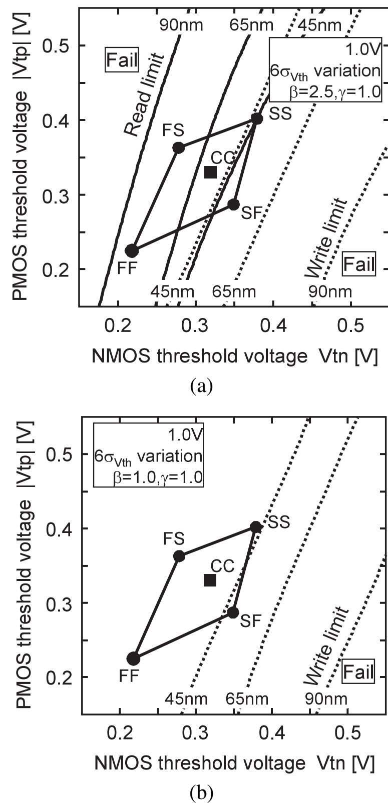



**Fig. 7** Milky-way plots of (a) 6T and (b) 8T SRAM cells in a 90-nm, 65-nm, and 45-nm processes when the $\beta$ and $\gamma$ ratios are fixed.

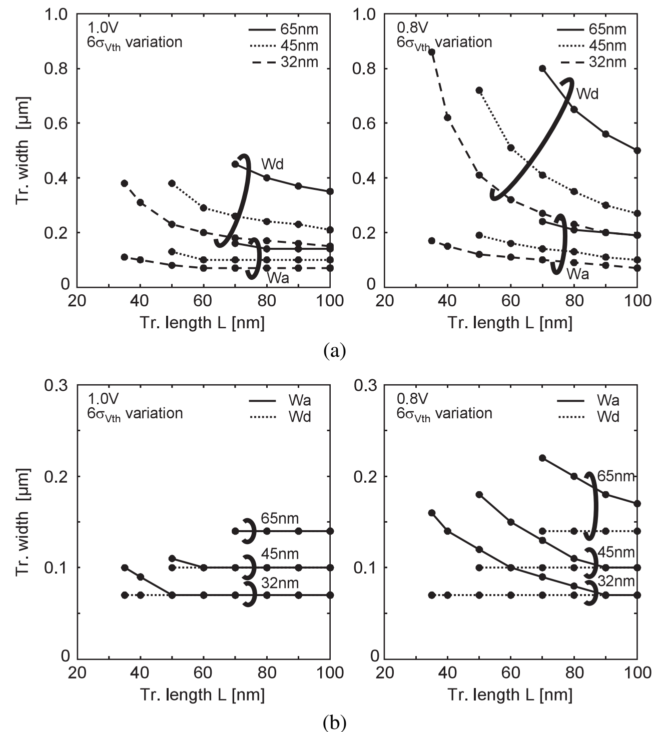



**Fig. 8** Minimum channel widths when the channel length is varied in (a) a 6T cell and (b) an 8T cell. VDD is set to 1.0 V and 0.8 V.

margin exhibits the similar characteristics to Fig. 7(a) since the $\gamma$ ratio is the same. However, the $\beta$ ratio can be reduced to a low value in the 8T cell, which is the reason why we can make the 8T cell smaller.

Note that, in this discussion about the write operation in the 8T cell, we assume that we utilize the divided-wordline structure [10] or write-back scheme [11]. The divided-wordline structure hierarchically accesses to a local WWL, where only intended columns are accessed. In the write-back scheme, we read data out of all columns in the first half period of a clock cycle. Then in the last half period, intended data are written to the intended columns and on the other columns, the readout data are written back. If the conventional single-wordline structure was utilized and write-in columns were limited (not all columns), data flips might occur by uncertain data on the other columns than the intended ones.

## 3. Area Comparison between 6T and 8T Cells

In this section, we compare the areas between the 6T and 8T cells over the feature processes. The design conditions are as follows:

- The channel lengths of the load, driver, and access transistors are all the same. Each channel length may not be set to an arbitrary value in a scaled process because of a limitation of lithography [12].
- The load transistor has the minimum channel width ($W_{\text{min}}$).
- In the 6T cell, $W_{\text{a}}$ is first optimized for the write margin under the condition of $W_{\text{d}} = W_{\text{min}}$. Then, $W_{\text{d}}$ is optimized for the read margin.
- In the 8T cell, we merely optimize $W_{\text{a}}$ for the write margin. $W_{\text{d}}$ is set to $W_{\text{min}}$ since the read margin can be neglected.
- The channel widths of Na3 and Nd3 at the read port in the 8T cell are set to $0.20\,\mu$m and $0.40\,\mu$m, respectively, at a 90-nm node, and scaled down by 0.7 time per generation.

Figure 8(a) shows the tendencies of the minimum channel widths in the 6T and 8T cells when the channel length ($L$) is varied. The condition is that both the read and write margins are only just managed in the 6T cell. In the 8T cell, we set it so that the write limit squeaks by the SF corner. As $L$ becomes smaller, $W_{\text{d}}$ and $W_{\text{a}}$ must be increased in order to suppress the $V_{\text{th}}$ variation. In contrast, in the 8T cell, as illustrated in Fig. 8(b), only $W_{\text{a}}$ is increased as much as the 6T-cell case.

Figure 9 illustrates the cell area dependency when the channel length is varied. The minimum areas in the 6T and 8T cells at the 65-nm, 45-nm, and 32-nm nodes are signified by the circles. In the 8T cells, the minimum area can be achieved by using the minimum channel length while in the 6T cell, they cannot because of the large $W_{\text{d}}$ and $W_{\text{a}}$. This demonstrates that the 6T cell is not able to be aggressively scaled down in the future processes. In contrast, the optimized transistors can be utilized in the 8T cell, and thus it is

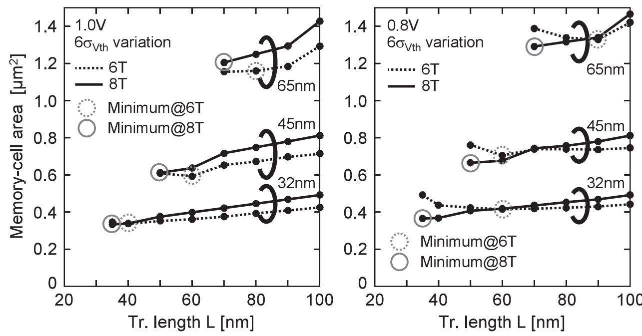



**Fig. 9** Cell area dependencies on the channel length.

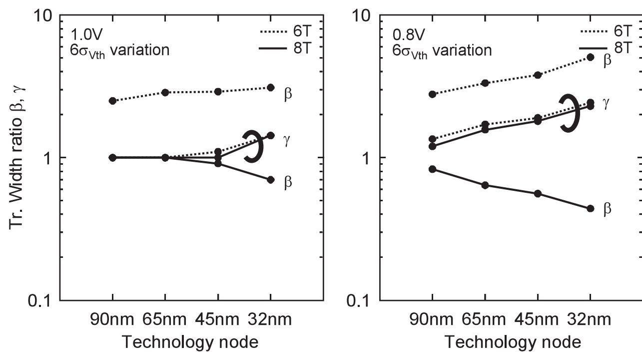



**Fig. 10** $\beta$ and $\gamma$ ratios in the minimum-area cells.

scalable.

Figure 10 shows the $\beta$ and $\gamma$ ratios in the minimum-area cells, and exhibits the superiority of the 8T cell from another point of view. The $\gamma$ ratios in the 6T and 8T cells have the same tendencies along with the advance of the process technology. However, the $\beta$ ratios display different behaviors. The $\beta$ ratio in the 8T cell is decreased as the process is advanced, while that in the 6T cell has to be increased, which makes the cell area larger.

The minimum cell areas between the 6T and 8T cells are compared in Fig. 11(a). At the 90-nm process node, the area of the 8T cell is larger than that of the 6T cell (compare Fig. 2(b) and Fig. 5(b)). However, at the 45-nm node, the lines in the figure intersect if the operating voltage is 1.0 V, and eventually the area of the 8T cell becomes smaller at the 32-nm node. If the operating voltage is set to 0.8 V, the 8T cell is superior to the 6T cell at the 65-nm node and later. Figures 12(a) and (b) are the layouts in the 6T and 8T cells at the 32-nm node when the operating voltage is 0.8 V. The 8T cell is smaller than the 6T cell by 14.6%. At the low voltage of 0.8 V, as depicted in Fig. 10, a larger $\beta$ and $\gamma$ ratios are required than the 1.0-V case in the 6T cells. This is the reason why the 8T cell becomes more advantageous at the lower operating voltage, in terms of cell area.

Another scenario about the minimum area in the 6T cell is the case that the channel length is set to the design rule, as shown in Fig. 11(b). The optimized transistor minimizes a read access time, but it results in a larger area, as already illustrated in Fig. 9. Figure 12(c) is the layout of the

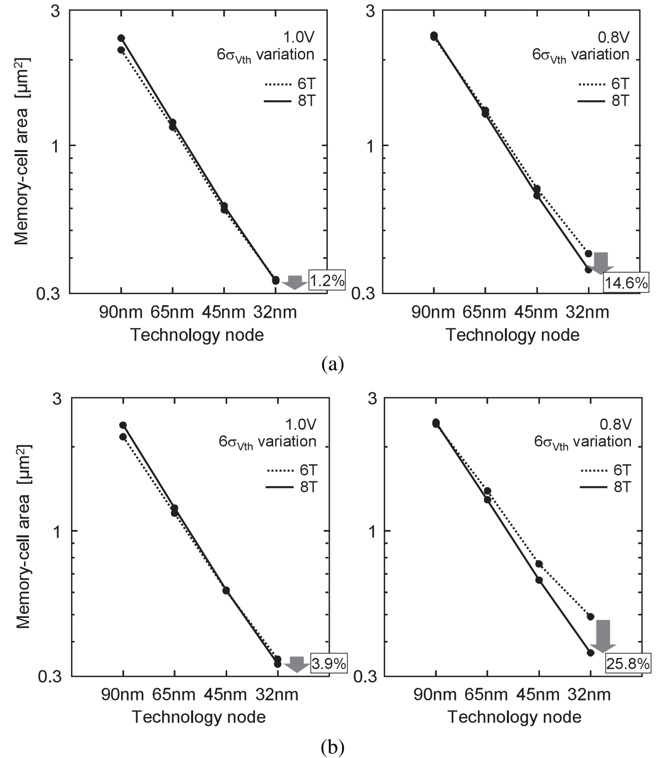



**Fig. 11** (a) Minimum-area comparison between 6T and 8T cells when the channel length can be arbitrarily set. The graph corresponds to the circles in Fig. 9. (b) The case that the channel length is fixed to the design rule.

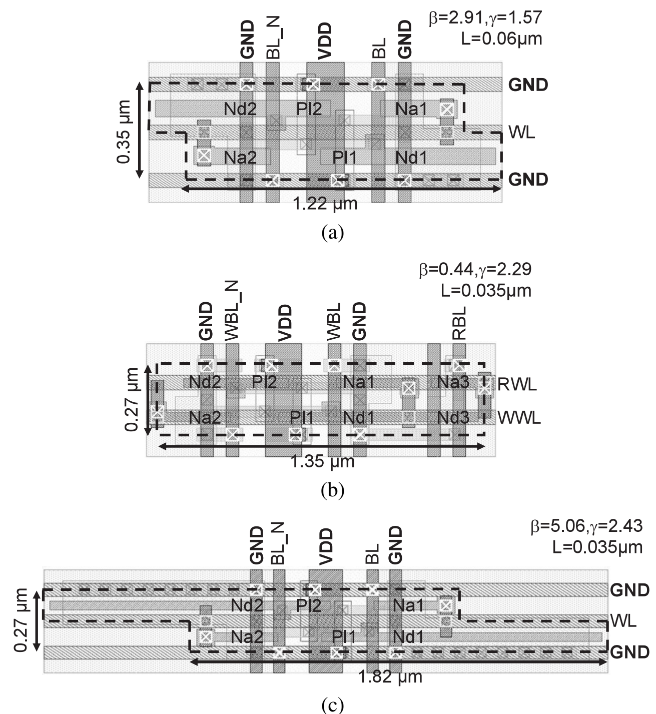



**Fig. 12** (a) and (b) are the minimum-area layouts in the 6T and 8T cells at the 32-nm node. (c) Another case of the 6T cell when the channel length is drawn in the minimum length. VDD is 0.8 V in all the cases.

**Table 1** Dimensions of 6T and 8T cells.

| Operating voltage | | | 1.0V | | | | 0.8V | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Technology node | | | 90nm | 65nm | 45nm | 32nm | 90nm | 65nm | 45nm | 32nm |
| 6T (L=Lmin) | Tr. width W [μm] | Access-NMOS | 0.20 | 0.16 | 0.13 | 0.11 | 0.27 | 0.24 | 0.19 | 0.17 |
| | | Drive-NMOS | 0.50 | 0.45 | 0.38 | 0.38 | 0.75 | 0.80 | 0.72 | 0.86 |
| | | Load-PMOS | 0.20 | 0.14 | 0.10 | 0.07 | 0.20 | 0.14 | 0.10 | 0.07 |
| | Tr. length L [μm] | | 0.10 | 0.07 | 0.05 | 0.035 | 0.10 | 0.07 | 0.05 | 0.035 |
| | β ratio | | 2.50 | 2.81 | 2.92 | 3.45 | 2.78 | 3.33 | 3.79 | 5.06 |
| | γ ratio | | 1.00 | 1.14 | 1.30 | 1.57 | 1.35 | 1.71 | 1.90 | 2.43 |
| | Cell area [μm²] | | 2.17 | 1.16 | 0.61 | 0.35 | 2.41 | 1.39 | 0.76 | 0.49 |
| 6T (Min. area) | Tr. width W [μm] | Access-NMOS | 0.20 | 0.14 | 0.10 | 0.10 | 0.27 | 0.20 | 0.16 | 0.11 |
| | | Drive-NMOS | 0.50 | 0.40 | 0.29 | 0.31 | 0.75 | 0.56 | 0.51 | 0.32 |
| | | Load-PMOS | 0.20 | 0.14 | 0.10 | 0.07 | 0.20 | 0.14 | 0.10 | 0.07 |
| | Tr. length L [μm] | | 0.10 | 0.08 | 0.06 | 0.04 | 0.10 | 0.09 | 0.06 | 0.06 |
| | β ratio | | 2.50 | 2.86 | 2.90 | 3.10 | 2.78 | 2.80 | 3.19 | 2.91 |
| | γ ratio | | 1.00 | 1.00 | 1.00 | 1.43 | 1.35 | 1.43 | 1.60 | 1.57 |
| | Cell area [μm²] | | 2.17 | 1.16 | 0.59 | 0.34 | 2.41 | 1.33 | 0.70 | 0.43 |
| 8T (L=Lmin, Min. area) | Tr. width W [μm] | Access-NMOS | 0.20 | 0.14 | 0.11 | 0.10 | 0.24 | 0.22 | 0.18 | 0.16 |
| | | Drive-NMOS | 0.20 | 0.14 | 0.10 | 0.07 | 0.20 | 0.14 | 0.10 | 0.07 |
| | | Load-PMOS | 0.20 | 0.14 | 0.10 | 0.07 | 0.20 | 0.14 | 0.10 | 0.07 |
| | Tr. length L [μm] | | 0.10 | 0.07 | 0.05 | 0.035 | 0.10 | 0.07 | 0.05 | 0.035 |
| | β ratio | | 1.00 | 1.00 | 0.91 | 0.70 | 0.83 | 0.67 | 0.56 | 0.44 |
| | γ ratio | | 1.00 | 1.00 | 1.10 | 1.43 | 1.20 | 1.50 | 1.80 | 2.29 |
| | Cell area [μm²] | | 2.39 | 1.20 | 0.61 | **0.33** | 2.45 | **1.29** | **0.67** | **0.36** |

6T cell at the 32-nm node, and shows the large areas caused by Nd1 and Nd2. In this worse case, the minimum-area in the 8T cell can be smaller by 25.8% than the 6T cell. Table 1 summarizes the dimensions discussed in this section.

## 4. Macro Area versus Access Time

This section discusses an area and access time comparisons between a 6T-cell array (6T-SRAM macro) and an 8T-cell array (8T-SRAM macro) at the 32-nm node. The 6T- and 8T-SRAM macros include the peripheral circuitry, such as address decoders, read/write circuitry, and so on. While the differential bitlines in the 6T cell can make faster readout, the 8T cell has a slower single-ended bitline for the read port as described in Sect. 2. This may result in longer access time in the 8T-SRAM macro because the voltage of the RBL should be full swing. To shorten the access time of the 8T-SRAM macro, we utilize the hierarchical-bitline structure [13] that hierarchically reads out a datum with a local RBL (LRBL) and global RBL (GRBL).

Figure 13 shows the ratios of the area and access time in a 128-kb (128 bits × 1024 words) 6T-SRAM and 8T-SRAM macros. In Fig. 13(a), we set the optimum channel length that minimizes the cell area, and set the minimum value ($L_{\min}$) in Fig. 13(b). In the simulation of the access time, the process corner is set to the SS corner since the access time becomes the worst case. As illustrated in Fig. 14, the local $V_{\rm th}$ variation of $6\sigma_{Vth}$ is also reflected on the access and driver transistors (connecting to the "L" storage) for the 6T cell and on the two transistors in the read port (Na3 and Nd3) for the 8T cell, so that the worst-case access time is further considered. A coefficient of $m$ in Fig. 14 is set to 4.24 to consider $6\sigma_{Vth}$ in the 6T and 8T cells. In this discussion, the access time is defined as the period, from the

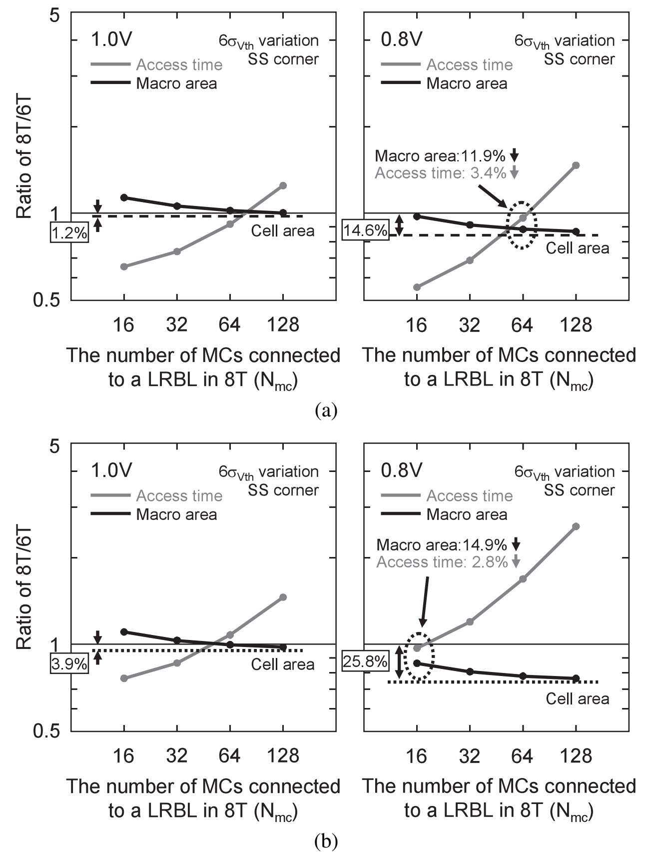



**Fig. 13** The area and access time comparison between the 128-kb 6T- and 8T-SRAM macros at the 32-nm node. The channel length is set to (a) the optimum value which enables the minimum cell area, and (b) the minimum value.

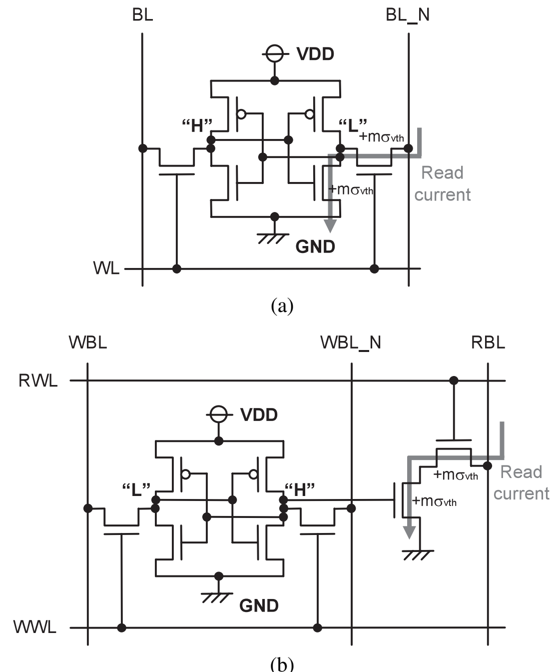



**Fig. 14** The worst-case conditions of local $V_{\rm th}$ variations considering the access time in (a) the 6T and (b) the 8T cells.

time when the wordline is asserted, to the time when the differential bitline voltage becomes 100 mV in the 6T-SRAM macro, or to the time when the GRBL voltage is dropped by a half of the operating voltage in the 8T case. The horizontal axis in Fig. 13 represents the number of memory cells connected to the LRBL in the 8T-SRAM macro ($N_{mc}$). The hierarchical-bitline structure, however, causes an area overhead in the 8T-SRAM macro. The width of the hierarchical-bitline circuitry in the direction of the LRBL is 1.71 times as long as that of the 8T cell. Note that the hierarchical-bitline structure is not implemented in the 6T-SRAM macro.

As $N_{mc}$ in the 8T-SRAM macro is increased, the access time of the 8T-SRAM macro becomes longer, while the macro area becomes smaller due to the smaller overhead of the hierarchal-bitline circuitry. If $N_{mc}$ = 128, the area ratio of the 8T-SRAM macro is almost equal to the ratio of the cell area (compare to the values in Fig. 11). That is, the area overhead of the hierarchical-bitline structure is negligible in that case.

Basically, as illustrated in Fig. 13, the relation between the macro area and access time is a trade-off. However, in Fig. 13(a), since the channel length is set to the optimum value and is longer than the minimum value ($> L_{min}$), the access time of the 6T-SRAM macro becomes longer, which turns out to a smaller access-time ratio. When $N_{mc}$ is set to 128 and the operating voltage is 0.8 V, we can obtain both the small macro area and short access time by 11.9% and 3.4%, respectively.

## 5. Conclusions

We clarified that an area of an 8T cell can be smaller than that of a 6T cell in a future process with a larger $V_{th}$ variation, regardless of the additional two transistors at a separate read port. In a 32-nm process, the 8T cell is smaller than the 6T cell by 14.6% at a supply voltage of 0.8 V. We also made the area and access time comparisons between the 6T-SRAM and 8T-SRAM macros, and the area reduction of the 8T-SRAM macro than 6T-SRAM macro is 11.9% when the access time is shorter by 3.9% in 0.8-V operation.

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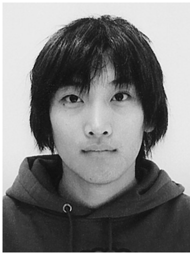

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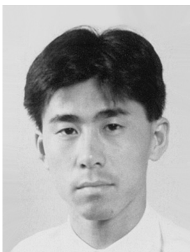

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