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A 433-MHz Rail-to-Rail Voltage Amplifier with Carrier Sensing Function for Wireless Sensor Networks

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SUMMARY In this paper we propose a novel functional amplifier suitable for low-power wireless receivers in a wireless sensor network. This amplifier can change input threshold level as carrier sensing level, since it has a minimum input amplitude to be amplified. A simple rail-to-rail output is suitable for a subsequent digital interface. The target frequency is 433 MHz, and the maximum voltage gain is 11 dB. The standby power is 39.5 nW, and the active power is 352 μW. The chip area is $82 \times 24\,\mu m^2$.
key words: *wireless sensor network, amplifier*

1. Introduction

Recent advances in microsensors, integrated circuits, and wireless communication technologies realize WSNs (wireless sensor networks) composed of a group of low-power sensor nodes [1]. One of the most important issues on the WSNs is the extension of their available period, that is, network lifetime to the longest period possible under the condition that each sensor node has only a strict energy budget. For this reason, it is effective to reduce the power of an RF (radio frequency) block in a sensor node since it is the major power-consuming block on the whole.

1.1 Standby Power

In WSNs, sensor nodes are intermittently activated since their data rate is low. Their activation ratio is merely 10^{-3} [2], and sensor nodes enter a standby mode in the rest period. Hence, a low standby power is important, which must be less than 10^{-4} of the active power. Otherwise, the standby power becomes predominant, and the lifetime of WSNs becomes shorter.

1.2 Carrier Sensing Function

We should avoid data collisions and interferences in WSNs so as not to waste the power budget. While one node is transmitting data, it is desirable that other nodes around it do not communicate with each other. One method to solve the problem is a carrier-sensing approach, which is widely utilized in many MACs (media access controls). All nodes make a carrier sense before they transmit data. If they detect a carrier, they defer the transmission of a packet. A typical carrier-sensing scheme is to measure an RSSI (received signal strength indicator). A channel is considered busy if the detected energy in the channel is above a threshold; otherwise it is considered idle. The RSSI carrier sense requires an additional A/D converter to detect the energy in the channel, which consumes significant power. Thus, this kind of carrier sense is unsuitable for a low-power wireless sensor node. We will describe another approach in this paper.

2. Conventional Amplifiers for Wireless Sensor Networks

In conventional research, low-power RF receivers for WSNs have been proposed [3], [4]. They adopt OOK (on-off keying), where data are modulated by the existence of a signal (e.g., "Hi" when there is a signal, and "Lo" when there is no signal). OOK is a simple modulation, and thus can be implemented with simple and low-power hardware. In [4], an LVA (low-voltage amplifier) is adopted as the first-stage amplifier in a receiver, after which there are inverter-type voltage amplifiers connected in series with no inductors. This circuit adopts an incoherent architecture, but is "digitally" analog. It works rail to rail at a frequency of 433 MHz. Figure 1 shows an inverter-type voltage amplifier with nMOS power switches; in the standby mode, these switches are cut off by the /Standby signal to reduce short current. This amplifier requires no bias adjustment because it has a feedback loop made of a resistor, and can automatically set bias voltage to half of the supply voltage. This type of amplifier has a high voltage gain, and is well utilized in a piezoelectric oscillator, but always draws short currents. Therefore, a large power is consumed even if no signal is input, and the chain of the inverter-type voltage amplifiers reaches 94% of the total power in the receiver [4].

Instead of an inverter-type voltage amplifier, a latch-type voltage amplifier in Fig. 2 for suppressing short current has been proposed [5]. It has bistability owing to its latch property, and the two bias points are fixed at V_h and V_l, at which a lower short current flows through the main amplifier. This is because V_h and V_l in the feedback inverter are slightly shifted from the middle of the supply voltage, but they are supplied externally in [5]. When a signal is input, the main amplifier amplifies it, and at the same time drives the feedback inverter. The feedback inverter helps the input signal be latched by its feedback. However, this con-

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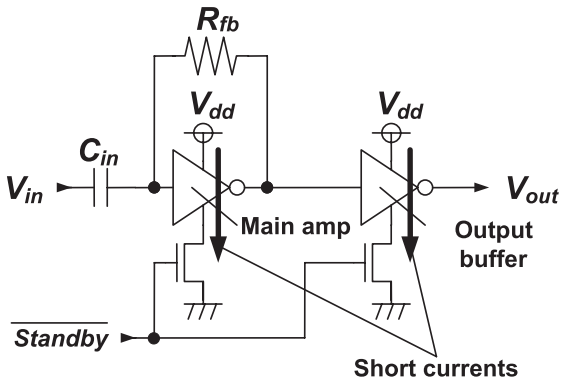

Fig. 1 Schematic of conventional inverter-type voltage amplifier.

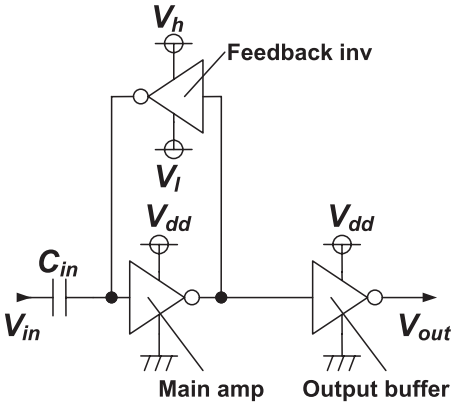

Fig. 2 Schematic of latch-type voltage amplifier.

ventional latch-type voltage amplifier only accepts a square wave. When a sinusoidal wave is input, the two bias voltages fluctuate owing to the phase error between the input and feedback signals. Therefore, we cannot use this latch-type voltage amplifier in an RF application.

3. Proposed Voltage Amplifier: Bistability Amplifier (BSAMP)

We propose a low-power voltage amplifier with a carrier sensing capability for OOK, named a BSAMP (bistability amplifier). The schematic is illustrated in Fig. 3(a). In the conventional and proposed schemes, the transistor sizings in the main amplifiers are all the same. To the conventional amplifiers, however, C_{fb} and R are added to stabilize the bias points and accept a sinusoidal wave. In the design of the proposed amplifier, the data rate of OOK is 20 kbps. R and C_{fb} in Fig. 3, which have a role of a high-pass filter, do not pass the data rate of 20 kbps to avoid low-frequency undulation. However, the high-pass filter passes the carrier frequency of 433 MHz, whose gain is –40 dB at the frequency of 20 kHz.

The intermediate voltages (V_h and V_l) are supplied by a voltage generator described below. The BS-aid (bistability aid) helps to bias the main amplifier and stabilizes the state of the main amplifier with its positive feedback. The main amplifier amplifies the input voltage (V_{in}), and drives the

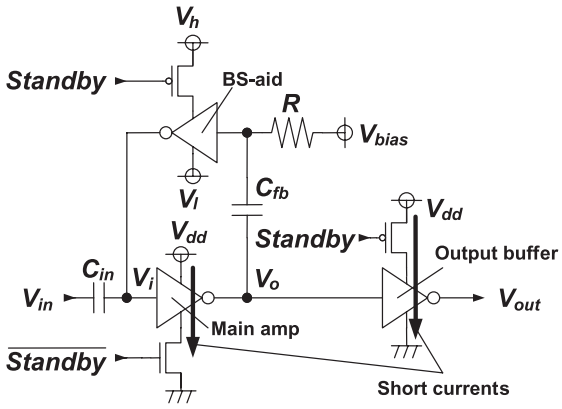

Fig. 3 Schematic of bistability amplifier (BSAMP).

output buffer. We take all parasitic elements and parasitic effects into account in simulations carried out with Synopsys HSPICE. In this section, we compare the proposed BSAMP with the conventional voltage amplifier in Fig. 1 by circuit simulations.

3.1 DC Characteristic

Figure 4(a) shows the operating points of the main amplifier and BS-aid at a supply voltage of 1.0 V. The main amplifier in the conventional scheme has the same DC characteristic as that in the proposed scheme because their transistor sizings are identical. The operation curves of the main amplifier and BS-aid intersect at two points. In the BSAMP, every time the amplitude of V_o exceeds V_a (= $(V_h–V_l)/2$), the bias points of the main amplifier alternate. The voltage gain at the bias point is almost the same as the conventional one because V_a is small (= 25 mV) and the bias points are close to the maximum slope at $(V_h + V_l)/2$.

Figure 4(b) shows the bias currents flowing through the main amplifier and BS-aid. The bias current flowing through the main amplifier is reduced to 232 μA (5% down from the maximum) owing to the shifted bias voltage, which also lowers the short current flowing through the output buffer. Meanwhile, the output buffer in the conventional amplifier draws a large short current owing to its bias point. As shown in Fig. 5, since the output buffer of the BSAMP is biased at 0.67 V as the input voltage, the short current is reduced by 86.4%, compared with the conventional one. The bias voltage of the BS-aid is fixed at V_{bias} (= V_h = 0.476 V), but the bias current through it is very small in nature because the supply voltage is 50 mV (= $V_h–V_l$).

In the proposed BSAMP, the zigzag cut-off scheme can be accommodated in a way that minimizes standby current [6], whereas in the conventional one, this is not possible and two nMOS are inserted as a power gating (see Fig. 1). The bias voltage fluctuates in the multistage inverters of the conventional amplifier if the zigzag scheme is applied, which would result in a low voltage gain. In the conventional scheme, the main amplifier biased at the point of the maximum leakage current is drawn by its feedback resistor

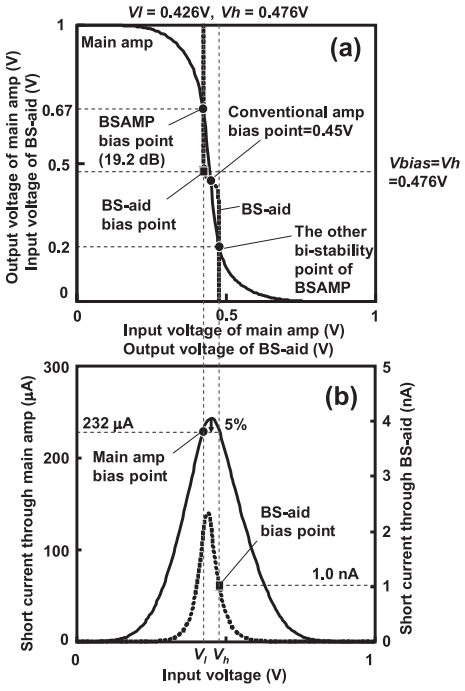

Fig. 4 DC characteristics of BSAMP. (a) Bias voltages, and (b) bias currents.

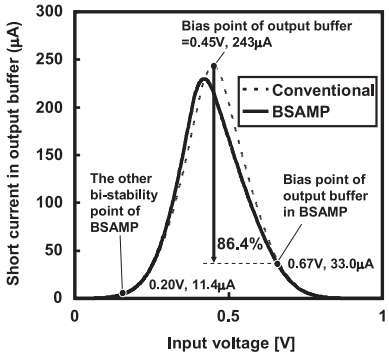

Fig. 5 Bias currents in output buffers.

even if the the nMOS switch is turned off in the standby mode. In contrast in the proposed BSAMP, the zigzag cut-off scheme is quite effective since the bias voltage of the BS-aid is moved to V_l by the cut-off pMOS in the BS-aid, which slightly turns off the nMOS in the main amplifier. At the same time, the nMOS switch in the main amplifier is also turned off; hence, the series of the slightly off nMOS and completely off nMOSs reduces leakage current more than the conventional amplifier, in the standby mode. Moreover, the two pMOSs in the output buffer are turned off, which completely cuts off the standby leakage current in it. This mechanism takes advantage of the zigzag cut off scheme in which two transistors are always off in a leakage path. The settling time from the standby mode to the active mode is 20 μs, which is shorter than the interval of one bit when the data rate is 20 kbps, and thus the delay penalty and power overhead are negligible when initiating communication.

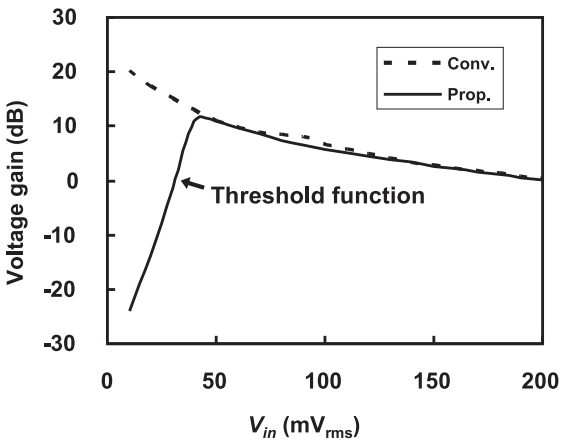

Fig. 6 Voltage gain characteristics.

The power consumed by the bias current and the standby power including the output buffer are 277 μW and 23.1 nW, whereas they are 547 μW and 178 nW in the conventional one. This demonstrates that we save 46% of the bias power and 87% of the standby power, respectively.

3.2 Operation in Active Mode

In the BSAMP, when V_{in} is input to the main amplifier and the amplitude of V_o is less than V_a, the BS-aid tries to convert V_{in} to its bias voltage using feedback because the bias point is a stable point. That is, the main amplifier is biased at V_l, and outputs a higher value; the output buffer has a negative gain owing to the high V_o.

In contrast, when the input voltage (V_i) is larger than V_a, the bias point is shifted to another stable point, V_h. In the meantime, the bias voltage of the main amplifier is changed between V_l and V_h, which drives the output buffer causing it to have a positive gain.

Figure 6 shows the voltage gain characteristics at an operating frequency of 433 MHz, and exhibits a threshold function. In the figure, when the input amplitude (= V_{in}) is around V_a (= 25 mV), BSAMP has a threshold. We can exploit this salient feature as a carrier sense. As input amplitude increases, voltage gain decreases owing to output saturation since the proposed amplifier is rail to rail. We can obtain a maximum voltage gain of 11 dB when the input amplitude is 50 mV in this simulation. Note that we presume that there is a LVA just before the BSAMP, since even a value of 50 mV is large.

Figure 7 shows the frequency characteristic in terms of voltage gain in the conventional and proposed amplifiers. The input amplitudes are set to 50 mV in both. At 433 MHz, no bandwidth degradation of the BSAMP is observed; however, beyond 1 GHz, the characteristic declined. This is because the conductance of the BS-aid is very small (= 1.0 nA, see Fig. 4(b)). The supply voltage of the BS-aid is only 50 mV, and its bandwidth turns out to be low. The bandwidth of the BS-aid would be improved by increasing V_h–V_l, but threshold voltage also becomes large, which is

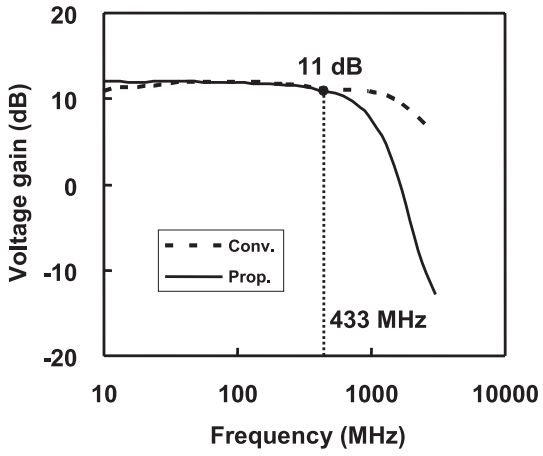

Fig. 7 Frequency characteristics.

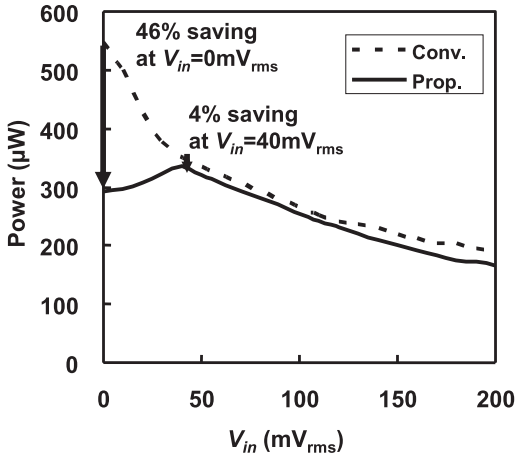

Fig. 8 Power characteristics.

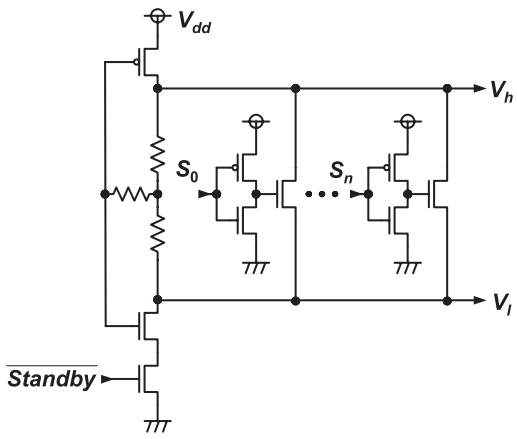

Fig. 9 Schematic of voltage generator.

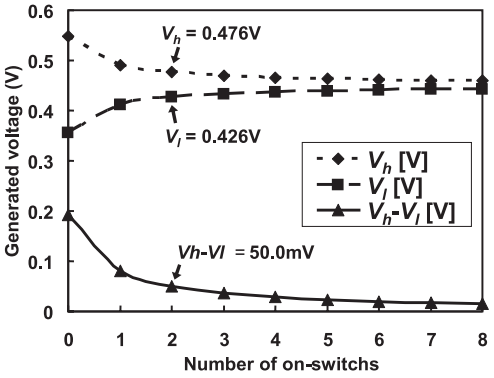

Fig. 10 Output characteristics of voltage generator.

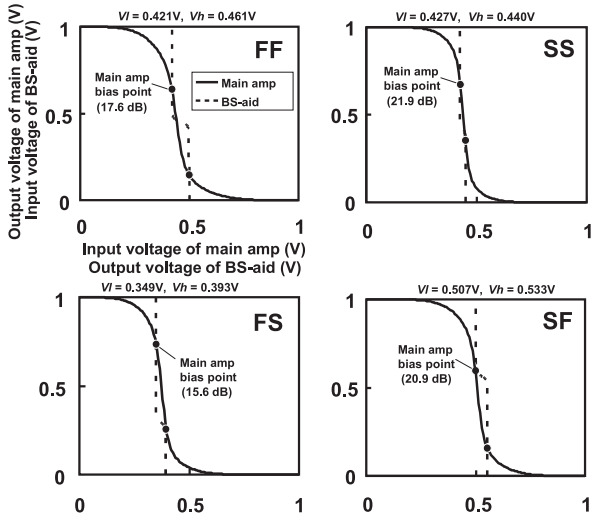

Fig. 11 DC characteristics at process corners. Data in parentheses indicate the voltage gain of the main amplifier at each process corner.

no use for a small signal in an RF application.

Figure 8 shows the power characteristics when input amplitude (V_{in}) is changed. The active powers are almost the same when V_{in} is greater than 50 mV because of the saturation. Note that this indicates a situation when the signal is "Hi" (a case in which the signal is 40 mV$_{\rm rms}$ or more). If there is no signal (signal "Lo") in an active mode and V_{in} is zero, the active power at the signal "Lo" is the same as the short power mentioned in the previous subsection. Because the saving factor is larger at the signal "Lo," we can save more active power as the duty ratio of a signal becomes smaller. When an input signal is changed from "Hi" to "Lo," it takes 10 μs until the BS-aid settles at the bias point. In the case of "Lo" to "Hi," it takes 1 μs. This means that the maximum data rate is limited to 100 kbps in this design.

3.3 Voltage Generator

Figure 9 shows the circuit diagram of the voltage generator for the BS-aid that can generate V_h and V_l. Because $V_a = (V_h – V_l)/2$, we can change V_a programmatically with a combination of S_i ($i = 0, \ldots, n$) by controlling the impedance between V_h and V_l nodes. In a wireless sensor network application, the required carrier sensing level is different because transmitting power and distance are varied. S_i has to be fixed according to specifications. By using a programmable voltage generator, we can adjust the minimum input amplitude. S_i may be utilized for trimming the carrier sensing

level. Other than this, a microcontroller can dynamically change S_i, on the basis of the condition of the communication channel.

Figure 10 shows the output characteristics of the voltage generator. V_h–V_l can be changed from 16 mV to 193 mV with eight nMOS switches. When the resistors in the voltage generator are varied, output voltage is changed as well, but the resistors are also adjustable using the S_i switches.

If a process corner of transistors is varied, the outputs (V_h and V_l) of the voltage generator are changed. However, the bias voltage of the main amplifier should be properly set, and the main amplifier should have a voltage gain. Fig. 11 shows the DC characteristic of the BSAMP at four process corners (FF, SS, FS, and SF corners: e.g. FS means fast nMOS and slow pMOS). Depending on the process corner, bias voltage is varied, but the bistability is always sustained; the main amplifier has a voltage gain in any case. This is because the voltage generator and main amplifier have the same circuit configuration to cope with process variability.

The power of this programmable voltage generator is 12.5 μW even in an active mode owing to the low-power characteristic of the BS-aid. In the standby mode, leakage power can be suppressed to 0.5 nW with the standby signal and S_i signals.

4. Measurement Results

Figure 12 shows a chip photograph and a layout of the BSAMP in a 0.15-μm process technology. The area is about $82 \times 24\,\mu m^2$. The extra BS-aid and C_{fb} (= 1.6 pF) has an area overhead of 16%, compared with the conventional amplifier. We measured this circuit using probers, where V_{in} is fed from a signal generator, and V_{out} is observed. V_h, V_l, and V_{bias} are set to the values in Fig. 4.

Figure 13 shows the measured voltage gain characteristics at an operating frequency of 433 MHz. In a very low V_{in} region, the voltage gain is larger than the simulation gain. This is the measurement limitation of the high-impedance probe.

Figure 14 shows the measurement result of the frequency characteristics. The voltage gain was 11 dB at an operating frequency of 433 MHz. Figure 15 shows the measured power characteristics of the BSAMP. Power can be reduced when the input voltage is small. The BSAMP achieved a 46% power reduction over the conventional amplifier when the input voltage is zero. We observed that the measured power consumed more than the simulation in a

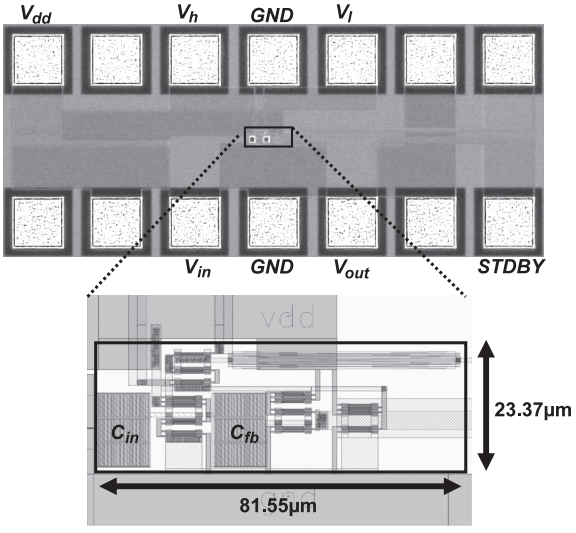

Fig. 12 Chip photograph and layout of BSAMP.

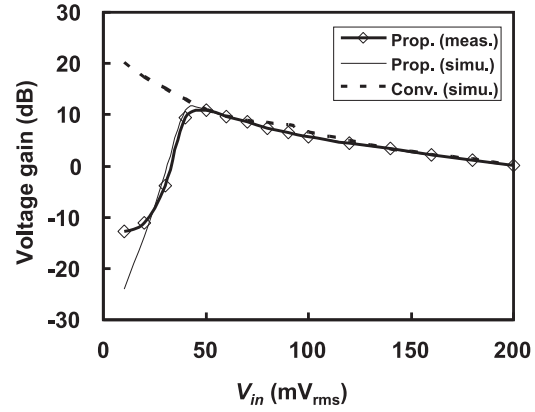

Fig. 13 Measurement result of voltage gain.

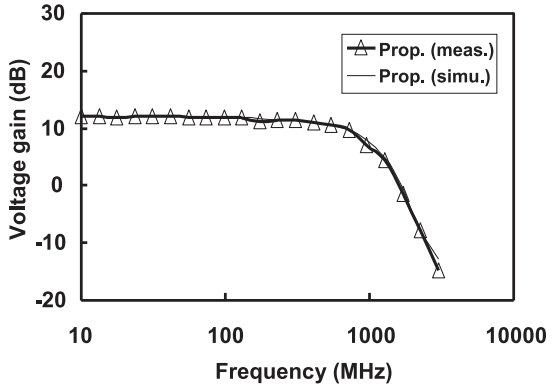

Fig. 14 Measurement result of frequency characteristics.

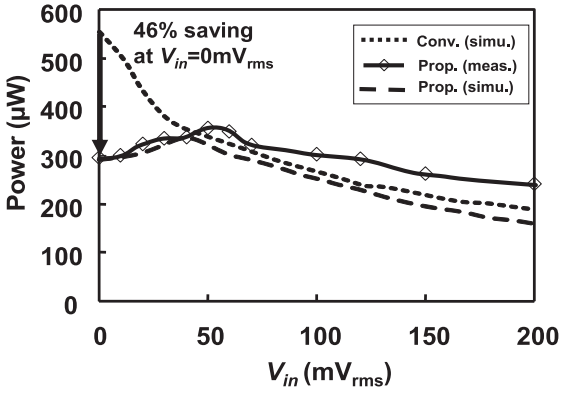

Fig. 15 Measurement result of power.

Table 1 Total power consumption.

	Standby		Active				
	AMP	Voltage gen.	AMP Sig. "Lo" ($0mV_{rms}$)	AMP Sig. "Hi" ($40mV_{rms}$)	Voltage gen.	Average of active	Total***
Conv.*	178 nW	-	547 μW	350 μW	-	449 μW	627 nW
Prop.**	39 nW	0.5 nW	295 μW	352 μW	12.5 μW	336 μW	376 nW
Saving	78%	N/A	46 %	-0.5 %	N/A	25 %	40 %

* Simulation
** Measurement data
*** Activation ratio = 10^{-3}

high-V_{in} region; however, the whole power was suppressed when V_{in} was less than 50 mV.

The power savings are summarized in Table 1. The standby power is about 10^{-4} of the active one. To calculate total power, we assumed that the activation ratio is 10^{-3} for the wireless sensor network. We can achieve a total of 40% saving when we utilize the proposed BSAMP.

5. Conclusion

In this paper, we proposed the bistability amplifier BSAMP. The maximal voltage gain is 11 dB at an operating frequency of 433 MHz. The standby and active powers at the signal "Hi" are lower than the conventional inverter-type voltage amplifier by 78% and 46%, respectively. The operating power is 376 nW when the activation ratio is 10^{-3}. The proposed BSAMP has a carrier sensing function without adding other circuits since it inherently has a minimum input amplitude to be amplified. This function is important to avoid collisions and interferences that cause needless communications.

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