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# A Dependable SRAM with 7T/14T Memory Cells

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**SUMMARY** This paper proposes a novel dependable SRAM with 7T/14T memory cells, and introduces a new concept, "quality of a bit (QoB)" for it. The proposed SRAM has three modes: a normal mode, high-speed mode, and dependable mode, and dynamically scales its reliability, power and speed by combining two memory cells for one-bit information (i.e. 14 T/bit). By carrying out Monte Carlo simulation in a 65-nm process technology, the minimum voltages in read and write operations are improved by 0.21 V and 0.26 V, respectively, with a bit error rate of $10^{-8}$ kept. In addition, we confirm that the dependable mode achieves a lower bit error rate than the error correction code (ECC) and multi module redundancy (MMR). Furthermore, we propose a new memory array structure to avoid the half-selection problem in a write operation. The respective cell area overheads in the normal mode are 26% and 11% in the cases where additional transistors are pMOSes and nMOSes, compared to the conventional 6T memory cell.

***key words:*** *SRAM, dependability, quality of a bit*

## 1. Introduction

As silicon LSIs support massive infrastructure in society, we have paid attention to dependable computing systems. However, the advanced process technology tends to cause accidental errors like a soft error and negative bias temperature instability (NBTI), more frequently. In addition, there might be some errors left in a design, manufacturing, or test phase. It is supposed to be almost impossible to perfectly eliminate these human-induced errors in a future complicated LSI. That is, a product will be shipped with some errors, and accidentally malfunction. We no longer expect error-free LSIs with sufficient operating margins.

Since reliability is varied with operating conditions (speed, supply voltage, temperature, and even altitude corresponding to a soft error), it is desirable to dynamically improve the reliability on worse conditions. Furthermore, required reliability depends on application software, which indicates that the reliability should be changed in accordance with an application.

Considering this background, we propose an SRAM that can dynamically control its reliability and speed. SRAM has recently dominated operating margins of a chip due to a large number of transistors [1]–[7]. Namely, the proposed SRAM can change quality of its information, in terms of reliability, speed, and/or power.

In the next section, we mention the overview of proposed SRAM. In Sect. 3, we propose a novel 7T memory cells that can dynamically improve the quality of information, and we introduce a new concept called "quality of a bit" (QoB). In Sect. 4, we discuss the reliability of the proposed memory cell, from viewpoints of bitline delay time and bit error rates. In Sect. 5, we describe a new memory cell array structure to avoid the half-selection problem in a write operation. Section 6 exhibits measurement results. The final section summarizes this paper.

## 2. Dependable SRAM: Overview

Operating conditions affect reliability of an SRAM, while the reliability depends on application software that uses the SRAM. For example, an encryption program and a screen saver program demand different levels of reliability. This means that the reliability is changed by the operating conditions, and is dependent on the application.

On the other hand, in order to save a power of an SoC, dynamic voltage and frequency scaling (DVFS) that adaptively controls an operating frequency and supply voltage has been implemented [8]. However, an SRAM might not work correctly in a lower operating voltage, because operating margins of memory cells are degraded due to threshold-voltage variation of MOSFETs as a fabrication technology is scaled down. Therefore, at the lower voltage, it is necessary to keep the reliability.

In our proposed SRAM, the reliability of an SRAM can be dynamically changed on a block-by-block basis, as illustrated in Fig. 1. In the normal-dependability blocks (Blocks 0–3), assignment is as usual as one memory cell has one bit. On the other hand, in the high-dependability blocks (Blocks 4 and 5), one-bit information is stored in two memory cells by combining a pair of memory cells. This mechanism realizes the high dependability, while the memory capacity becomes a half in the high-dependability blocks.

This dynamic switching between the typical dependability and high dependability opens up new resource allocation in an SRAM. For instance, an operating system (OS) or firmware can allocate an encryption program to the high-dependability block. An application software can also change the reliability of its data by a system call. Encryption data or personal information should be in the high-dependability block. If memory utilization of programs and

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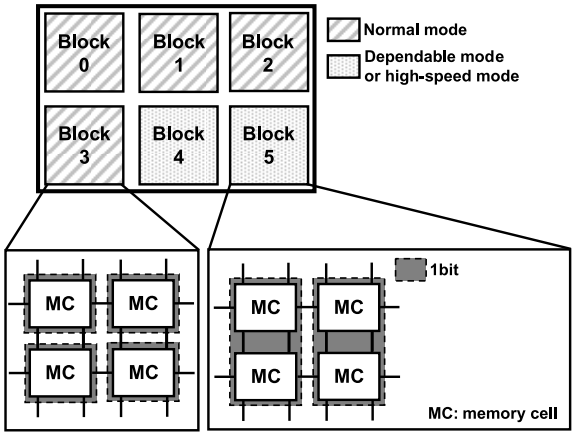



**Fig. 1** A dependable SRAM.

data is 50% or less, the high-dependability mode can be aggressively exploited by the OS or firmware, without the memory-capacity overhead. A small code with small data always runs in the high-dependability mode.

In the next section, we explain how to achieve the proposed dependable SRAM on a circuit level.

## 3. Memory Cell and the Concept of the Quality of a Bit (QoB)

### 3.1 Conventional 6T Memory Cell

Figure 2 is a pair of the conventional 6T memory cells. The layout is based on a logic design rule in a 65-nm process technology. Usually, only one memory cell (MC) is accessed (for instance, WL[0] = "H," WL[1] = "L") in write and read operations. We call this conventional scheme "a 1-MC mode."

As well, we can set both WL[0] and WL[1] to "H" at the same time, in which case, we can write a same datum to the two memory cells (2-MC mode). After that, a larger cell current can be obtained in read operation by enabling the two wordlines. This means that we can trade off the speed against the cell area.

Figure 3 shows the distributions of cell currents in the 1-MC and 2-MC modes. The worst case cell current in the 2-MC mode is increased by 133%. Statistically, it is very unlikely that a pair of memory cell is both the worst case. This is the reason why the cell current is more than double. In other words, a local variation (random variation) is suppressed by combining a pair of memory cells. The 2-MC mode achieves a faster access time in the read operation.

Another merit in the 2-MC mode is a self-recovery effect. In the 1-MC mode, if a memory cell has a large variation and is not marginal (bad cell), datum stored in it is sometimes flipped in read operation [4]. On the other hand, in the 2-MC mode, the datum in the bad cell is recovered by another good cell in a pair with a high probability since the existing probability of the bad cell is far lower than that of the good cell in general use. Figure 4(a) illustrates the

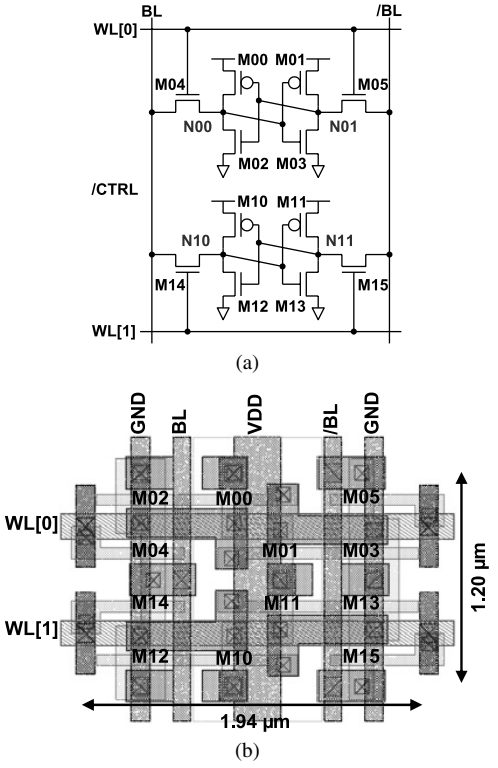



**Fig. 2** A pair of the conventional 6T memory cells: (a) schematic and (b) layout.

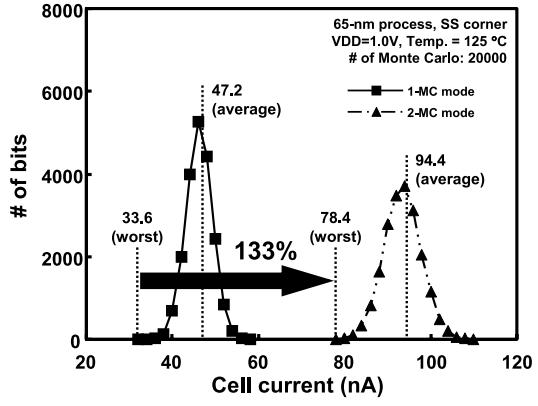
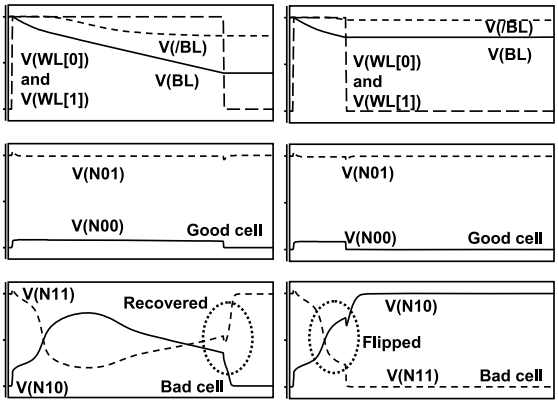



**Fig. 3** Cell current distributions in 1-MC mode and 2-MC mode.

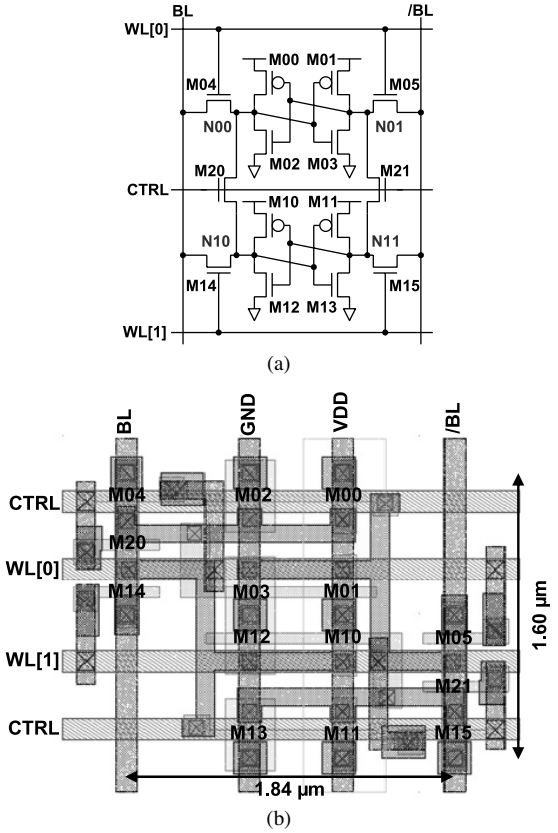
self-recovery effect in the 2-MC mode. Even if the bad cell is not marginal and is once flipped, the storage data is sustained after all, and can be properly read out.

However, note that the self recovery takes long time in the 2-MC mode comprised of the conventional 6T memory cells, because the internal nodes in the bad cell are slowly recovered by the good cell through the two access transistors and bitline. After the voltage difference opens significantly between the differential bitlines, the self recovery takes place. This infers that the cycle time becomes slow for the proper operation. In addition, if wordline pulse width is not sufficient for the self recovery, the datum in the bad cell is turned out flipped as shown in Fig. 4(b). This means that




(a) (b)

**Fig. 4** Operating waveforms in the 2-MC mode: (a) self recovery (long wordline pulse width) and (b) datum flip (short wordline pulse width), in a bad cell.



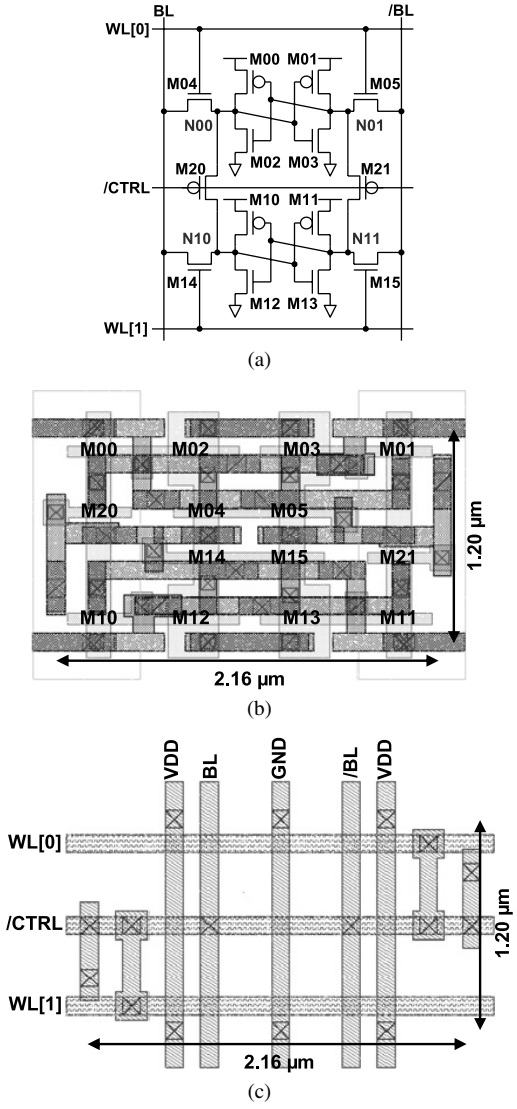

(a) (b)

**Fig. 5** Dependable 7TN/14TN memory cells (additional transistor: nMOS): (a) schematic and (b) layout.

it is difficult to set the wordline pulse width considering the time of the self recovery. In the next subsection, we proposed a novel memory cell, in which the internal nodes are directly connected with additional transistors.

### 3.2 Dependable 7T/14T Memory Cell

The proposed 7T memory cells are shown in Figs. 5 and 6; two nMOSes or pMOSes connect the internal nodes in the




(a) (b) (c)

**Fig. 6** Dependable 7TP/14TP memory cells (additional transistor: pMOS): (a) schematic, (b) layout in lower layers (diffusion layer to the second metal layer), and (c) layout in upper layers (the third and fourth metal layers).

pair of memory cells ("N00 and N10," "N01 and N11"), respectively. Hereafter, we name these memory cells, 7TN cell and 7TP cell. Compared with the conventional 6T memory cell, the respective area overheads are 26% and 11%, in the case of the logic design rule. A pair of 7TNs is 14TN, and a pair of 7TPs is 14TP, which are for the high-speed and dependable modes.

The proposed 7T/14T memory cells have three modes shown in Table 1.

- Normal mode (7T); the additional transistors are turned off (CTRL = "L" or /CTRL = "H"), and the 7T cell acts as the conventional 6T cell.
- High-speed mode (14T); the additional transistors are turned on (CTRL = "H" or /CTRL = "L"), and the internal nodes are shared by the memory cell pair. Both WL[0] and WL[1] are driven, which enables faster

**Table 1** Three modes in 7T/14T memory cell.

| | # of MCs comprising 1 bit | # of WL drives | CTRL (/CTRL) |
|---|---|---|---|
| Normal | 1 (7T/bit) | 1 | "L" ("H") |
| High-speed | 2 (14T/bit) | 2 | "H" ("L") |
| Dependable | 2 (14T/bit) | 1 | "H" ("L") |

readout using 14 transistors.

- Dependable mode (14T); the additional transistors are activated, but either WL[0] or WL[1] is asserted. By doing so, a larger static noise margin can be obtained because a $\beta$ ratio is doubled.

In the normal mode, one-bit datum is stored in one memory cell, which is the most area-efficient. In the high-speed mode and dependable mode, one-bit datum is stored in two memory cells although the quality of the information is different from the normal mode. The "higher-speed" or "more dependable" information can be obtained. We call this concept "quality of a bit (QoB)." The quality of the information is scalable in our proposed memory cell [9].

There are other high-reliable techniques using some area overhead: the error correction code (ECC) and the multi module redundancy (MMR). However, the ECC degrades an access time, and does not have the scalability of dependability. The reliability is always fixed. Moreover, the both ECC and MMR have to pay power overhead. In Sect. 4.4, the comparison of reliability among the proposed 7T/14T cell, ECC and MMR are discussed in detail.

## 4. Comparison between Conventional 6T Cell and Proposed 7T/14T Memory Cell

In this section, we discuss the quality of our proposed memory cells from view points of a speed and bit error rates in read, write operations and retention.

### 4.1 Bitline Delay

As shown in Fig. 3, the worst case cell current is increased more than double by asserting the both WL[0] and WL[1]. Fig. 7 compares the worst-case bitline delays (SS corner, VDD = 1.0 V, 125°C) in the read operation. In the comparison, the bitline length and the number of memory cells on the bitline are the same for the 7TP and 14TP cells (the memory capacity of the 14TP cells becomes a half of the 7TP cells). The bitline delay is defined as a period from a time at which a WL rises to VDD/2 to a time at which a differential voltage between BL and /BL is expanded to 100 mV. The worst-case bitline delay time is improved by 53% in the high-speed mode. Furthermore, the high-speed mode has higher tolerance of bitline leakage, thanks to the on current improvement. The ratio of the cell current versus bitline leakages is increased [3]–[5].

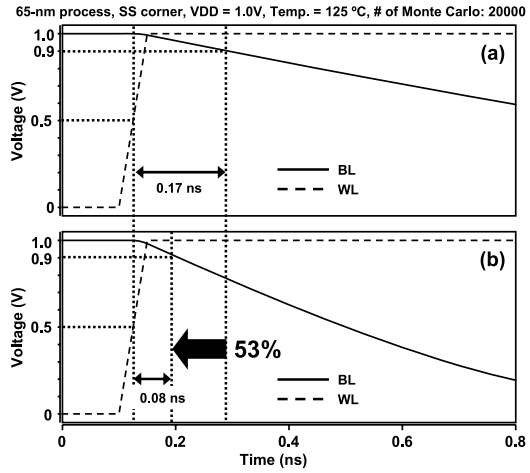



**Fig. 7** The worst-case bitline delay simulations: (a) 7TP cell and (b) 14TP cell in high-speed mode.

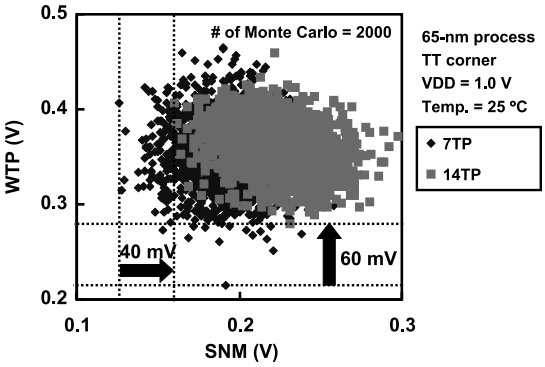



**Fig. 8** Static noise margins (SNMs) and write trip points (WTPs) in 7TP and 14TP cells.

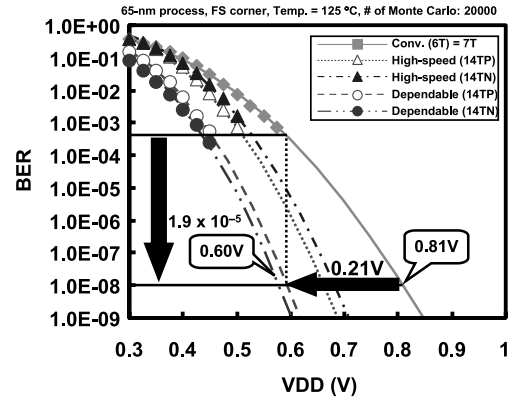
### 4.2 Bit Error Rates (BERs)

Figure 8 shows comparisons of static noise margins (SNMs) and write trip points (WTPs) [10], [11] in the 7TP and 14TP cells, under the typical conditions. The number of Monte Carlo simulation samples is 2,000. The SNMs of the 14TP cells are simulated with the dependable mode, and the WTPs of it are simulated with the high-speed mode. The 14TP cell achieves larger SNM and WTP by 40 mV and 60 mV, respectively.

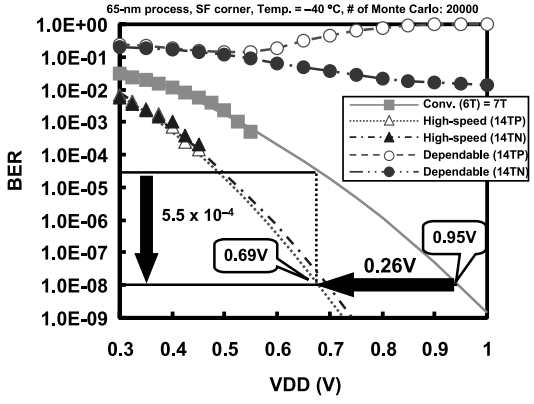
Figure 9 shows bit error rates (BERs). The BERs of the proposed 7TP and 7TN cells are almost the same. Hence, we will describe the comparison between 6T and 14T cells. All dots in the figures are derived from Monte Carlo simulation using HSPICE. The extrapolated line shows an approximated BER function, $BER(VDD)$, as follows:

$$\begin{cases} f(x) = \begin{cases} \dfrac{1}{\sqrt{2\pi}\sigma}\mathrm{EXP}\left[-\dfrac{(x-\mu)^2}{2\sigma^2}\right] & (x \geq \mu) \\ 0 & (x < \mu) \end{cases} \\ BER(VDD) = \int_{VDD}^{\infty} f(x)dx \end{cases} \quad (1)$$

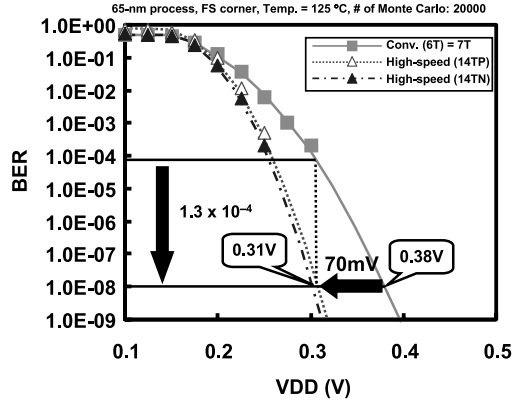
where $f(x)$ is a probability density function and is assumed




(a)




(b)




(c)

**Fig. 9** Bit error rates (BERs): (a) read operation, (b) write operation, and (c) retention. In the legend, "6T"/"14T" signify the conventional/proposed memory cells. "N"/"P" mean that the additional transistors are nMOSes/pMOSes in the proposed memory cell. Note that the performance of 7T is almost same as 6T.

to be a normal distributed function. Hence, $BER(VDD)$ is a cumulative distribution function. $\mu$ is a voltage below which a BER becomes 0.5 (i.e. random). $\mu$ can be obtained by the Monte Carlo simulation. $\sigma$ is the fitting parameter.

Figure 9(a) illustrates a bit error rate in the read operation. The dependable mode works fine below 0.60 V with a BER of $10^{-8}$ kept even in the worst-case condition (FS corner, 125°C). The minimum operating voltage, which is defined as a voltage at which the BER is $10^{-8}$, and the BER

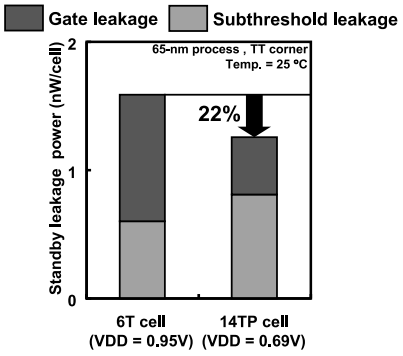



**Fig. 10** Standby leakage power per cell udder typical condition (TT corner, 25°C).

itself are improved by 0.21 V and $1.9 \times 10^{-5}$, compared with the 6T cell (and thus with the 7T normal mode). The dependable mode is the most reliable in the read operation since the $\beta$ ratio can be doubled. The reason why the BER in the 14T high-speed mode is better than the conventional one is that, SNMs in a pair cells is averaged out by connecting the internal nodes.

Figure 9(b) is a BER in the write operation (worst-case condition: FS corner, −40°C). The dependable mode is inappropriate because the conductance of the access transistor is not sufficient. Instead, in the write operation, the high-speed mode should be exploited. In the high-speed mode, the conductance of the access transistors is doubled, and variation is suppressed. Thereby, the write margin becomes larger. The proposed memory cell functions at 0.69 V with a BER of $10^{-8}$ kept. The minimum operating voltage and BER are improved by 0.26 V and $5.5 \times 10^{-4}$, compared with the normal mode.

The retention voltages are lowered by connecting the internal nodes, as illustrated in Fig. 9(c). This is because a retention voltage in a memory cell is averaged out by the additional transistors. Figure 9(c) abbreviates the BERs of retention voltages in the dependable modes, because the same results are obtained in the high-speed mode.

In the proposed dependable SRAM, we can select an appropriate mode, in terms of area overhead, speed or reliability. The proposed SRAM is also suitable to DVFS for low-power operation because it works in a low-VDD region.

### 4.3 Standby Leakage Current

Figure 10 compares the standby leakage powers at the minimum operating voltages [12]. The 14TP cell lowers the leakage power by 22% per cell on the typical conditions. Although the subthreshold leakage is increased in the 14TP cell, the gate leakage is decreased by more than 50%. This indicates that, even if one bit is stored in a memory cell pair, the 14TP cell pair has a less leakage than one 6T cell in the typical condition. As well, the proposed memory cell mitigates the NBTI due to its low-voltage operation.

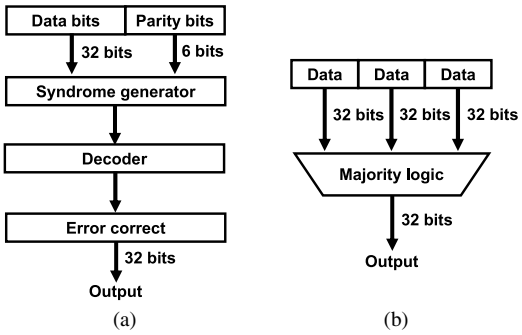



**Fig. 11** Conventional methods to improve BERs: (a) error correction code (ECC) and (b) multi module redundancy (MMR).

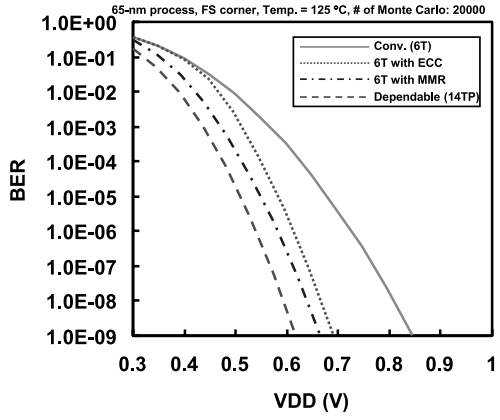



**Fig. 12** Comparison of BERs among the conventional methods and 14TP dependable mode.

### 4.4 Comparison with Other High-Reliability Methods

This subsection discusses the comparison with other high-reliability methods: the error correction code (ECC) in Fig. 11(a) [13]–[15] and the multi-module redundancy (MMR) in Fig. 11(b) [16], [17]. Figure 12 illustrates the comparison of BERs among the conventional methods and proposed dependable mode, in the read operation. The 14TP cell achieves the best BER.

The conventional methods have some drawbacks. The ECC induces more than 100% access time penalty due to an output critical path (syndrome generator, decoder, and error correct) [13], whereas the proposed dependable mode has no speed penalty. Besides, the conventional methods consume extra power, because of the additional bits; The ECC has parity bits, and the MMR has redundant, bits.

Note that, the proposed 7T/14T memory cell can adopt the conventional methods. The combination of the proposed dependable mode and the conventional methods can realize higher dependability.

## 5. Design of 7T/14T Dependable Memory Cell without Half Selection Problem

The proposed SRAM possibly incurs the half-selection problem [18]. Two wordlines in a memory cell pair have to be activated in the write operation because the high-speed mode is the best for the write-in, which might cause unexpected flips in unselected memory cells. Figure 13 portrays the situation. Although only the selected pair needs to be written in, neighbors are half-selected. Unfortunately, the static noise margin in the half-selected pairs is as much as the high-speed mode, which is smaller than the dependable mode.

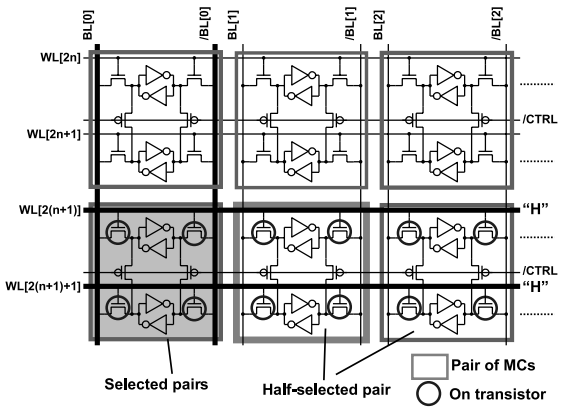


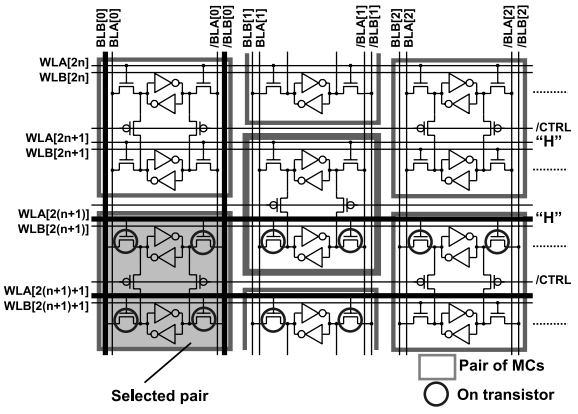

**Fig. 13** Schematic in general memory cell array with half-selection problem.

To solve this problem, we adopt a new array structure in Fig. 14(a). We introduce a wordline pair: WLA and WLB. There is, however, no cell area overhead paid for the wordline pair since WLA and WLB can be laid out with the fourth metal layer (see Fig. 6(c); there is a room for an additional track: both WLA and WLB can be drawn on a memory cell). Figure 14(b) is the wordline mapping. When the hatched pair is selected, WLA[2($n$ + 1)] and WLA[2($n$ + 1)+1] have to be asserted. This memory cell array structure solves the half-select problem up to eight column blocks.

In the logical structure of the schematics in Figs. 14(a) and (b), we shift a memory cell pair in every other column blocks, and the pattern is like a checkerboard. However, we can align the memory cell pairs in the real layout as well as the general memory cell array, as illustrated in Fig. 14(c). For this layout design, one extra wordline pair is required at the end: WLA[2($n$ + 2)] and WLB[2($n$ + 2)].

The decoder structure for the proposed memory cell array is shown in Fig. 15 (a), as a block diagram. In the high-speed and dependable modes, X[0] is fixed to "H." In other words, the X address (row address) always becomes an odd number in these modes. The HSM (high-speed mode) signal is asserted, that is, HSM = "H" only in the high-speed mode. HSM becomes "L" in the normal and dependable modes.

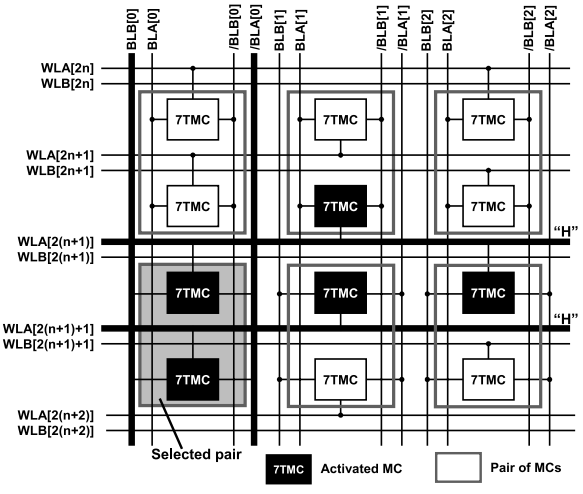
By using HSM, X[0], and X[6:1], the row decoder activates one or two row(s): one row for the normal and dependable modes, and two rows for the high-speed mode. Then, with the outputs from the row decoder (ROW[127:0]) and column addresses (Y[2:0]), the WL selector illustrated in Fig. 15(b) enables one or two WL(s) in accordance with the




(a)

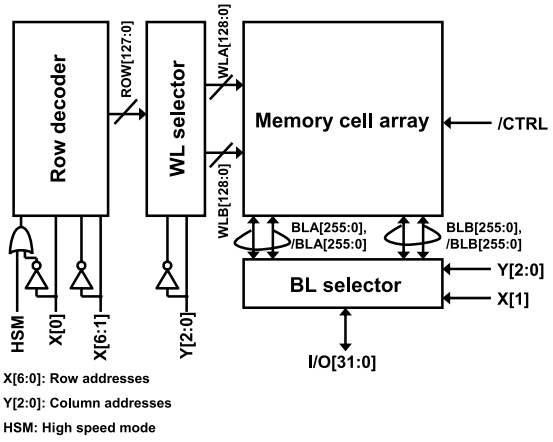
| | BL[0] | BL[1] | BL[2] | BL[3] | BL[4] | BL[5] | BL[6] | BL[7] |
|---|---|---|---|---|---|---|---|---|
| WL[2n] | WLA | WLA | WLA | WLA | WLB | WLB | WLB | WLB |
| WL[2n+1] | WLA | WLA | WLB | WLB | WLA | WLA | WLB | WLB |
| WL[2(n+1)] | WLA | WLA | WLA | WLA | WLB | WLB | WLB | WLB |
| WL[2(n+1)+1] | WLA | WLA | WLB | WLB | WLA | WLA | WLB | WLB |

(b)

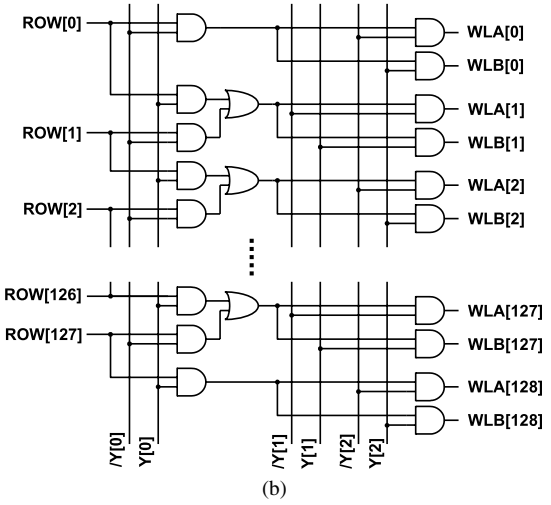



(c)

**Fig. 14** Proposed memory cell array without half-selection problem: (a) schematic, (b) wordline mapping, and (c) layout.




(a)




(b)

**Fig. 15** Decoder structure of the proposed memory cell array: (a) block diagram and (b) schematic of WL selector.

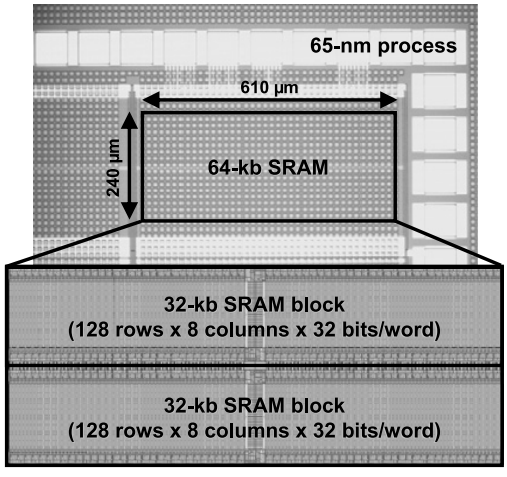



**Fig. 16** Chip micrograph and layout.

output(s) from the row decoder: one WL for the normal and dependable modes, and two WLs for high-speed mode. A BL pair are chosen by X[1] and the Y address (column address).

## 6. Measurement Results

Figure 16 is a micrograph of a dependable 64-kb SRAM test chip with the proposed memory cells whose additional transistors are pMOSes. The test chip was designed and fabricated in a 65-nm CMOS process technology.

Figure 17 shows the measured BERs of the 7TP and 14TP cells. The minimum operating voltage of the 14TP cell is improved by 0.12 V at the first-fail voltage, compared with the 7TP cell. The minimum operating voltage is much lower than the simulation in Fig. 9, and thus does not match with the simulation. This is because the process corner of the test chip is not FS or SF, and the ambient is room tem-

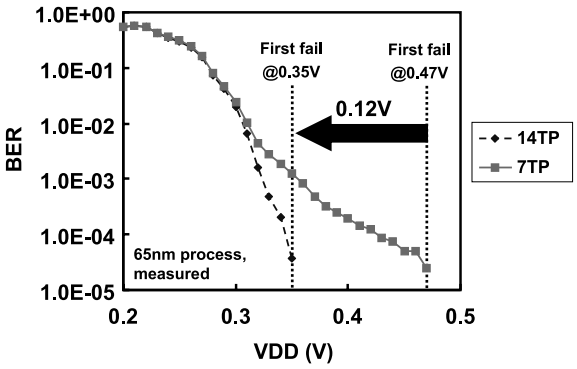



**Fig. 17** Measured BERs of 7TP and 14TP cells at room temperature.

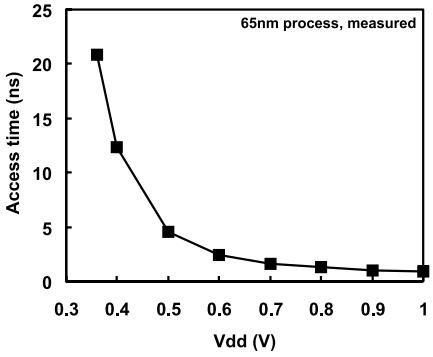



**Fig. 18** Measured access time in dependable mode.

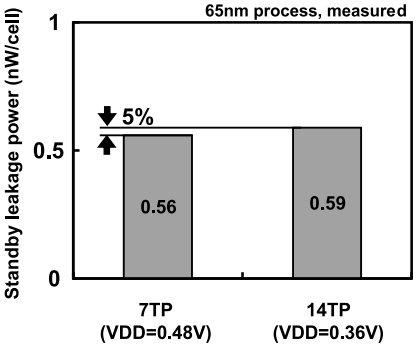



**Fig. 19** Measured leakage powers per cell.

perature.

The measured access time in the dependable mode is shown in Fig. 18. As a cycle time, the designed SRAM achieves 40 MHz operation at a supply voltage of 0.36 V in the dependable mode.

The measured leakage powers at the minimum operating voltage are depicted in Fig. 19. Although the leakage power in the 14TP cell is smaller than the 7TP in the simulation (see Fig. 10), the measure leakage power in the 14TP cell becomes adversely larger by 5%. It is supposed that the gate leakage becomes negligibly small in the measurement because the supply voltage is much smaller than the simulation.

As well as the leakage power, the operating powers on

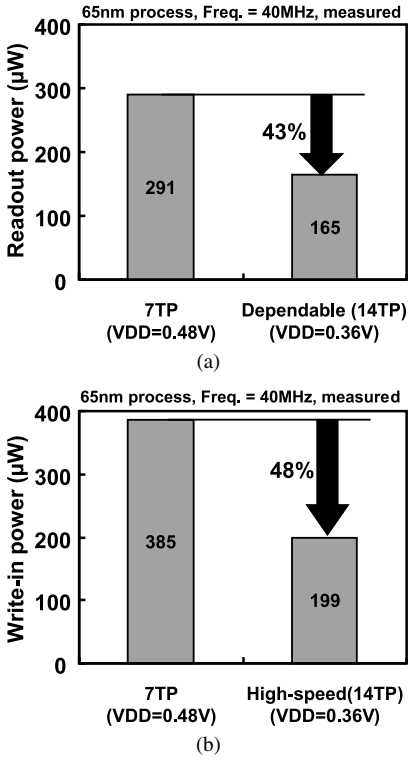



**Fig. 20** Test chip operating powers at 40 MHz: (a) readout power and (b) write-in power.

the test chip were measured. Figures 20(a) and (b) illustrate the readout and write-in powers, respectively, at the operating frequency of 40 MHz. Note that they include power in peripheral circuits, and the memory capacity of the 14TP cells is a half of the 7TP cells. The respective readout and write-in powers are lowered by 43% and 48%.

## 7. Conclusion

We designed a dependable SRAM with 7T/14T memory cells, which have three modes (normal mode, high-speed mode, and dependable mode) in a 65-nm process technology. The proposed SRAM can dynamically change its speed and dependability, based on the concept of "quality of a bit (QoB)." The area overheads are 26% and 11% in the cases where additional transistors are nMOSes and pMOSes, respectively. By running Monte Carlo simulation, we confirmed that the minimum voltages in read and write operations are improved by 0.21V and 0.26V, respectively, with a bit error rate of $10^{-8}$ kept without speed and power overheads. We showed that our dependable SRAM is superior to the error correction code (ECC) and the multi module redundancy (MMR). In addition, we proposed the new memory cell array structure to avoid the half-selection problem. The 64-kb SRAM test chip fabricated in a 65-nm process technology demonstrated that the 14T cell achieves a better BER than the 7T cell. The proposed SRAM will open up new memory allocation in an LSI system. Users can change its performance, depending on reliability, speed, supply voltage

(in particular, for dynamic voltage and frequency scaling: DVFS), standby power, and/or application.

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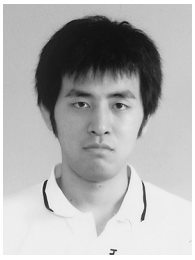
### References

[1] International Technology Roadmap for Semiconductors 2007. http://www.itrs.net/Links/2007ITRS/Home2007.htm
[2] H. Pilo, J. Barwin, G. Braceras, C. Browning, S. Burns, J. Gabric, S. Lamphier, M. Miller, A. Roberts, and F. Towler, "An SRAM design in 65 nm and 45 nm technology nodes featuring read and write-assist circuits to expand operating voltage," 2006 Symposium on VLSI Circuits Digest of Technical Papers, pp.15–16, June 2006.
[3] N. Verma and A.P. Chandrakasan, "A 65 nm 8T sub-vt SRAM employing sense-amplifier redundancy," ISSCC 2007 Digest of Technical Paper, pp.328–329, Feb. 2007.
[4] T.H. Kim, J. Liu, J. Keane, and C.H. Kim, "A high-density subthreshold SRAM with data-independent bitline leakage and virtural ground replica scheme," ISSCC 2007 Digest of Technical Papers, pp.330–331, Feb. 2007.
[5] I.J. Chang, J.J. Kim, S.P. Park, and K. Roy, "A 32 kb 10T subthreshold SRAM array with bit-interleaving and differential read scheme in 90 nm CMOS," ISSCC 2008 Digest of Technical Papers, pp.398–300, Feb. 2008.
[6] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara, "90-nm process-variation adaptive embedded SRAM modules with power-line-floating write technique," IEEE J. Solid-State Circuits, vol.41, no.3, pp.705–711, March 2006.
[7] Y. Morita, H. Fujiwara, H. Noguchi, K. Kawakami, J. Miyakoshi, S. Mikami, K. Nii, H. Kawaguchi, and M. Yoshimoto, "A Vth-variation-tolerant SRAM with 0.3-V minimum operation voltage for memory-rich SoC under DVS environment," 2006 Symposium on VLSI Circuits Digest of Technical Papers, pp.16–17, June 2006.
[8] K. Kawakami, J. Takemura, M. Kuroda, H. Kawaguhi, and M. Yoshimoto, "A 50% power reduction in H.264/AVC HDTV video decoder LSI by dynamic voltage scaling in elastic pipeline," IEICE Trans. Fundamentals, vol.E89-A, no.12, pp.3642–3651, Dec. 2006.
[9] H. Fujiwara, S. Okumura, Y. Iguchi, H. Noguchi, Y. Morita, H. Kawaguchi, and M. Yoshimoto, "Quality of a Bit (QoB): A new concept in dependable SRAM," 9th Int. Symposium on Quality Electronic Design (ISQED 2008) Digest of Technical Papers, pp.98–102, March 2008.
[10] E. Seevinck, F.J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid-State Circuits, vol.22, no.5, pp.748–754, Oct. 1987.
[11] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Statically aware SRAM memory array design," 7th Int. Symposium on Quality Electronic Design (ISQED 2006), pp.25–30, March 2006.
[12] K. Nii, Y. Tsukamoto, T. Yoshizawa, S. Imaoka, Y. Yamagami, T. Suzuki, A. Shibayama, H. Makino, and S. Iwade, "A 90-nm low-power 32-kB embedded SRAM with gate leakage suppression circit for mobile applications," IEEE J. Solid-State Circuits, vol.39, no.4, pp.684–693, April 2004.
[13] T. Suzuki, Y. Yamagami, I. Hatanaka, A. Shibayama, H. Akamatsu, and H. Yamauchi, "A Sub-0.5-V operating embedded SRAM featuring a multi-bit-error-immune hidden-ECC scheme," IEEE J. Solid-State Circuits, vol.41. no.1, pp.152–160, Jan. 2006.
[14] K. Osada, Y. Saitoh, E. Ibe, and K. Ishibashi, "16.7 fA/cell tunnel-leakage-suppressed 16 Mb SRAM for handling cosmic-ray-induced multi-errors," IEEE J. Solid-State Circuits, vol.38, no.11, pp.1952–1957, Nov. 2003.
[15] J. Maiz, S. Hareland, K. Zhang, and P. Armstrong, "Charactrization of multi-bit soft error events in advanced SRAMs," IEDM 2003 Digest of Technical Papers, pp.519–522, Dec. 2003.
[16] J.F. Wakerly, "Microcomputer reliability improvement using triple-modular redundancy," Proc. IEEE, vol.64, no.6, pp.889–895, June 1976.
[17] C.-H. Chen, and A.K. Somani, "Fault-containment in cache memories for TMR redundant processor systems," IEEE Trans. Comput., vol.48, no.4, pp.386–397, April 1999.
[18] H. Yamauchi, T. Suzuki, and Y. Yamagami, "A 1R/1W SRAM cell design to keep cell current and area saving against simultaneous read/write disturbed accesses," IEICE Trans. Electron., vol.E90-C, no.4, pp.749–757, April 2007.



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