

Simple Waveform Model of Inductive Interconnects by Delayed Quadratic Transfer Function with Application to Scaling Trend of Inductive Effects in VLSI's

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SUMMARY A simple analytical model based on Delayed Quadratic (DQ) Transfer Function approximation is proposed for estimating waveforms of inductive single-line interconnects in VLSI's. An expression for overshoot voltage is derived by the model within 17% error for the line width less than 10 times the minimum line width and typical input signal. A delay expression is also proposed within 15% for the same condition. The strength of the inductive effect is shown to be expressed by a closed-form expression, $A = 2(L(C_T + 0.5C))^{1/2} / (R_T(C_T + C_J) + R_T C + RC_T + 0.4RC)$. By using the criteria, a scaling trend of inductive effects in VLSI's is discussed. It is shown that the inductive effect of single-line, minimum-width VLSI interconnect peaks off at 90 nm based on the ITRS predicted parameters.

key words: on-chip interconnects, inductive effect, inductive index, overshoot, propagation delay

1. Introduction

Signal integrity has become a more serious issue as VLSI's scaling of technology continues into deep sub-micron region. While scaling of transistors results in faster yet low-power circuits, shrinking the physical size of interconnect may restrict VLSI's performance. While the electrical property of interconnect consists of resistance, inductance and capacitance. In the older technologies, however, interconnect was well modeled only with resistance and capacitance (RC model) [1]. Recently, neglected interconnect inductance was said to become the cause of various signal integrity issues such as overshoot and propagation delay error, and therefore inductance was also need to be considered for modeling of interconnect [2], [3].

Table 1 summarizes several previous works concerning interconnect modeling as well as the aim of this work. Where L , C_J , and C_T are inductance, junction capacitance, and load capacitance, respectively. In the previous works, inductance and junction capacitance were neglected in [1]; in [2] junction capacitance was neglected and only delay formula was proposed; and the output response was expressed

Table 1 Comparison to the previous interconnect modeling works.

Ref.	Waveform	Delay	L	C_J	C_T	Type
[1]	O	O	X	X	O	Closed-form
[2]	X	O	O	X	O	Closed-form
[3]	O	X	O	O	X	Complicated
Aim	+ Overshoot	O	O	O	O	Closed-form

not in closed-form function in [3]. Those previous works also did not consider the effect of the slope of input signal. Comparing the expressions and all derivations proposed in [1]–[3], it is also clear that considering inductance for interconnect modeling would lead to complicated or difficult calculation. Thus it is practical if there is a rule-of-thumb whether inductance can be neglected or otherwise need to be considered for any case.

In this paper, a simple analytical model based on Delayed Quadratic (DQ) Transfer Function is proposed for estimating waveforms of inductive single-line interconnects in VLSI's. Based on the proposed approximation function, closed-form expressions for calculating the strength of inductive effect, overshoots, and propagation delay are derived. Scaling trend of inductive effects in VLSI's is also discussed.

2. Modeling of Single Inductive Interconnect

2.1 Delayed Quadratic Transfer Function

Figure 1 shows the typical model of single line on-chip interconnect. Driver inverter can be expressed by using equivalent resistance R_T and junction capacitance C_J . While load inverter can be expressed by load capacitance C_T . Parameters R , L , C and d are showing total interconnect resistance, inductance, capacitance, and length, respectively. While interconnect conductance G can be neglected [2]. Note that interconnect is shown with transmission line element (distributed model) based on telegrapher equations.

As aforementioned, previously VLSI's interconnect is well modeled by using RC model. The output response of non-inductive (RC) interconnect model was proposed in [1]. By considering additional junction capacitance as pointed out in [3], when step function is provided for input signal ($V_{IN} = V_{DD}/s$), thus the transfer function of the output response can be rewritten as (1). Note that $0.1RC$ in the nu-

Manuscript received March 13, 2006.

Manuscript revised June 13, 2006.

Final manuscript received August 2, 2006.

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DOI: 10.1093/ietfec/e89-a.12.3569

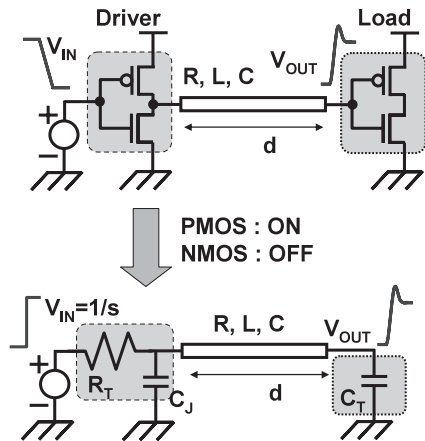


Fig. 1 Single line interconnects.

merator is pure delay factor as proposed in [1].

When inductive effect could be neglected the output response can be modeled by using RC model as (1), while output response with overshoot can be generated only with quadratic or higher degree transfer function. Thus, naturally it is simple if the transfer function of output response of single line inductive interconnect is expressed by using Delayed Quadratic (DQ) Transfer Function as shown in (2).

$$\frac{V_{OUT,RC}(s)}{V_{DD}} = \frac{1}{s} \times \exp(-0.1RCs) / \{ (R_T(C_T + C_J) + R_T C + RC_T + (2/\pi)^2 RC) s + 1 \} \quad (1)$$

Although the candidate for coefficient of s^2 in (2) may vary, the simplest way for determining the coefficient is by considering only the interconnect inductance L as well as capacitances C and C_T . While the effect of junction capacitance C_J may be neglected here. The effect of each capacitance is assumed to be independent to each other and the strength of each effect is expressed by constants α and β as in (2).

$$\frac{V_{OUT}(s)}{V_{DD}} = \frac{1}{s} \times \exp(-0.1RCs) / \{ L(\alpha C_T + \beta C) s^2 + (R_T(C_T + C_J) + R_T C + RC_T + (2/\pi)^2 RC) s + 1 \} \quad (2)$$

Constants α and β are then determined by using moment matching method between (2) and the exact transfer function of output response of inductive interconnect shown in (3) as follows.

$$\frac{V_{OUT,EXACT}(s)}{V_{DD}} = \frac{1}{s} \times \left\{ (1 + sR_T(C_T + C_J)) \times \cosh \sqrt{s^2 LC + sRC} + \sqrt{\frac{sC}{R + sL}} \times \left(R_T + sC_T \frac{R + sL}{sC} (1 + sR_T C_J) \right) \sinh \sqrt{s^2 LC + sRC} \right\}^{-1} \quad (3)$$

First, to simplify the problem by using transformation of variables, both (2) and (3) are normalized with $\sigma = sRC$.

Therefore (2) and (3) become (4) and (5) and normalized parameters are shown in (6). Note that although strictly $V'_{DD} = V_{DD}RC$, however, since the level of scaled power supply V'_{DD} needs to be the same as the original power supply V_{DD} . Thus scaling on voltage domain is not necessary, and hereafter $V'_{DD} = V_{DD}$.

$$\frac{V_{OUT}(\sigma)}{V'_{DD}} = \frac{1}{\sigma} \times \exp(-0.1\sigma) / \{ l_T(\alpha c_T + \beta) \sigma^2 + (r_T(c_T + c_J) + r_T + c_T + (2/\pi)^2) \sigma + 1 \} \quad (4)$$

$$\frac{V_{OUT,EXACT}(\sigma)}{V'_{DD}} = \frac{1}{\sigma} \left\{ (1 + \sigma r_T(c_T + c_J)) \cosh \sqrt{\sigma(1 + \sigma l_T)} + \sqrt{\sigma/(1 + \sigma l_T)} (r_T + c_T(1 + \sigma l_T)(1 + \sigma r_T c_J)) \times \sinh \sqrt{\sigma(1 + \sigma l_T)} \right\}^{-1} \quad (5)$$

$$\{ r_T = R_T/R, c_J = C_J/C, c_T = C_T/C, \sigma = sRC, V'_{DD} = V_{DD}RC \} \quad (6)$$

Next, assuming that constant $(2/\pi)^2$ in (4) and pure delay factor 0.1 are not known yet and expressed with variable a and b , respectively. Considering asymptotical condition of $r_T = c_T = 0$, which means very big driver and smallest load inverters are used. Thus (4) and (5) become (7) and (8). Using moment matching between (7) and (8), constants β , a and b are obtained as (9). Note that a and b in (9) are similar with those in [1].

To obtain α , the second asymptotical condition of $r_T = 0$ with substituting the results of (9) into (4) is applied. Therefore (4) and (5) become (10) and (11) approximately. Matching the moments of (10) and (11), α can be approximated to be 1. This result is in the agreement with second method for calculating α .

$$\frac{V_{OUT}(\sigma)}{V_{DD}} = \frac{1}{\sigma} \frac{\exp(-b\sigma)}{\beta l_T \sigma^2 + a\sigma + 1} \quad (7)$$

$$\frac{V_{OUT,EXACT}(\sigma)}{V_{DD}} = \frac{1}{\sigma \cosh \sqrt{\sigma(1 + \sigma l_T)}} \quad (8)$$

$$\{ a = 1/\sqrt{6} \approx 0.4, b = (3 - \sqrt{6})/6 \approx 0.1, \beta = 0.5 \} \quad (9)$$

$$\frac{V_{OUT}(\sigma)}{V_{DD}} \approx \frac{1}{\sigma} \left(1 - \left(c_T + \frac{1}{2} \right) \sigma - \left(\alpha l_T c_T + \frac{l_T}{2} - c_T^2 - \left(\frac{3 + \sqrt{6}}{6} \right) c_T - \frac{5}{24} \right) \sigma^2 \right) \quad (10)$$

$$\frac{V_{OUT,EXACT}(\sigma)}{V_{DD}} \approx \frac{1}{\sigma} \left(1 - \left(c_T + \frac{1}{2} \right) \sigma - \left(l_T c_T + \frac{l_T}{2} - c_T^2 - \frac{5}{6} c_T - \frac{5}{24} \right) \sigma^2 \right) \quad (11)$$

As aforementioned, since C and C_T are assumed to be independent to each other, therefore C is neglected here ($C = 0$). Then, lumped model of interconnect is used for replacing the distributed model. For asymptotical condition of $R_T = 0$, the transfer function of output response becomes as simple as (12). Comparing (12) with (2) for the same condition, which is $R_T = 0$ and $C = 0$, then $\alpha = 1$ is obtained.

Finally, a simple analytical model based on Delayed Quadratic (DQ) Transfer Function as shown in (13) is proposed for estimating waveforms of inductive single-line interconnects in VLSI's.

$$\frac{V_{OUT}(s)}{V_{DD}} = \frac{1}{s} \frac{1}{LC_T s^2 + RC_T s + 1} \quad (12)$$

$$\frac{V_{OUT}(s)}{V_{DD}} = \frac{1}{s} \times \exp(-0.1RCs) / \{L(C_T + 0.5C)s^2 + (R_T(C_T + C_J) + R_T C + RC_T + 0.4RC)s + 1\} \quad (13)$$

If (13) is rewritten as (14), and Laplace function (14) is transferred to time domain function (15), then it is clear that proposed approximation function is closed-form. Where residues k_1 and k_2 , and poles p_1 and p_2 are given in (16), respectively. Note that $(LC)^{1/2}$ is time-of-flight parameter of transmission line.

$$\frac{V_{OUT}(s)}{V_{DD}} = \frac{1 \exp(-0.1RCs)}{s a_2 s^2 + a_1 s + 1} \quad (14)$$

$$\frac{v_{OUT}(t)}{V_{DD}} = 1 + k_1 \exp(-p_1(t-0.1RC)) + k_2 \exp(-p_2(t-0.1RC)) \quad (\text{if } t > \text{MAX}(0.1RC, \sqrt{LC}))$$

$$= 0 \quad (\text{if } t \leq \text{MAX}(0.1RC, \sqrt{LC})) \quad (15)$$

$$\left\{ \begin{array}{l} k_1 = \frac{a_1 - \sqrt{a_1^2 - 4a_2}}{2\sqrt{a_1^2 - 4a_2}}, \quad k_2 = -\frac{a_1 + \sqrt{a_1^2 - 4a_2}}{2\sqrt{a_1^2 - 4a_2}} \\ p_1 = \frac{a_1 + \sqrt{a_1^2 - 4a_2}}{2a_2}, \quad p_2 = \frac{a_1 - \sqrt{a_1^2 - 4a_2}}{2a_2} \end{array} \right. \quad (16)$$

2.2 Inductive Index, Overshoot, and Delay

Employing transformation of variable of (14) as (17), then (14) becomes (18). The waveform of output response of inductive interconnect is determined by only one parameter A as in (19), with additional normalized pure delay factor λ as in (20). As aforementioned, although strictly power supply V_{DD} is also scaled to V'_{DD} as in (21). To satisfy the same voltage level of initial power supply V_{DD} , however, power supply is kept constant as $V'_{DD} = V_{DD}$. Hereafter V'_{DD} is written as V_{DD} .

$$(R_T(C_T + C_J) + R_T C + RC_T + 0.4RC)s = 2\sigma \quad (17)$$

$$\frac{V_{OUT}(\sigma)}{V'_{DD}} = \frac{1 \exp(-0.1\lambda s)}{\sigma A^2 \sigma^2 + 2\sigma + 1} \quad (18)$$

$$A = \frac{2\sqrt{L(C_T + 0.5C)}}{(R_T(C_T + C_J) + R_T C + RC_T + 0.4RC)} \quad (19)$$

$$\lambda = \frac{2RC}{R_T(C_T + C_J) + R_T C + RC_T + 0.4RC} \quad (20)$$

$$V'_{DD} = V_{DD} \left(\frac{2}{R_T(C_T + C_J) + R_T C + RC_T + 0.4RC} \right) \quad (21)$$

Parameter A is to be called inductive index and proposed for showing the strength of inductive effect on single line interconnects. Note that inductive index A is dimensionless and has physical meaning as the ratio of time constant of inductance-capacitance (lossless inductive) interconnect to time constant of resistance-capacitance (lossy non-inductive) interconnect. When A is less than 1, interconnect is less inductive or behave as resistance-capacitance interconnects. Otherwise, inductive effect may need to be considered for designing interconnect.

Moreover, transferring (18) to time domain function, then the output response can be expressed as (22). Where τ is normalized time parameter as shown in (23).

$$\frac{v_{OUT}(\tau)}{V_{DD}} = 1 + \frac{1 - \sqrt{1 - A^2}}{2\sqrt{1 - A^2}} \exp\left(-\frac{1 + \sqrt{1 - A^2}}{A^2}(\tau - 0.1\lambda)\right) - \frac{1 + \sqrt{1 - A^2}}{2\sqrt{1 - A^2}} \exp\left(-\frac{1 - \sqrt{1 - A^2}}{A^2}(\tau - 0.1\lambda)\right) \quad (\text{if } \text{MAX}(0.1\lambda, \tau > 2\lambda\sqrt{LC}/(RC)))$$

$$= 0 \quad (\text{if } \text{MAX}(0.1\lambda, \tau > 2\lambda\sqrt{LC}/(RC))) \quad (22)$$

$$\tau = \frac{2t}{(R_T(C_T + C_J) + R_T C + RC_T + 0.4RC)} \quad (23)$$

Overshoot is one of phenomena caused by inductive effect. It is unwanted phenomenon since the voltage of overshoot exceeds V_{DD} and may threaten the reliability of circuits. Figure 2 shows an illustration of overshoot, undershoot, and propagation delay. From (22), it is clear that the waveform oscillates and overshoot occurs when $A > 1$. The peak times of overshoot/undershoot can be obtained by solving Eq. (24). The results are shown in (25). When $n = 1$ it shows the first and highest overshoot peak time, $n = 2$ it shows the first undershoot, and so on. However, the most important attention is only for the first overshoot. Substitute (25) with $n = 1$ to (22), the highest overshoot peak voltage is obtained as shown in (26). Note that overshoot peak vol-

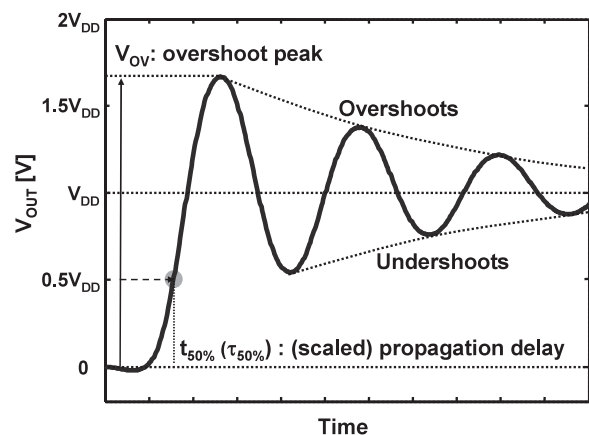


Fig. 2 Overshoot and propagation delay.

tage is not dependent on time domain but power supply V_{DD} and inductive index A .

$$\frac{dv_{OUT}(\tau)}{d\tau} = 0 \quad (24)$$

$$\tau_{OV/UD} = \frac{n\pi A^2}{\sqrt{A^2 - 1}} + 0.1\lambda \quad (25)$$

$$\frac{v_{OV}}{V_{DD}} = 1 + \exp\left(-\frac{\pi}{\sqrt{A^2 - 1}}\right) \quad (\text{if } A \geq 1) \quad (26)$$

Propagation delay is defined as time when $v_{OUT} = 0.5V_{DD}$. Since propagation delay formula cannot be derived from (22) analytically. Thus, approximation function of propagation delay is derived as follows.

First, let neglect pure delay factor then (18) becomes (27). Considering asymptotical condition of $A = 0$, then (18) and (22) become expressions shown in (28). Solving $v_{OUT} = 0.5V_{DD}$ then propagation delay is obtained as in (29).

Next, as A increases, then the propagation delay of (30) approximates that of (18) better. Similarly, after transforming (30) into time domain function (31) and solving $v_{OUT} = 0.5V_{DD}$ then propagation delay is obtained as in (32).

$$\frac{V_{OUT}(\sigma)}{V'_{DD}} = \frac{1}{\sigma} \frac{1}{A^2\sigma^2 + 2\sigma + 1} \quad (27)$$

$$\frac{V_{OUT}(\sigma)}{V_{DD}} = \frac{1}{\sigma} \frac{1}{2\sigma + 1} \Leftrightarrow \frac{v_{OUT}(\tau)}{V_{DD}} = 1 - \exp\left(-\frac{\tau}{2}\right) \quad (28)$$

$$\frac{v_{OUT}(\tau)}{V_{DD}} = 0.5 \Rightarrow \tau_{50\%} = 2 \ln 2 \quad (29)$$

$$\frac{V_{OUT}(\sigma)}{V_{DD}} = \frac{1}{\sigma} \frac{1}{A^2\sigma^2 + 1} \quad (30)$$

$$\frac{v_{OUT}(\tau)}{V_{DD}} = 1 - \cos\left(\frac{\tau}{A}\right) \quad (31)$$

$$\frac{v_{OUT}(\tau)}{V_{DD}} = 0.5 \Rightarrow \tau_{50\%} = \frac{\pi}{3}A \quad (32)$$

Finally, using the results of (29) and (32), propagation delay formula is then fitted to the formula shown in (33). In addition, reconsidering the pure delay formula, approximation function of propagation delay is then proposed as (34). Note that (34) is in normalized time scale. While in the real time scale, by substituting τ in (23) into (33), propagation delay can be expressed as (35).

$$\tau_{50\%} = 2 \ln 2 \sqrt{1 + \frac{\pi}{3(2 \ln 2)^2} A^2} \approx 1.39 \sqrt{1 + 0.55A^2} \approx 1.34 \sqrt{1 + 0.64A^2} \quad (33)$$

$$\tau_{50\%} = 1.34 \sqrt{1 + 0.64A^2} + 0.1\lambda \quad (34)$$

$$t_{50\%} = \tau_{50\%} \times \frac{R_T(C_T + C_J) + R_T C + R C_T + 0.4RC}{2} = 0.1RC + 0.67(2.56L(C_T + 0.5C) + (R_T C_T + R_T C_J + R_T C + R C_T + 0.4RC)^2)^{1/2} \quad (35)$$

Table 2 Parameter range for calculation/simulation.

Parameter	Range
Interconnect length d	1 μ m, 10 μ m, 100 μ m, 1mm, 10mm.
Relative driver size H_{DR}	1,2,5,10,20,50,100,200,500,1000.
Relative load size H_{LD}	1,2,5,10,20,50,100,200,500,1000.
Interconnect width W	$W_0, 2W_0, 5W_0, 10W_0$.
Interconnect height H	Local and global lines.
Input signal slope time T_{IN}	FO1, FO3, FO5, FO7.

2.3 Calculation/Simulation Result

Simulation is carried out using parameters shown in Table 2 in 90 nm-technology with Hspice circuit simulator in transistor/gate level. To be our best knowledge that no previous works [1]–[3] did both of considering the slope time of input signal and comparing their proposed approximation functions directly with simulation using inverters for both of the driver and load. Instead, they used lumped resistor and capacitors for R_T , C_J and C_T in circuit simulation.

Physical data of interconnect as well as the device is referred from ITRS [4]. Interconnect structure is assumed as single plate and calculated as follows [5]. Resistance R is calculated using conventional formula $R = \rho d/W/T$. Where ρ , d , W , and T are interconnect resistivity, length, width, and thickness, respectively. While capacitance and inductance are calculated using formulas proposed in [6] and [7]. In circuit simulation, instead of using n -step π -ladder circuit, transmission line element, which based on telegrapher equations, is used for distributed interconnect.

Both driver and load inverters are designed to have characteristics of $V_{IN} = V_{OUT} = 0.5V_{DD}$ by adjusting the gate width of PMOS to be about 2.5 times as big as the gate width of NMOS. Note that the minimum gate width is 0.2 μ m in 90 nm-technology, while gate length is kept constant to 0.1 μ m, and minimum gate width is 0.2 μ m.

Although ITRS points out various metal layers of interconnects for local and global ones. In this paper, however, for simplifying the problem, local and global lines are assigned for the lowest level of interconnect metal layer and for 10th level of interconnect metal layer, respectively. The work is focused on signal line, where interconnect width is small enough. Therefore, as shown in Table 2, interconnect width is from $W = W_0$ to $W = 10W_0$. Minimum interconnect width is assumed as a half of wiring pitch and varies for local line $W_{0,LOCAL} = 107$ nm and global line $W_{0,GLOBAL} = 210$ nm [4].

Input signal slope time T_{IN} is set to be equal to the slope time of output signal of first inverter in two-inverter-chain-circuit, when step function is inserted to the input of first inverter. Although, typical input signal slope time is about the slope time of fan-out-3 (25 ps) to fan-out-5 (40 ps) signal, fast signal (fan-out-1, 12 ps) and slow signal (fan-out-7, 54 ps) are also calculated. 64 configurations of driver

size and load size are used, where the configuration of driver size and load size is either $H_{DR} \geq H_{LD}$ or $H_{LD} = 2-2.5H_{DR}$. Since inductive effect is predicted to be significant when driver size H_{DR} is bigger enough than load size H_{LD} . Finally, from all parameters shown in Table 2, total more than 10000 cases of interconnects are used for calculation/simulation.

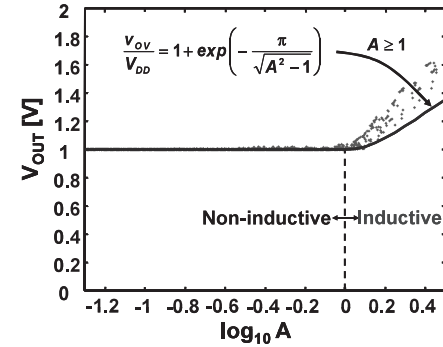
Figure 3 shows the comparison of overshoots peaks by simulation (dots) with calculation (line) using (26) with all parameters mentioned in Table 2 and in respect to various input signal slope times, which are $T_{IN} = 12$ ps (FO1), $T_{IN} = 25$ ps (FO3), $T_{IN} = 40$ ps (FO5), and $T_{IN} = 54$ ps (FO7). It is clear that overshoots occur when $A > 1$ or $\log_{10} A = 0$, and those peaks may increase when faster signal is used. Note that R_T , which has big impact on the overshoot peak, is intentionally calculated as simple as possible by neglecting T_{IN} but the equivalent resistance between pentode and triode regions [8]. For typical and slow input signals, the error of overshoot peak calculation/simulation result is less than 16%, where the error is calculated by (36) and $V_{MAX} \geq V_{DD}$.

Figures 4, 5, 6, and 7 are showing peaks of output responses with only typical input signal slope time $T_{IN} = 25$ ps (FO3) and other parameters shown in Table 2 in respect to driver size H_{DR} (Fig. 4), interconnect length d (Fig. 5), interconnect width W (Fig. 6), and load size H_{LD} (Fig. 7), respectively. No overshoot is confirmed when either small buffer size ($H_{DR} \leq 10$ in Fig. 4), short interconnect ($d \leq 10 \mu\text{m}$ in Fig. 5), or minimal interconnect width ($W = W_0$ in Fig. 6) is used. It is also interesting to note that there is no overshoot confirmed when too long interconnect is used ($d = 10$ mm in Fig. 5). It means that there is an optimal length for such driver-load configuration where inductive index becomes maximal. In the other hand, the effect of H_{LD} is not significant as shown in Fig. 7.

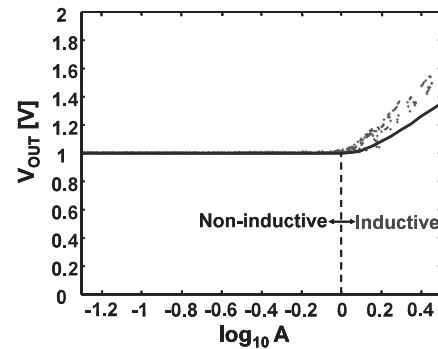
$$Error_{OV} = \left| \frac{V_{MAX,CAL} - V_{MAX,SIM}}{V_{MAX,SIM}} \right| \times 100\% \quad (36)$$

Delay is much more difficult to model. Considering the input signal slope time, the definitions of simulation delay ($delay_{SIM}$) and calculation delay ($delay_{CAL}$) are illustrated in Fig. 8. Simulation delay $delay_{SIM}$ is defined as propagation time needed from $V_{IN} = 0.5V_{DD}$ to $V_{OUT} = 0.5V_{DD}$, while calculation delay $delay_{CAL}$ is calculated by (37). Where T_0 is starting time calculated from the time input signal crosses $0.5V_{DD}$ and expressed as (38) [8], while T_{CAL} is calculated using proposed expression (35). Note that the coefficient T_{IN} in (38) is about 0.21 with $V_{DD} = 1$ V and $V_{TH,PMOS} = -0.35$ V. In addition, parameter dt is used for expressing time due to feed forward effect of input voltage. When input signal makes a high-to-low transition, the voltage of output of driver inverter is temporarily driven down below GND before PMOS pulls the output up [9].

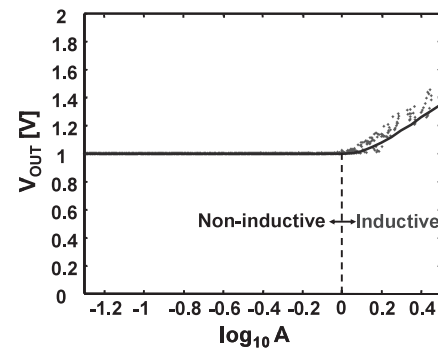
In the real case, by considering that the input signal as an output signal from other circuit, it means that input signal itself may include delay error besides the delay error between calculation/simulation delay defined above. Therefore the delay error can be defined as (39). Figure 9 shows



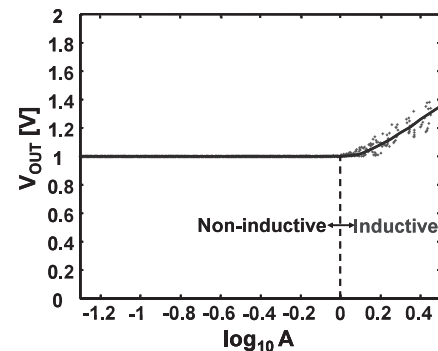
(a) $T_{IN} = 12$ ps (FO1), Error < 21%.



(b) $T_{IN} = 25$ ps (FO3), Error < 17%.

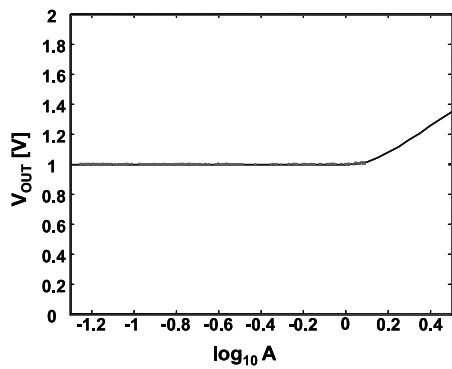


(c) $T_{IN} = 40$ ps (FO5), Error < 11%.

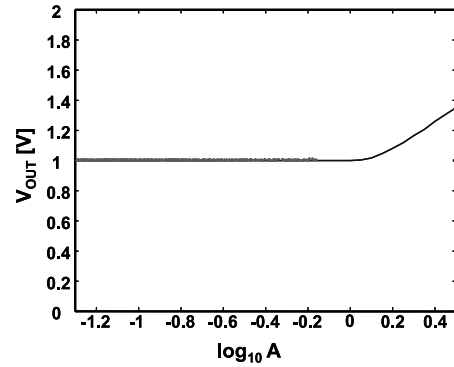


(d) $T_{IN} = 54$ ps (FO7), Error < 9%.

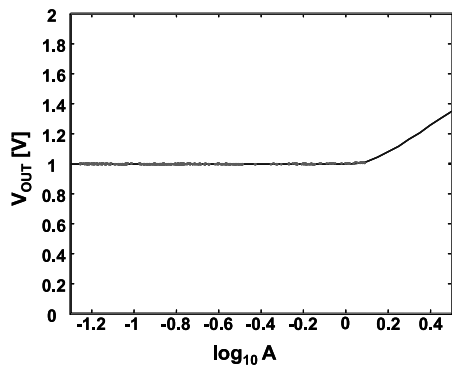
Fig. 3 Overshoots calculation/simulation results in respect to T_{IN} .



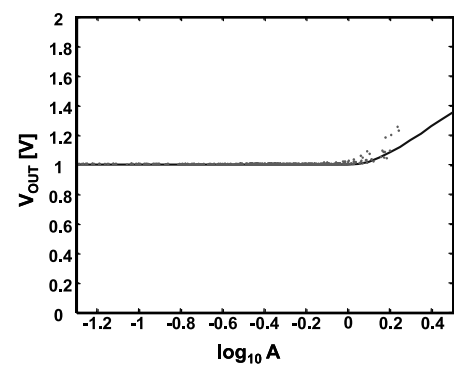
(a) $H_{DR} = 1$, Error < 1%



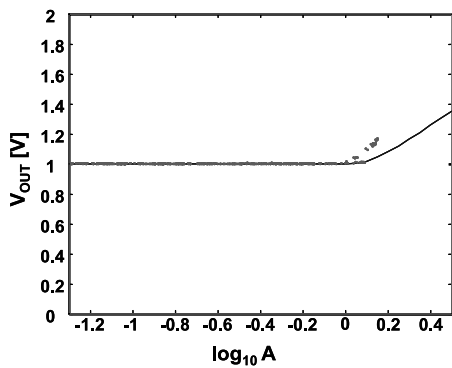
(a) $d = 10 \mu\text{m}$, Error < 1%.



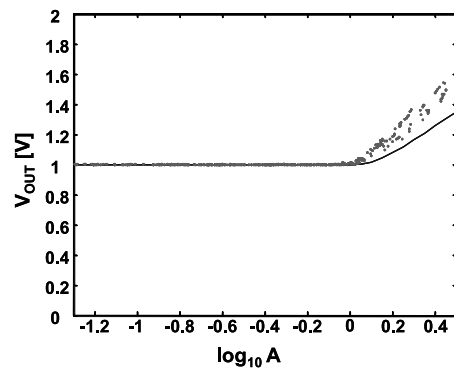
(b) $H_{DR} = 10$, Error < 1%



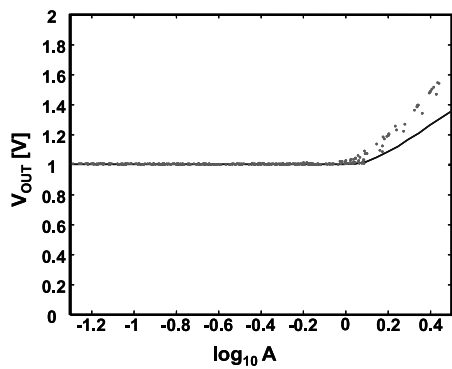
(b) $d = 100 \mu\text{m}$, Error < 12%.



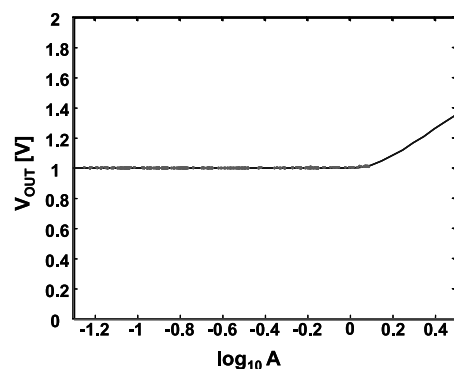
(c) $H_{DR} = 100$, Error < 11%



(c) $d = 1 \text{ mm}$, Error < 17%.



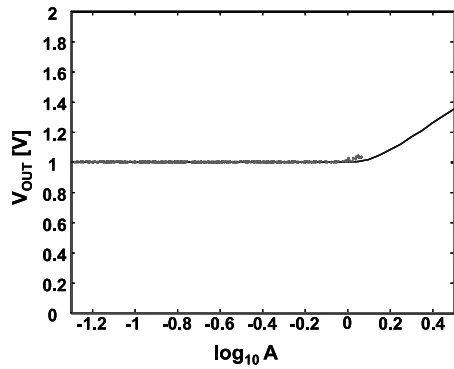
(d) $H_{DR} = 1000$, Error < 17%



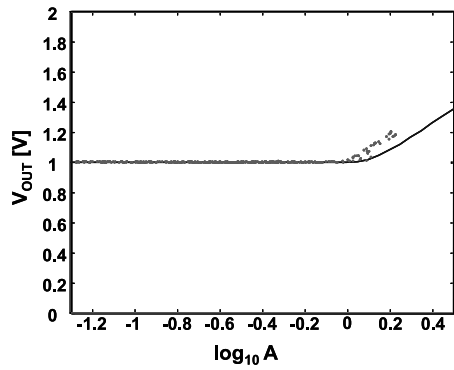
(d) $d = 10 \text{ mm}$, Error < 1%.

Fig. 4 Overshoots calculation/simulation results in respect to H_{DR} .

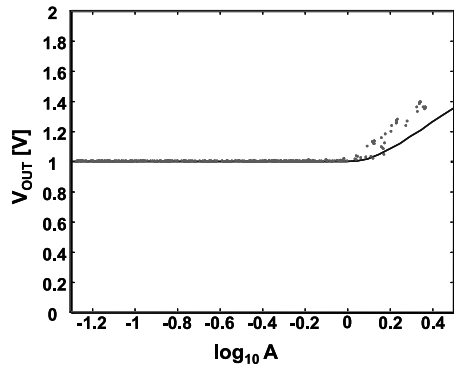
Fig. 5 Overshoots calculation/simulation results in respect to d .



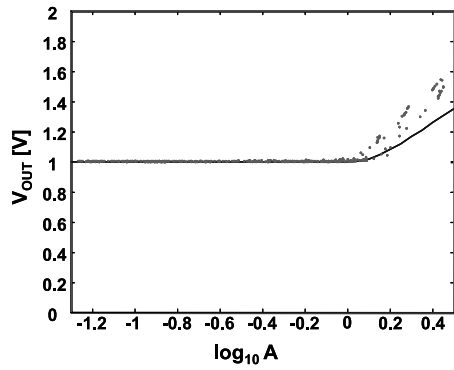
(a) $W/W_0 = 1$, Error < 4%.



(b) $W/W_0 = 2$, Error < 10%.

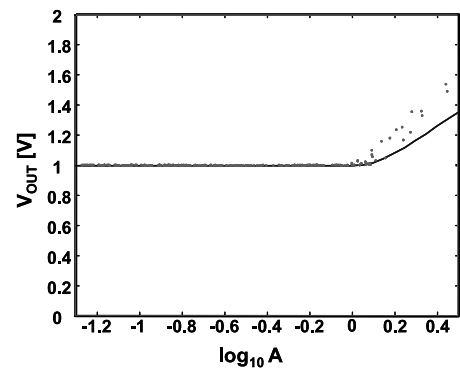


(c) $W/W_0 = 5$, Error < 14%.

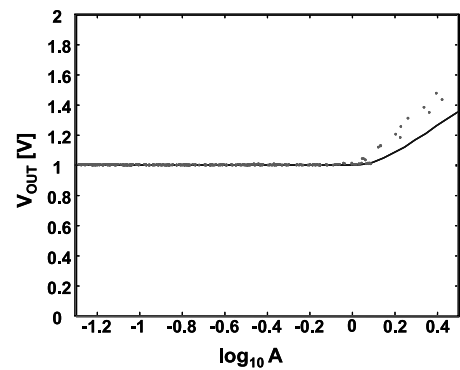


(d) $W/W_0 = 10$, Error < 17%.

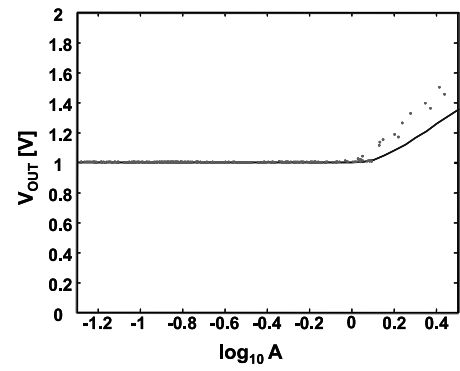
Fig. 6 Overshoots calculation/simulation results in respect to W .



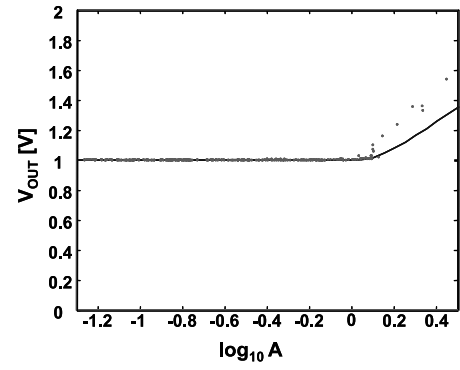
(a) $H_{LD} = 1$, Error < 15%.



(b) $H_{LD} = 10$, Error < 16%.



(c) $H_{LD} = 100$, Error < 16%.



(d) $H_{LD} = 1000$, Error < 17%.

Fig. 7 Overshoot calculation/simulation result in respect to H_{LD} .

can be rewritten as (42). Since gate time constant τ_G is not dependent on driver size H_{DR} as shown in (41).

As aforementioned, inductive effect increases as bigger driver is used. Therefore, if using big driver then the effect R_T is less significant and can be neglected. Therefore, (42) becomes (43). The next step is finding the optimal value of A_2^2 in respect to C_T as shown in (44). Substitute optimal junction capacitance $C_{T,OPT}$ to (43), then (43) becomes as simple as (45). From (40)–(45), it can be concluded as (46), that maximal quadrate of inductive index A_{MAX}^2 is proportional to $L/R/\tau_G$. Note that A_{MAX}^2 is dimension-less and has similar form to the well-known inductive quality factor parameter shown in (47).

$$A_0^2 = \frac{4L(C_T + 0.5C)}{(R_T C_J + R_T(C_T + C) + RC_T + 0.5RC)^2} \quad (40)$$

$$\tau_G = R_T C_J = \left(\frac{R_{T0}}{H_{DR}} \right) (C_{J0} H_{DR}) = R_{T0} C_{J0} = \tau_G \quad (41)$$

$$A_1^2 = \frac{4L(C_T + 0.5C)}{(\tau_G + R_T(C_T + C) + RC_T + 0.5RC)^2} \quad (42)$$

$$A_2^2 = \frac{4L(C_T + 0.5C)}{(\tau_G + RC_T + 0.5RC)^2} \quad (43)$$

$$\frac{\partial A_2^2}{\partial C_T} = 0 \Rightarrow C_{T,OPT} = \tau_G - 0.5C \quad (44)$$

$$A_3^2 = \frac{L}{R\tau_G} \quad (45)$$

$$A_0^2 \leq A_1^2 \leq A_2^2 \leq A_3^2 \propto A_{MAX}^2 \quad (46)$$

$$Q = \frac{\omega L}{R} \quad (47)$$

Figure 10 shows the trends of interconnect driver time constant τ_G , resistance and inductance per unit length when for $W = W_0$ from the old 1.2 μm -technology to the future 22 nm-technology. Where W_0 is minimum width of interconnect. Driver time constant τ_G has been decreased gradually as scaling of technology continued. This trend should be similar in the future. In other hand, resistance was increasing as scaling rate $\sim s$ from 1.2 μm -technology to 130 nm-technology. Since in the old technologies, cross section of interconnect is scaled linearly.

The utilizing of copper metal helps decreasing interconnect resistance starting from 90 nm-technology. In deep sub-micron region, cross section of interconnect is scaled with scaling rate $\sim s^2$. While, inductance was increasing due to the increasing number of interconnect layer in previous technologies. Therefore, top metal layer became higher. Recently and in deep-sub-micron region, however, the height of top metal layer decreases although the interconnect layer number is still increasing. Note that when calculating inductance, the worst case, which is there is not any other interconnect in its surrounding, is assumed.

Finally, as shown in Fig. 11, the peak of inductive effect is achieved on 90 nm-technology for $W = W_0$. Note that the oldest 1.2 μm -technology data was obtained from the chip data, while ITRS 1999 was referred for 130 nm- and 180 nm-data [10]. The data on technologies between

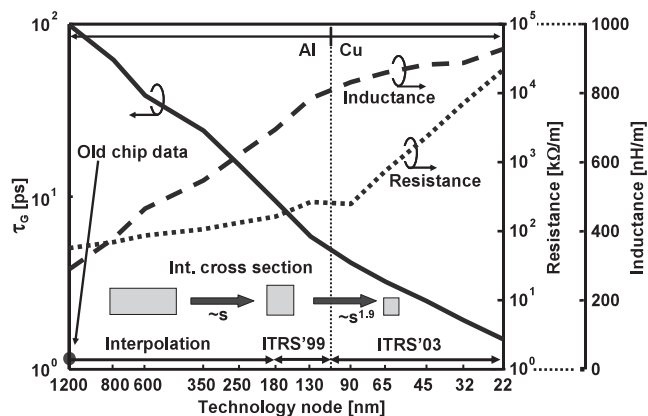


Fig. 10 Trends of resistance, inductance, and driver time constant τ_G .

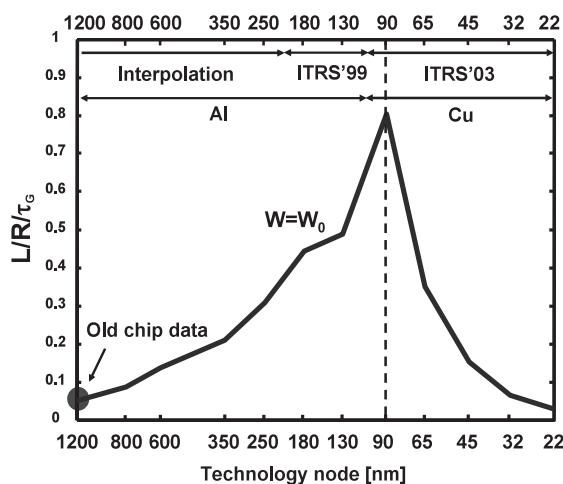


Fig. 11 Trend of inductive interconnects.

1.2 μm and 180 nm were calculated by interpolation. For deep sub-micron region, the data is calculated from ITRS 2003 [4].

4. Conclusion

A simple analytical model based on Delayed Quadratic Transfer Function approximation is proposed for estimating waveforms of inductive single-line interconnects in VLSI's. When $L \rightarrow 0$, proposed transfer function is in the agreement with previously proposed and widely used non-inductive interconnect model.

Based on the proposed transformation function, simple expressions for calculating overshoot time and voltage as well as propagation delay were derived. In addition, novel parameter, which is to be called as inductive index A , is proposed for showing the strength of inductive effect. Interconnect is less-inductive or behaves as resistive-capacitive interconnect when A is less than 1. Otherwise, inductive effect may need to be considered.

Simulation is carried out with considering various input signals. For typical and slow input signals with wide range of parameters, the errors of overshoot and propagation delay

are 17% and 15%, respectively.

Using inductive index, it is also shown that the trend of inductive effect of single-line. With minimum width, inductive effect of interconnect peaks off at 90 nm based on ITRS predicted parameters.

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