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Area Comparison between 6T and 8T SRAM Cells in Dual-V_{dd} Scheme and DVS Scheme

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SUMMARY This paper compares areas between a 6T and 8T SRAM cells, in a dual-V_{dd} scheme and a dynamic voltage scaling (DVS) scheme. In the dual-V_{dd} scheme, we predict that the area of the 6T cell keep smaller than that of the 8T cell, over feature technology nodes all down to 32 nm. In contrast, in the DVS scheme, the 8T cell will becomes superior to the 6T cell after the 32-nm node, in terms of the area.

key words: *6T SRAM cell, 8T SRAM cell, V_{th} variation*

1. Introduction

As a CMOS process technology in an SoC is advanced, its minimum feature size is scaled down, which enables higher density and lower chip cost. Since a chip area of 80% or more is supposed to be occupied with memories [1] like large-capacity SRAMs for storing data, smaller-area SRAMs are required in terms of chip cost and yield. However, the technology scaling expands threshold-voltage (V_{th}) variation in MOS transistors due to random dopant fluctuations, and thus degrades operating (read and write) margins in an SRAM cell. To suppress the V_{th} variation, a larger-size transistor is preferable because a standard deviation of V_{th} (σ_{Vth}) is proportional to $1/\sqrt{L_{eff}W_{eff}}$ [2], where L_{eff} and W_{eff} are an effective channel length and width of a MOS transistor, respectively.

Figure 1 illustrates a schematic and layouts of the conventional 6T SRAM cell with various β ratios (a size ratio of a drive transistor to an access transistor) and γ ratios (a size ratio of an access transistor to a load transistor). The layout is designed with a 90-nm logic rule, and is arranged in parallel, not symmetrically. Also, it is not rectangular in shape, because the channel width of the drive transistor is different from that of the access transistor. The read and write margins in the 6T cell are improved by increasing β and γ ratios, respectively. This fact implies that the drive transistor is far larger than the load transistor to satisfy both the read and write margins. In Fig. 1(c), the β and γ ratios are set to 2.5 and 1.0, respectively, in order to obtain the read and write margins at an operating voltage of 1.0 V. As threshold-voltage variation condition, we assume that, at

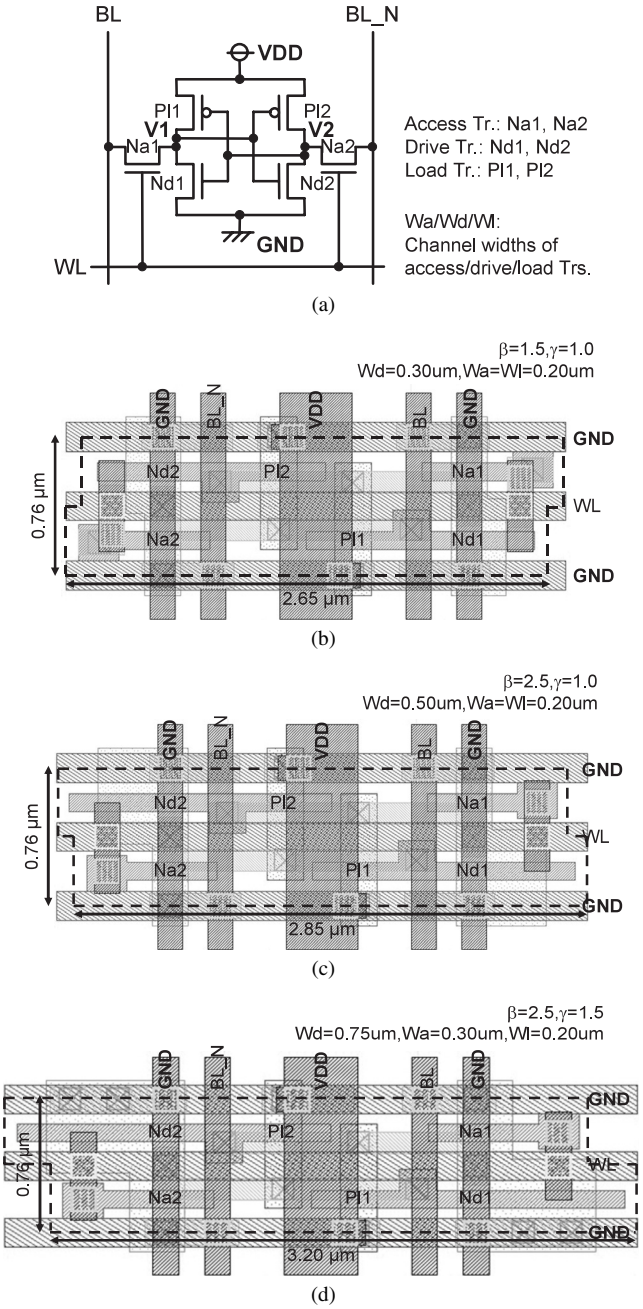

Fig. 1 (a) A schematic, and layouts of a 6T SRAM cell with (b) $\beta = 1.5$ and $\gamma = 1.0$, (c) $\beta = 2.5$ and $\gamma = 1.0$, and (d) $\beta = 2.5$ and $\gamma = 1.5$. The layouts are designed with a 90-nm logic rule.

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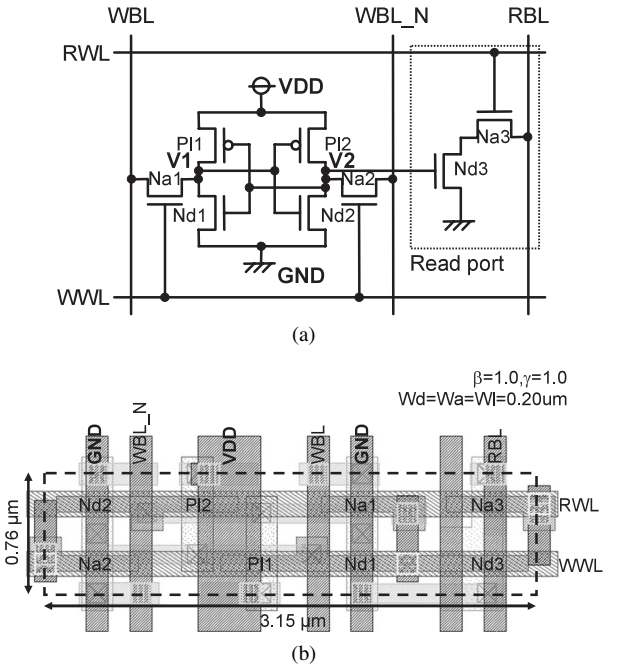


Fig. 2 (a) A schematic and (b) layout of an 8T SRAM cell designed by the same rule as Fig. 1(b)–(d).

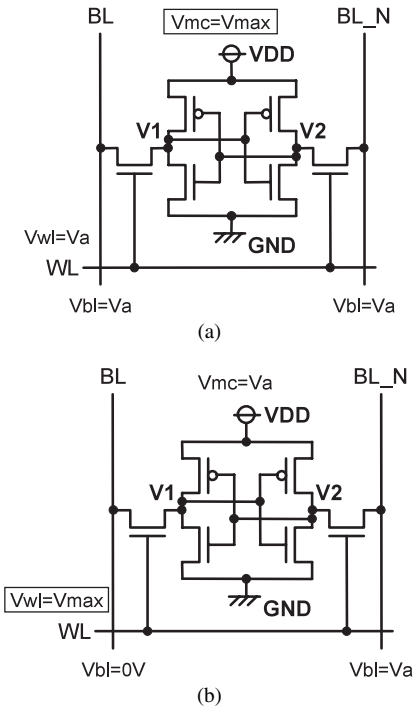


Fig. 3 Voltage controls in a 6T SRAM cell on a (a) read and (b) write conditions.

the 90 nm node, the global (wafer-to-wafer/lot-to-lot) component is three times of the standard deviation of the process deviation and the local (random) component is 6 σ_{Vth}. In the 6T cell, the cell area turns out larger, as the local variation (σ_{Vth}) is increased or a supply voltage (V_{dd}) is decreased.

In contrast, in an 8T SRAM cell shown in Fig. 2(a), the β ratio does not need to be enlarged because the 8T cell has a separate read port comprised of two transistors. The layout in Fig. 2(b) is, however, still larger than that in Fig. 1(b) by 10% at the 90-nm node, which is due to the separate read port. We have clarified that, in a single-V_{dd} scheme, the area of the 8T cell can be smaller than that of the 6T cell even if the 8T cell is utilized as a single-port SRAM cell [3].

A low power is of importance as well as a small area. Thus, a low V_{dd} is required. In particular, in a dynamic voltage scaling (DVS) scheme, the minimum operating voltage (V_{min}) has to be reduced in order to achieve wide-range power scaling on an SoC. For the 6T and 8T cells, we have proposed voltage-control schemes for sufficient operating margins at low V_{dd} [4], [5]. In these schemes, two voltages are supplied and selectively controlled in the SRAM cells. The read and write margins become larger even at lower V_{dd}, which in turn allows smaller area. In this paper, we report the area comparison between the 6T and 8T cells with the voltage-control scheme. In addition to the DVS scheme, we will focus on a dual-V_{dd} scheme.

The rest of this paper is organized as follows. The next section describes the voltage-control schemes for the 6T and 8T cells from a viewpoint of operating margins. In Sects. 3 and 4, we make area and access time comparisons, respectively. Section 5 summarizes this paper.

2. Voltage-Control Schemes for 6T and 8T Cells

2.1 Dual-V_{dd} Scheme

To improve the operating margins at low voltage, in this subsection, we apply the dual-V_{dd} scheme to both the 6T and 8T cells. Two fixed voltages (V_a and V_{max}, $V_{max} > V_a$) are provided to the SRAM cells, and the supply voltage in the memory cells (V_{mc}) and the wordline (WL) voltage (V_{wl}) are switched according to the read and write conditions. In this paper, V_{max} is set to 1.0 V as a nominal voltage.

As shown in Fig. 3(a), in a read operation, V_{mc} is set to V_{max} that stabilizes a stored datum, which maximizes a read margin. Alternatively in a write cycle, V_{wl} is set to V_{max} as illustrated in Fig. 3(b), which increases the conductance of the access transistors. This operation makes a bitline datum easily written, and thus improves the write margin.

On the other hand, in the 8T cell, the write-WL (WWL) voltage (V_{wwl}) is merely set to V_{max} as shown in Fig. 4, since we do not have to pay attention to the read margin.

2.2 DVS Scheme

Under the DVS environment depicted in Fig. 5, the fixed V_{max} is applied externally, but V_a is adaptively controlled and varied with a DC/DC converter according to a clock frequency. V_a is between V_{min} and V_{max}. In the DVS scheme, both V_a and V_{max} are provided to the SRAM cell. Note that V_a is dynamically changed in operation unlike the dual-V_{dd} scheme.

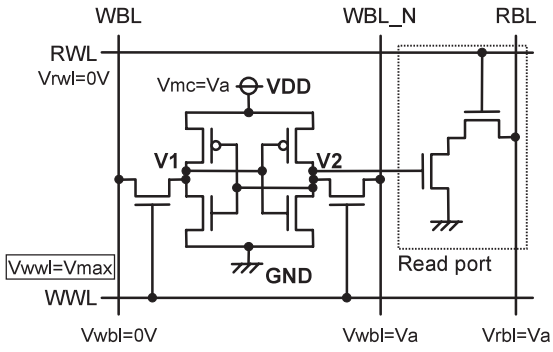


Fig. 4 Voltage control in an 8T SRAM cell on a write condition.

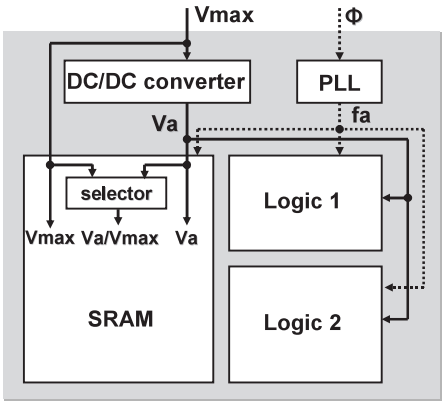
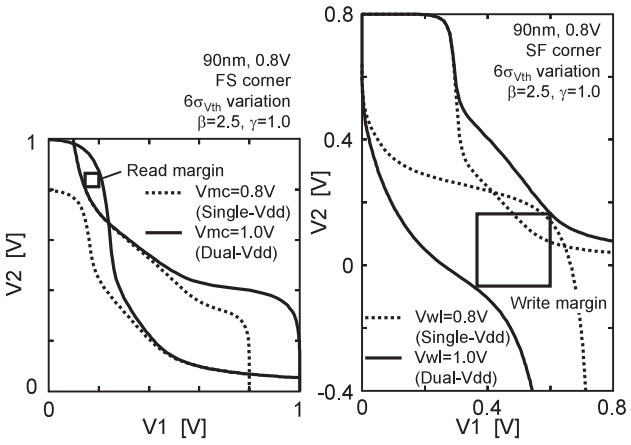


Fig. 5 Block diagram of DVS scheme.

In the DVS scheme, V_{mc} and V_{wl} in the 6T cell and V_{wwl} in the 8T cell are controlled as well as the dual-V_{dd} scheme. Since V_a is varied, we have to consider the worst-case read margin where $V_a = V_{max}$. Similarly, the worst-case write margin takes place when $V_a = V_{max}$. In any event, the worst-case operating voltage of V_a is V_{max}, which means that the DVS scheme is the same as the conventional single-V_{dd} scheme at $V_a = V_{max}$ (1.0 V) in terms of the operating margins.

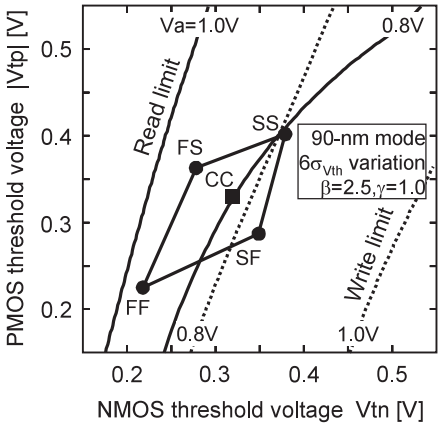
2.3 Improvement of Operating Margins

The improvement of the operating margins with the dual-V_{dd} scheme is illustrated in Fig. 6 through Fig. 8 by means of butterfly plots [6] and milky-way plots [7]. Figure 6 and Fig. 7 correspond to the 6T-cell case, and Fig. 8 is the 8T-cell case. The diamond shape in the milky-way plot indicates the process corners (FF, FS, SF, SS, and CC corners), where a global V_{th} variation of the triple standard deviation is reflected. As for the random V_{th} variation, $6\sigma_{vth}$ is considered in an SRAM cell. In the milky-way plots, the read margin cannot be obtained on the left side from the read limit curve, where a stored datum possibly flips in read operation. Similarly, the write margin is not satisfied on the right side from the write limit curve. In the 6T-cell case, the read and write margins are both obtained in the region between the read and write limit curves, which means that the 6T cell works correctly under the V_{th} variation. On the other hand, in the 8T cell, the write operation curve is the only constraint, and the write operation will pass in the region on the left side from the write limit curve.

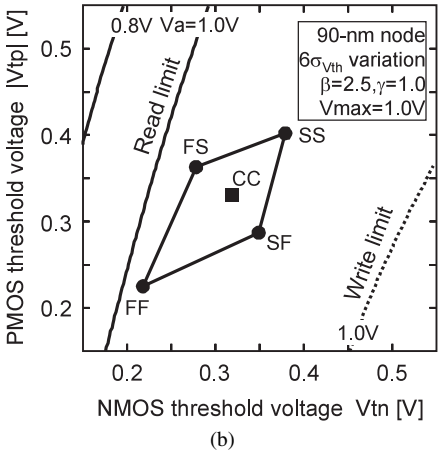


(a) Read condition. (b) Write condition.

Fig. 6 Improvement of read and write margins.



(a)



(b)

Fig. 7 Milky-way plots of a 6T cell in (a) the conventional single-V_{dd} scheme and (b) dual-V_{dd} scheme. A write-limit curve at V_a = 0.8 V in the dual-V_{dd} scheme is out of the graph.

In the conventional single-V_{dd} scheme, V_{max} is equal

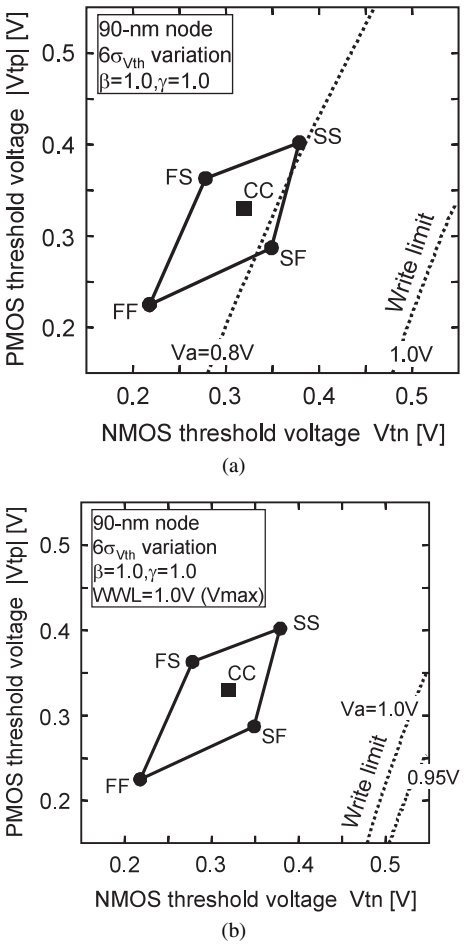


Fig. 8 Milky-way plots of an 8T cell in (a) the conventional single-V_{dd} scheme and (b) dual-V_{dd} scheme.

to V_a. Figure 6 illustrates the case that the channel-width ratios of $\beta = 2.5$ and $\gamma = 1.0$ are the minimum values for the schemes to satisfy both the read and write margins at $V_a = V_{max} = 1.0$ V in the 6T cell. If $V_a = V_{max} = 0.8$ V, there is neither read margin nor write margin. Figure 7 explains that the 1.0 V has the operating margins from another aspect. The lines of the 0.8 V intersect the diamond shape, which exhibits neither margin.

Figure 7(b) shows that, the region between the read and write limits in the dual-V_{dd} scheme becomes wider as V_a is reduced. This is because the dual-V_{dd} scheme improves the operating margins as described in Sect. 2.1. In other words, the dual-V_{dd} can have sufficient margins at a low V_a, with smaller β and γ values. This implies that the cell area in the dual-V_{dd} can be reduced if a low V_a is given.

In the 8T cell, the read margin does not need to be considered. However, we have to pay attention to the write margin. Figure 8 illustrates that the single-V_{dd} scheme does not have a write margin at V_a of 0.8 V, while the dual-V_{dd} has one. Note that, in the single-V_{dd} scheme, the write margin in the 8T cell becomes slightly larger than that in the 6T cell (compare the write limit curves in Fig. 7(a) and Fig. 8(a)), because the smaller β ratio in the 8T cell makes the logical V_{th} of the cell inverter higher and helps stable "H"-write operation at the "L"-stored node.

3. Area Comparison

In this section, we compare the areas of the 6T and 8T cells in the dual-V_{dd} scheme, the single-V_{dd} scheme, and the DVS scheme with a varied V_a. The design conditions are as follows;

- The transistor length (L) of each transistor is set to the minimum (L_{min} = design rule).
- The load transistor has the minimum channel width (W_{min}).
- L_{min} and W_{min} are scaled by 0.7 time per generation.
- In the 6T cell, the channel width of the access transistor (W_a) is first optimized for the write margin, on the condition of $W_d = W_{min}$ (W_d: the channel width of the drive transistor). Then, W_d is optimized for the read margin.
- In the 8T cell, we merely optimize W_a for the write margin. W_d is set to W_{min} since the read margin can be neglected.
- The global V_{th} variation (the size of the diamond shape) remains constant in any generation since the global V_{th} is determined by manufacturing equipments and environments.
- However, the process corners can be shifted in parallel over a V_{th} range of ±0.1 V. Namely, we can set the nominal V_{th} (the CC corner) in the range of ±0.1 V. The V_{th} setting is optimized to minimize the area.
- The channel width of Na3 and Nd3 at the read port in the 8T cell are set to 0.20 μm and 0.40 μm in a 90-nm node, respectively, and scaled down by 0.7 time per generation.

The operating margins are verified by HSPICE DC simulation. An industrial 90-nm model is utilized, and we apply it to the simulations from the 65-nm to the 32-nm technology nodes. The V_{th} variations in the advanced technology nodes are illustrated in the Pelgrom plots in Fig. 9, which are based on the ITRS Roadmap [1]. σ_{Vth} becomes larger along with the process generations due to the smaller channel area ($L_{eff} \cdot W_{eff}$), although the oxide thickness (T_{ox}) is gradually thinned and the slopes of the Pelgrom plots get gentler.

3.1 Single-V_{dd} Scheme

Figure 10 and Fig. 11 illustrate the β and γ ratios and the cell area dependencies on technology nodes, in the conventional single-V_{dd} scheme. In the 8T cell, W_d and W_a can be set to W_{min} over all process nodes at 1.0 V, which demonstrates that the 8T already achieves the minimum area. In the past, the areas of both the 6T and 8T cells have been scaled down almost by half, along with the technology nodes. However in the future, the β and γ ratios in the 6T cell should be larger as the process is advanced. This makes the cell area larger

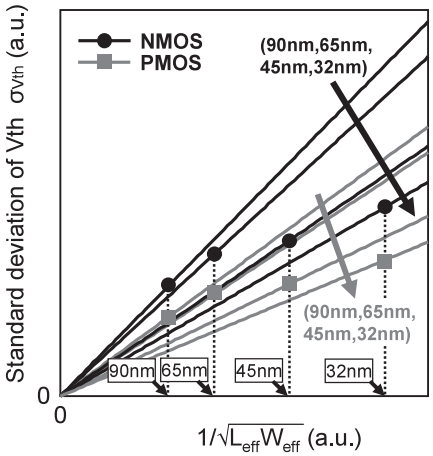


Fig. 9 Pelgrom plots in different processes. These plots are derived from the ITRS [1].

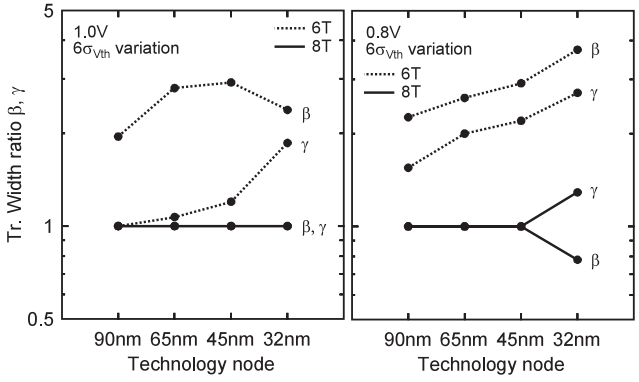


Fig. 10 β and γ ratios in the conventional single-V_{dd} scheme.

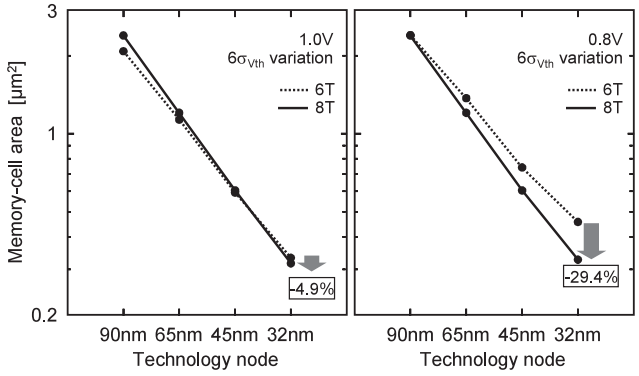


Fig. 11 Area comparison between a 6T and 8T cells in the conventional single-V_{dd} scheme.

in the 6T cell, resulting in the gentler slopes as illustrated in Fig. 11.

In the 1.0-V operation, the curves of the memory-cell area intersect at the 45-nm node and the area of the 8T cell becomes smaller by 4.9% at the 32-nm node, as illustrated in Fig. 11. If V_{dd} is 0.8 V, the 8T cell is further superior to the 6T cell at the 65-nm node and later. The area of the 8T cell is smaller by 29.4% at the 32-nm node. Note that, in the

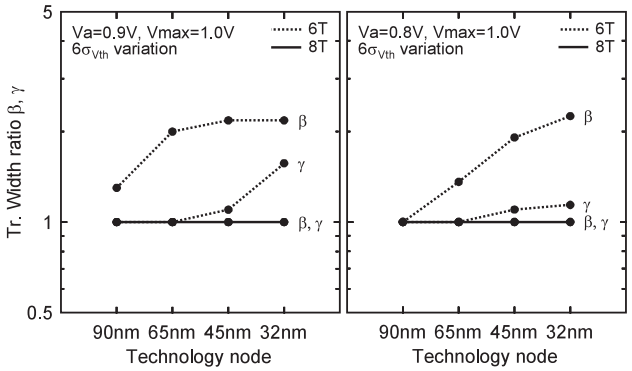


Fig. 12 β and γ ratios in the dual-V_{dd} scheme.

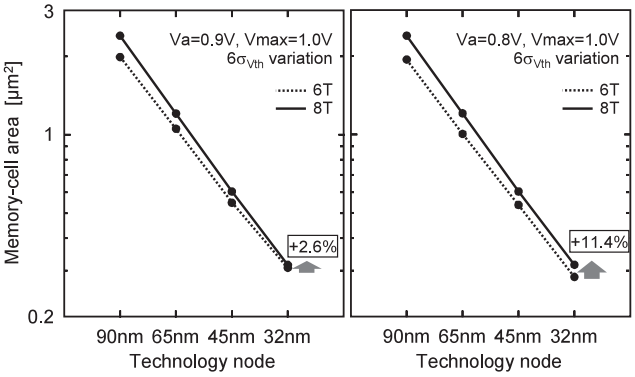


Fig. 13 Area comparison between a 6T and 8T cells in the dual-V_{dd} scheme.

0.8-V operation at the 32-nm node, W_a has to be increased to obtain the write margin even in the 8T cell. Thus, the γ ratio is increased, but the β ratio is decreased.

We would like to mention the leakage currents of the 6T and 8T cells. Since the target V_{th} values in the 6T and 8T cells are independently set for the minimum cell areas, the leakage currents in the 6T and 8T cells are different. In particular, in the 8T cell, a low nMOS V_{th} (V_{tn}), and a low pMOS V_{th} (V_{tp}) or a high absolute value of V_{tp} ($|V_{tp}|$) are optimum for the minimum cell area. On this condition, the write margin is expanded, and thus W_a or the γ ratio can be narrowed. As for the 6T cell, the optimum V_{th} point is in moderate V_{th} setting. Consequently, the leakage current in the 8T cell is 8.1 times as large as that in the 6T cell.

3.2 Dual-V_{dd} Scheme

In the dual-V_{dd} scheme, the β and γ ratios of the 6T and 8T cells can be smaller than those in the single-V_{dd} scheme because the low V_a improves the operating margin. Thus, the dual-V_{dd} scheme can potentially save the cell area. Figure 12 illustrates the β and γ ratios dependencies on technology nodes.

As shown in Fig. 13, the area of the 6T cell is always smaller than that of the 8T cell at a V_a of 0.9 V since the β ratio in the 6T cell becomes much smaller than the single-V_{dd} scheme case. Besides, we can make the β and γ ratios

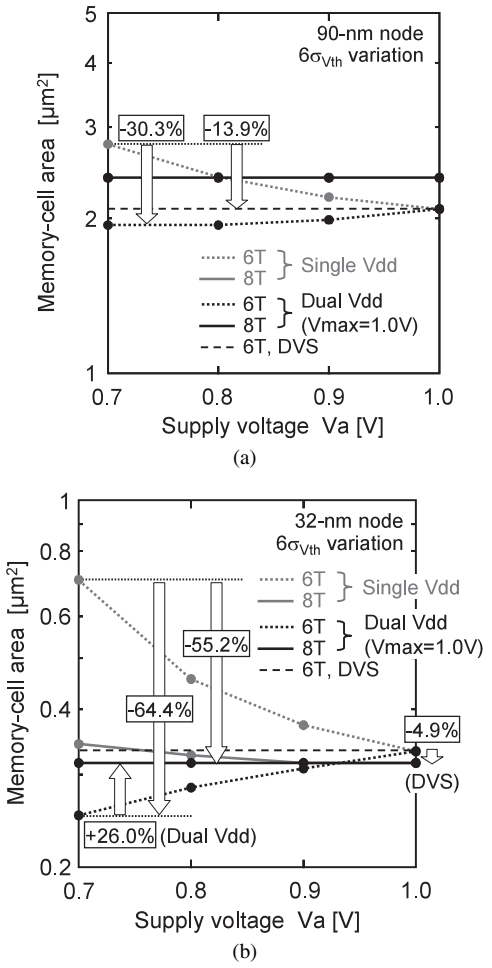


Fig. 14 Area dependencies on V_{dd} at a (a) 90-nm and (b) 32-nm nodes. The lines of an 8T-cell area with DVS scheme overlap those with dual-V_{dd} scheme.

smaller as V_a is reduced, which results in a smaller area than that in the single-V_{dd} scheme. For instance, at a V_a of 0.8 V, the area of the 8T cell is larger than that of the 6T cell by 11.4%.

3.3 Area Dependency on V_{dd}

The area of the 6T and 8T cells dependencies on V_{dd} are summarized in Fig. 14. The cell area in the DVS scheme is the same as that at $V_a = 1.0$ [V], which is the worst-case V_{dd} of operating margins as previously described. At the 90-nm technology node, the areas of the 8T cell with dual-V_{dd} and DVS schemes are always larger than those of the 6T cell. On the other hand, at the 32-nm node, the 8T cell is superior to the 6T cell when V_a is around 1.0 V and DVS scheme is utilized. When the dual-V_{dd} scheme is applied, the 6T cell is still preferable at less than 0.9 V where operating margins are larger than those in a 1.0-V operation.

At the 32-nm process node, in the DVS scheme, the area of the 8T cell can be smaller by 4.9% than that of the 6T cell. In contrast, in the dual-V_{dd}, the 8T-cell area is larger than the 6T-cell area by 26.0% in the 0.7-V operation.

Compared to the 6T cell with the conventional single-V_{dd} scheme, the 6T cell with the dual-V_{dd} scheme reduces the area of 64.4%, and the 8T cell with the DVS scheme achieves the area saving of 55.2% in the 0.7-V operation and at the 32-nm technology node.

4. Access Time Tradeoff

This section compares an access time and total area in a whole SRAM macro comprised of a 6T-cell array (6T-SRAM macro) and an 8T-cell array (8T-SRAM macro). The 6T-SRAM and 8T-SRAM macros have peripheral circuitry, such as address decoders, read/write circuitry, and so on. For the dual-V_{dd} and DVS schemes, the WL level shifters are also introduced just after X decoders in order to amplify the WL voltage in the 6T-SRAM macro or the WWL voltage in the 8T-SRAM macro.

In our cell design, the channel widths of all the transistors are optimized only by the operating margins under the V_{th} variation in order to obtain the stable read/write operations, as previously mentioned. Considering the access time of the SRAM macro, the 6T cell can read out faster thanks to the differential bitlines, while the 8T cell has a longer access time due to the single-ended read bitline (RBL in Fig. 4). To fasten the read access in the 8T-SRAM macro, we adopt the hierarchical-bitline structure [8] that hierarchically accesses with a local RBL (LRBL) and a global RBL (GRBL). However, it causes an area penalty in the 8T-SRAM macro. Note that a single-bitline structure is sufficient for the 6T-SRAM macro.

Figure 15 illustrates the area and access time ratios of the 8T-SRAM macro to the 6T-SRAM macro, in a 128-kb (128 bits × 1024 words) memory, where the single-V_{dd}, dual-V_{dd}, and DVS schemes are considered. In the simulation, the access time is defined as the period, from the time when the wordline is asserted, to the time when the differential bitline voltage becomes 100 mV in the 6T-SRAM macro, or to the time when the GRBL voltage is dropped by a half of the operating voltage in the 8T-SRAM macro. The process corner is set to SS corner and the local V_{th} variation of $6\sigma_{Vth}$ is reflected to the 6T and 8T cells as the worst-case access time. The horizontal axis in the figure is the number of memory cells connected to the LRBL in the 8T-SRAM macro (N_{mc}). As N_{mc} is increased, the access time of the 8T-SRAM macro is longer, while the area overhead of it becomes smaller and the area ratio of the macro becomes almost equal to that of the cell.

As shown in Fig. 15(a), the access time of the 8T-SRAM macro can be shorter than that of the 6T-SRAM macro in the single-V_{dd} scheme, if N_{mc} is set to a smaller value. Even when N_{mc} is set to 128 and the operating voltage is 1.0 V, for example, we can obtain both the shorter access time and smaller macro area by 3.2% and 2.9%, respectively.

In the dual-V_{dd} and DVS schemes shown in the Fig. 15(b)(c), the access-time ratio is always smaller than one. This is because the access time in the 8T cell is gov-

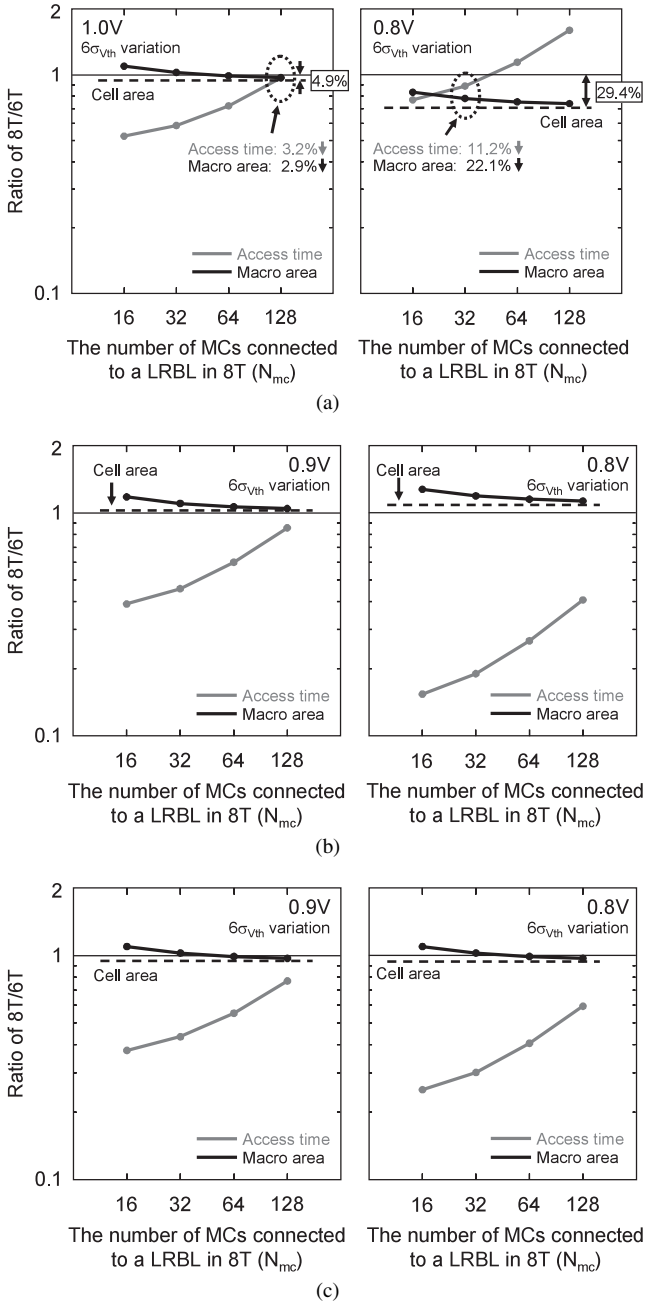


Fig. 15 The access time and area comparisons between the 128-kb 6T- and 8T-SRAM macros in the (a) single-V_{dd}, (b) dual-V_{dd}, and (c) DVS schemes. The technology node is 32 nm.

erned by the separate read port, although the β ratio or W_d value in the 6T cell is set to a small value. In the dual-V_{dd} scheme, the β ratio is smaller as V_a is decreased as previously mentioned in Fig. 12. Also, the worst-case operating voltage in the DVS scheme is 1.0 V, and, even if V_a is lower than 1.0 V, the β ratio is set to a value at $V_a = 1.0$ V, which is smaller than that in the single-V_{dd} scheme. The access time of the 6T-SRAM macro with the dual-V_{dd} or DVS scheme is thus longer.

5. Conclusions

In this paper, we clarified that, in the dual-V_{dd} scheme, the area of the 6T SRAM cell keeps the area smaller than that of the 8T SRAM cell, over feature process nodes. In contrast, in the DVS scheme, the 8T cell is preferable in a 32-nm process technology. The DVS scheme saves the 8T cell area by 4.9% compared with the 6T-cell case in the 32-nm node.

Considering a 0.7-V operation at the 32-nm node, the area of the 6T cell is smaller by 64.4% in the dual-V_{dd} scheme than the single-V_{dd} scheme. The DVS scheme achieves the area saving of 55.2% with the 8T cell, compared with the 6T cell in the single-V_{dd} scheme.

Acknowledgment

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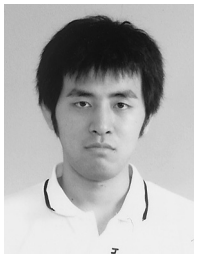

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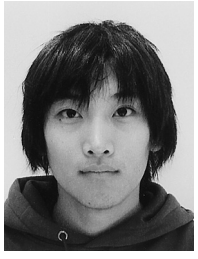

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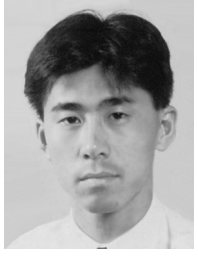

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