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製造ばらつきを考慮したセンサネットワークノード消費電力モデルの提案と評価

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あらまし ワイヤレスセンサネットワークでは、ライフタイムの拡大が最も重要な課題である。ネットワークのライフタイムを拡大するためには、システム全体の最適設計をしなければならない。設計したシステムを評価するために、シミュレータに実装可能なセンサノードの消費電力モデルが求められていた。本研究では、センサノードの消費電力モデルに、現在CMOS回路で問題となっている閾値電圧の製造ばらつきを導入した。従来モデルと比較すると、閾値電圧ばらつきを考慮した場合、消費電力がばらつき、平均消費電力が増大することが判明した。さらに、ネットワークシミュレータに実装し、ネットワークレベルで比較した。その結果、従来のモデルはばらつきのあるモデルよりもシステムライフタイムを長く見積もる傾向にあることがわかった。

キーワード ワイヤレスセンサネットワーク，閾値電圧ばらつき，消費電力モデル

Impact of Node Power Variation against Life Time of Sensor Networks

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Abstract We introduced manufacturing variation into a power model for a wireless sensor network node. Network protocols for wireless sensor networks such as media access control and routing should be evaluated in terms of life time as a whole system. In fact, there exists variation in power node-by-node due to the manufacturing variation. In the previous research, however, this effect has not been investigated at all since it has been supposed that all nodes have the same power. In this paper, we develop a more exact power model for sensor nodes, which we name the threshold-voltage variation model, considering threshold-voltage variation in a manufacturing process. A microprocessor and RF part are considered as hardware blocks in the model, which is then implemented to QualNet in order to evaluate the impact on the life time. The simulation results show that the conventional model overestimates the life time longer than our model.

Keyword Wireless sensor network, Threshold-voltage variation, Power mode

I. INTRODUCTION

In wireless sensor networks (WSNs), expansion of available time, i.e. life time, is one of the most important subjects. Network protocols for WSNs such as media access control and routing should be evaluated in terms of life time in a whole network system. Therefore, many researchers have implemented their proposed protocols into network simulators such as NS-2 and QualNet [1-2]. In their studies, every node has the same power performance. However in fact, there exists variation in power node-by-node due to manufacturing variation, where only a few nodes with high power consumption may shorten the network life time. To the best of our knowledge, however, this aspect has not been addressed at all.

Process, voltage, and temperature (PVT) are major factors of variation in CMOS VLSI process. The process variation is called a manufacturing variation, which is twofold: systematic variation, and random variation. Although both variations take the form of a threshold-voltage variation, behaviors are different. The random variation appears as a transistor-by-transistor variation while the systematic one is observed as a chip-by-chip variation. The random variation is mitigated in a chip power since millions transistors are distributed on a chip. In this paper, therefore, we consider only the systematic variation as a first step. To the best of our knowledge, scientific data about threshold-voltage variation in a latest CMOS process technology has not been published.

In this paper, we address the effect of power variation of nodes on system-level performance, i.e. network life time. First, we develop a power model for a node considering threshold-voltage variation in a microprocessor and RF (radio frequency) part, which we call the *threshold-voltage variation (TV) model*. We then implement the model into QualNet, which is one of network simulators, and evaluate the effect of the power variation on network life time.

The rest of the paper is organized as follows: In Section II, we show a typical architecture of sensor node. In Section III, we build a model of threshold-voltage variation based on variation of an operating frequency in an Intel microprocessor. In Section VI, we describe power variation in the node chip compared with the conventional *threshold-voltage constant (TC) model*. In Section V,

we exhibit a result of network simulation. Finally, we conclude the paper in Section VI.

II. Sensor Node Architecture and Power Components

Fig. 1 shows a typical schematic of a sensor node. A small battery, solar cell, or even energy scavenging such as vibration energy [3] is utilized as a power source, and thus its output voltage is not unregulated. The step-down DC-DC converter in the figure regulates the output voltage of the power source to a lower one, which is supplied to a node chip as a rated supply voltage (V_{dd}). If the output voltage of the power source becomes lower than V_{dd}, the node chip goes down since the step-down DC-DC converter cannot compensate the negative voltage gap. A node chip is generally comprised of two blocks; a microprocessor and RF part. An RF part receives/transmits data and control packets from/to other sensor nodes by means of radio waves, and a microprocessor process them.

The node chip actually has power variation derived from threshold-voltage variation, and thus a life time of the sensor node is strictly varied node-by-node. In this paper, the impact against the life time in the sensor nodes caused by the power variation is described. Note that an energy variation in the power source is not considered, but if its variation is known, a similar analysis can be carried out.

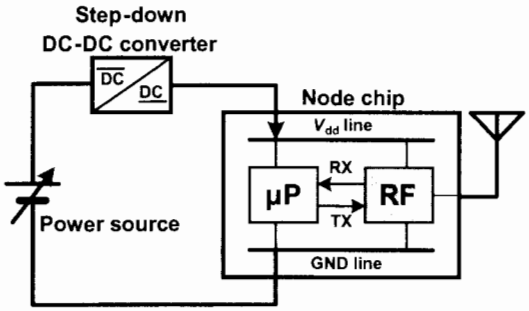

Fig. 1. A typical sensor node. μP signifies a microprocessor.

A power in the node chip, P_{node}, is given as follows:

$$P_{node} = (P_{\mu P} + P_{RF}) / K_{DCDC}, \quad (1)$$

where $P_{\mu P}$ and P_{RF} are powers of a microprocessor and RF part, respectively. K_{DCDC} is an efficiency of a DC-DC converter, and achieves more than 90%[4].

A. Power in Microprocessor

In a CMOS digital circuit, a switching delay, T_p, is briefly expressed as a time to take a gate capacitance, C_L, to be charged/discharged by a transistor on-current, I_{on}. When there are n logic gates serially connected in a critical path, the maximum operating frequency, f_{max}, is given as follows:

$$f_{max} \propto \frac{1}{nT_p} = \frac{I_{on}}{nQ_L} = \frac{(V_{dd} - V_{th})^{\alpha}}{nC_L V_{dd}} = K_1 \frac{(V_{dd} - V_{th})^{1.5}}{nV_{dd}}, \quad (2)$$

where $I_{on}=(V_{dd}-V_{th})^{\alpha}$ and α is a velocity saturation index [5]. If $\alpha=2$, it is said that I_{on} is based on the classic Shockley model, however in a scaled process technology, α is lowered and set to 1.5 in this paper [6]. A rated operating frequency, f_{op}, must be lower than f_{max}.

Power consumed in a digital circuit is comprised of two components. A power in a microprocessor, $P_{\mu P}$, includes a dynamic power, P_{dyn}, and subthreshold-leakage power, P_{leak}, as well.

1) Dynamic power

P_{dyn} is a charge/discharge power along with transistor switching, which is proportional to f_{op}, and the square of V_{dd} [7].

$$P_{dyn} = K_2 f_{op} C_L V_{dd}^2. \quad (3)$$

2) Subthreshold-leakage power

Even when a transistor is in a subthreshold region, a subthreshold-leakage current flows through the transistor, which is P_{leak}. P_{leak} results in larger one as V_{th} becomes lower [7]:

$$P_{leak} = K_3 V_{dd} 10^{-V_{th}/S}, \quad (4)$$

where S is a subthreshold swing, which is about 0.1 V/decade in a recent process technology. This implies that a subthreshold-leakage current goes up to ten times when V_{th} is reduced by 0.1 V.

B. Power in RF Part

In the RF part, transistors are biased to an intermediate voltage by a bias circuit, which always draws a bias current in an analog circuit. The biased transistor is usually in a saturation region, and the bias current is unfortunately dominant.

In an analog-circuit design, long-channel transistors are utilized to avoid the channel-length modulation effect and obtain the ideal saturation characteristics. A power in the RF part is represented as follows [8]:

$$P_{RF} = \beta V_{dd} (V_{gs} - V_{th})^{\alpha} = \beta V_{dd} (V_{gs} - V_{th})^2, \quad (5)$$

where β is a current amplification factor. α is set to two since a long-channel transistor is used in the analog-circuit design, while it was 1.5 in the digital circuit as previously mentioned.

III. Threshold-Voltage Variation Model

In every chip, doping concentration and oxide thickness are different due to manufacturing variation, which basically causes the threshold-voltage variation.

1) Threshold-Voltage Variation in Intel High- Performance μP

A distribution of chip frequencies in Intel high-performance microprocessors, which are determined by critical-path delays, was reported [9]. Fig. (a) is the distribution of the chip frequency. From this, we can conjecture the threshold-voltage variation as the systematic variation.

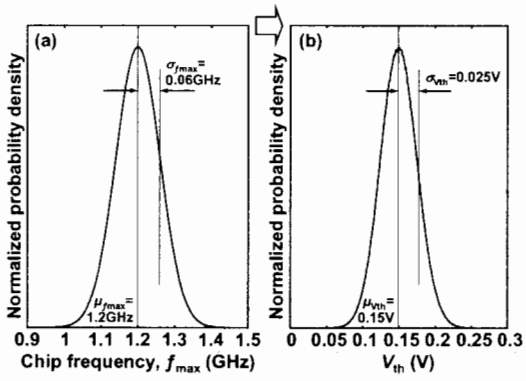

Fig. 2. Chip frequency distribution in Intel microprocessors, and its estimated distribution of threshold voltage.

Using (2), the threshold-voltage variation can be estimated as follows:

$$V_{th} = V_{dd} - \sqrt[1.5]{\frac{nf_{max}V_{dd}}{K_1}}. \quad (6)$$

As the design parameters of the Intel microprocessor, we set V_{dd} and μ_{Vth} to 0.9 V and 0.15 V, respectively. The critical path has 14 logic gates (n=14). Therefore, the constant, K_1, is 23.3×10^6 in (6). Fig.

(b) is the estimated distribution of the threshold voltage. The standard deviation of the threshold voltage in the Intel microprocessor, σ_{Vth}, is 0.025 V.

2) Threshold-Voltage Variation in Sensor Node

Since a frequency of 1.2 GHz and threshold voltage of 0.15 V in the Intel microprocessor are too fast and leaky for a node chip, we modify the design parameter. n in the Intel microprocessor is also small due to micro pipelining, however, we can mitigate it, and n is increased to three times in the node chip. As for the threshold voltage of the node chip, μ_{Vth} is shifted to 0.3 V as shown in Fig. (a) in order to suppress a subthreshold-leakage current. V_{dd} is set to 1.2 V.

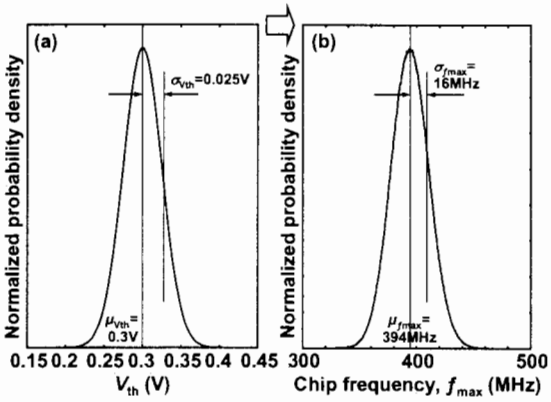

Fig. 3. Estimated distributions of threshold voltage and maximum operating frequency in sensor node.

We assume that the node chip is made with the same manufacturing process as the Intel microprocessor, and thus σ_{Vth} in the node chip is set to 0.025 V. Fig. (b) illustrates the estimated distribution of the maximum operating frequency under the conditions, where μ_f=394 MHz and σ_{fmax}=16 MHz. Table 1 summaries the design parameters.

TABLE I. Design parameter comparison between Intel high-performance processor and node chip.

	Path length	Vdd	μVth	σVth	μfmax	σfmax
Intel μP [7]	14 gates	0.9 V	0.15 V	0.025 V	1.2 GHz	0.06 GHz
Node chip	42 gates	1.2 V	0.3 V	0.025 V	394 MHz	16 MHz

3) Yield of Node Chip

Although there is the variation of the maximum operating frequency in the node chips, a rated operating frequency is uniquely settled to all nodes, which is generally set lower to enhance yield. Fig. 4 is the yield curve of the node chips. If the margin is set to $3\sigma_{fmax}$, in other words, if the rated operating frequency is 0.345 GHz ($=\mu_{fmax}-3\sigma_{fmax}$), the yield achieves 99.87%, which is high enough.

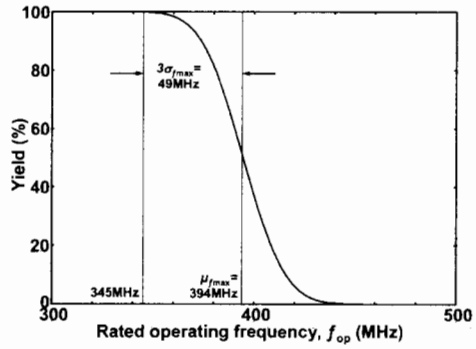

Fig. 4. Yield of node chips.

IV. Power Variation

A. Power Variation in Microprocessor

Power optimization by controlling V_{th} and V_{dd} is a difficult problem. If V_{th} is large, V_{dd} must be large to maintain a speed of a circuit, which turns out to large power. To the contrary, if V_{th} is small, V_{dd} can be small, and thus a dynamic power can be small. However, this increases a subthreshold-leakage power. According to [10], a power consumed in a digital circuit is minimized when a subthreshold-leakage power occupies 30% of a total power at a threshold voltage of $\mu_{Vth}-3\sigma_{Vth}$.

Once a rated operating frequency is fixed, P_{dyn} in (3) is fixed as well in all node chips.

$$P_{dyn} = K_p V_{dd}^2, \tag{7}$$

where $K_p=K_2 f_{op} C_L$. In the optimum design, P_{leak} should be $3P_{dyn}/7$ when $V_{th}=\mu_{Vth}-3\sigma_{Vth}$ according to [10]. Therefore, (4) is rewritten as follows:

$$P_{leak} = \frac{3}{7} K_p 10^{-\frac{V_{th}-(\mu_{Vth}-3\sigma_{Vth})}{S}} V_{dd}^2, \tag{8}$$

which indicates that P_{leak} is varied node-by-node. P_{leak} is exponentially changed by the threshold-voltage variation.

B. Power Variation in RF Part

When $V_{gs}=V_{OD}+\mu_{Vth}$ (V_{OD} is called an overdrive voltage), (5) is rewritten as follows:

$$\begin{aligned} P_{RF} &= \beta(V_{OD}+\mu_{Vth}-V_{th})^2 \\ &= \beta(V_{OD}^2+2V_{OD}(\mu_{Vth}-V_{th})+(\mu_{Vth}-V_{th})^2) \\ &= \beta(V_{OD}^2+2V_{OD}(\mu_{Vth}-V_{th}) \\ &\quad (\because V_{OD} >> \mu_{Vth}-V_{th}) \end{aligned}, \tag{9}$$

which exhibits that P_{RF} is linearly changed by the threshold-voltage variation.

C. Power Variation in Node Chip

Since the microprocessor and RF part are located on a same chip, the threshold-voltage variation commonly affects to both.

$P_{\mu P}$ is a sum of (7) and (8). Supposing that P_{dyn}=1.2 mW, K_p becomes 1/1200 in (7) since V_{dd} is 1.2 V in the design. The value of 1.2 mW is reasonable compared with [11]. In the conventional TC model without the threshold-voltage variation, V_{th} only takes 0.3 V, and then $P_{\mu P}$ would be set to $P_{dyn}+P_{leak}$=1.2+0.16=1.36 mW. On the other hand in the proposed TV model, $P_{\mu P}$ is distributed due to the variation of the subthreshold-leakage power as shown in Fig. 5.

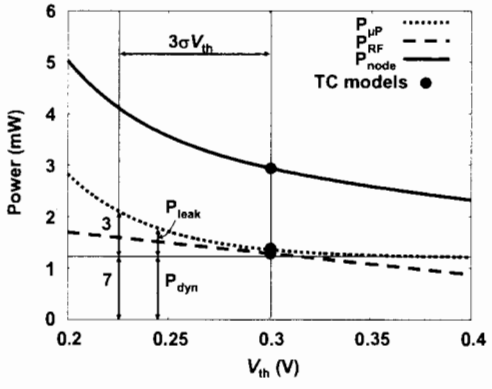

Fig. 5. Power variations in node chip.

As for P_{RF}, we carried out a circuit-level simulation to evaluate the threshold-voltage variation in the RF part, assuming the LNA. The

P_{RF} variation exhibits the linear characteristics, and given as follows:

$$P_{RF} = 10^{-3} K_4 (-3.43 V_{th} + 2.10) V_{DD} \quad (10)$$

where K_4 is a fitting parameter. K_4=1 means that P_{RF} is equal to P_{dyn} of the microprocessor at a threshold voltage of 0.3 V, and P_{RF} in this case is shown in the figure. In the conventional TC model, P_{RF} would be fixed to 1.29 mW.

P_{node} in the conventional TC model eventually becomes $(P_{\mu P} + P_{RF})/K_{DCDC}$=(1.36+1.29)/0.9=2.943 mW. In the proposed TV model, an average power of the node chips, μ_{Pnode}, is 2.976 mW, which is larger than the conventional one just by 1.12%.

V. Verification with Network Simulator

In this section, we introduce both power models with and without power variation in a network simulator, and investigate an impact of power variation on system-level performance from viewpoint of life time. The network simulator which we used is QualNet [2]. In the field of 100 x 100m^2, 256 sensor nodes are deployed at random, and a base station is placed in the center. Application is data gathering where each sensor node transfers its sensed data into the base station every round which is set to 1,000 seconds. A physical layer protocol is Low Power Listening [12], and its duty cycle ratio is set to 0.5%. MAC layer protocol is PAMAS [13]. A network layer protocol is tiny diffusion [14], and an interest is flooded only once at the beginning of a simulation trial. Before defining a metric of network life time, we define data acquisition rate by the ratio of the amount of data received by the base station in a round to the amount of data generated by all nodes in the round regardless of their life-and-death. We define life time as duration in which successful data received rate is 90% or more. Fig. 6 shows characteristics of successful data received rate in the cases of TV and TC power model. The powers of a microprocessor and RF part are in the ratios 1:1. Recall that TV power model consumes slightly more power than TC power model by 1.121% on average in Fig. 6. We observe that TV power model leads to shorter life time than TC power model by 10.75% rather than 1.121%. In TV power model case, some nodes have inefficient power performance. This fact can make the network vulnerable. By contrast, this effect is not involved in TC power model. This is reason why the figure shows that TC power model indicates optimistic results compared with TV power model. Microprocessor power is distributed more than RF part power as previously mentioned in Section IV. Node power is eventually distributed more as microprocessor power becomes dominant. This leads to the situation where more nodes have inefficient power performance, which makes the network more vulnerable. If sensor nodes are more sophisticated in the future, the variation of microprocessor power will influence system-level performance.

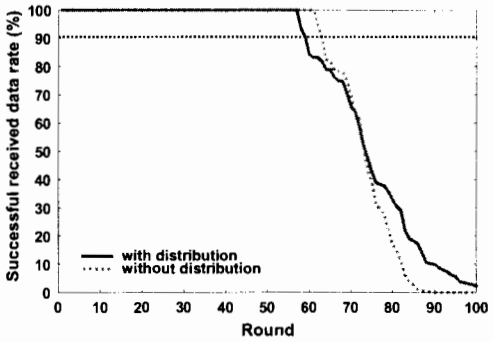

Fig. 6. Data received rate, μP:RF=I:1

VI. Summary

In this paper, we developed the power consumption model, which we named TV power model, considering manufacture variation of subthreshold voltage in a processor and an RF circuit, and implement the model to QualNet. Simulation results showed that the conventional power model which we call TC power model optimistically estimates network life time longer than our proposed TV power model by 10.75% although TV power model consumes slightly more power than TC power model by 1.121%.

In our future research, we will consider not only systematic variation but also random variation and peripherals and power source variations. We suppose that these factors enlarge variation of node power performance, which has a more significant impact on system-level performance such as network life time.

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