Subthreshold-Leakage Suppressed Switched Capacitor Circuit Based on Super Cut-Off CMOS (SCCMOS)

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ABSTRACT

A subthreshold-leakage suppressed switched capacitor (SC) circuit based on super cut-off CMOS (SCCMOS) scheme is introduced. This scheme realizes low-voltage SC circuits using low threshold voltage (V_{TH}) transistors which are superior in drivability and are compatible with digital circuits. The SC circuit cannot be operated under 0.5V with high-V_{TH} devices but on the other hand, SC circuits with low-V_{TH} transistors suffer from charge loss even in analog operations. A 0.5-V sigma-delta modulator with the proposed scheme is successfully manufactured and measured by using 0.15-µm FD-SOI process with 0.1-V V_{THN} transistors.

1. INTRODUCTION

Ubiquitous sensor network applications are getting focus these days, and small, inexpensive, low-voltage, low-power VLSI's become important for this type of applications. In these environments, analog building blocks for sensor modules tend to be embedded in scaled digital circuits as a part of SoC (System-on-a-Chip) implemented with advanced scaled VLSI technology.

Several sub-1V sigma-delta modulators and ADC's have been reported but so far they are implemented in a high-V_{TH} process [1, 2, 3]. In the above-mentioned applications, however, low-V_{TH} transistors compatible with the mainstream scaled digital circuits are to be used. With the low-V_{TH} process, however, subthreshold leakage current is a critical issue even for analog circuits. The use of low-V_{TH} devices even in analog components is important anyway if we think about the future VLSI environments.

In this paper, an issue of the subthreshold leakage current on SC circuits is experimentally clarified, and a subthreshold-leakage suppressed SC circuit utilizing SCCMOS is introduced. The proposed scheme is applied to a 0.5-V sigma-delta modulator. The modulator is experimentally shown to improve the leakage issues. They can be operated with solar cells and are suitable for ubiquitous electronics applications such as sensors for temperature, humidity, and sound data acquisition.

2. DESIGN OF LOW VOLTAGE SC

2.1 An Issue on Conventional SC

The subthreshold leakage has been recognized as a cause of an exploding power issue in digital circuits, and SCCMOS was proposed [4]. On the other hand, since bias current much larger than the subthreshold leakage always flows through typical analog circuits, the subthreshold leakage current won't increase power consumption dramatically for typical analog circuits such as amplifiers. The subthreshold leakage current, however, will be a critical issue in charge storing circuits such as SC circuits and sample & hold circuits. Consequently, leakage current suppression scheme is getting essentially important for the SC-based building blocks in low-V_{TH} SoC environments.

Figure 1 shows a schematic of the conventional SC integrator and the SPICE simulation results. In the conventional SC integrator with 0.1-V V_{TH} MOS switches, the leakage current exceeds 80nA that is over 500 times larger than the case with 0.3-V V_{TH} transistors. This leakage leads to the voltage error of the integrator output of 16mV (8%), which can be considered as a voltage noise and the precision of the analog circuit is severely degraded, which is experimentally verified in Fig. 2.

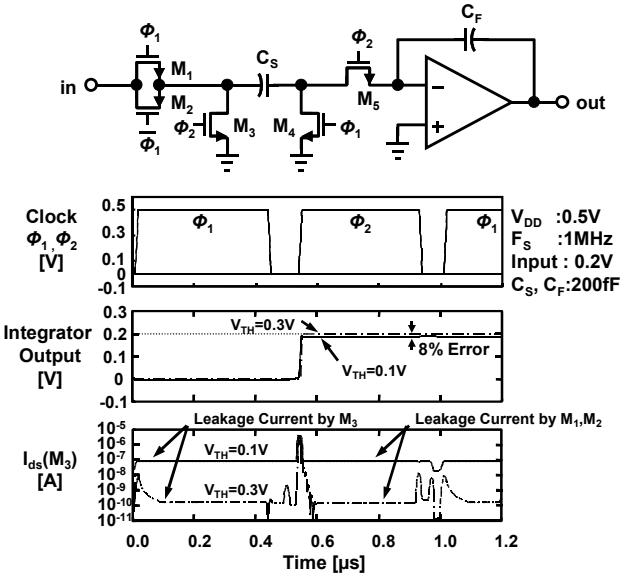

Figure 1. A schematic and SPICE simulation results of the conventional SC integrator.

In Fig. 2, measured leakage current is shown for the conventional SC circuit implemented by a 0.15-µm FD-SOI technology with V_{THP}=-0.2V and V_{THN}=0.1V. The measurement result shows that the voltage error of 8% is introduced by the subthreshold leakage but this percentage error depends on the input voltage, since the leakage current changes non linearly over input and output voltage of the SC circuit. Thus the leakage current does introduce 'non-linear' errors and the non-linear error cannot be compensated nor digitally corrected.

(I_{LEAK} × sampling time)/(C_S × V_{IN}) is a good index of the voltage error induced by the leakage in the SC circuit. This index is also plotted in the figure. The error increases in the lower sampling frequency. One may argue that increasing the sampling frequency can reduce the leakage effects, the power consumption increases at the higher sampling frequency.

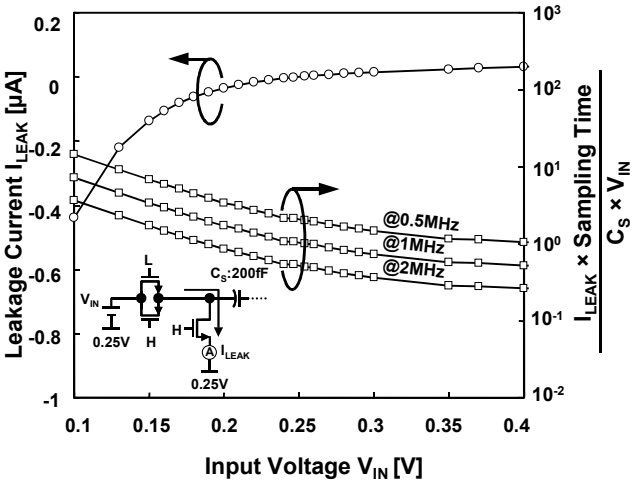

Figure 2. Measured leakage current and plots on calculated charge-error index.

2.2 Proposed Leakage Suppression Scheme

Low-V_{TH} MOS transistor has advantages. First, it is compatible with the mainstream scaled digital circuits. Secondly, it enables low voltage operation. Lastly, it is useful in minimizing the size of MOS switches for the SC since the low-V_{TH} transistor has larger drivability. On the other hand, there is a drawback. That is the large subthreshold leakage. Therefore, it is reasonable to choose low-V_{TH} MOSFET's to build low-voltage, low-cost, small area SC's if there is a subthreshold leakage suppression technique.

A proposed schematic of an SC circuit utilizing SCCMOS scheme for leakage suppression is shown in Fig. 3. In the scheme subthreshold current is significantly suppressed by applying gate voltage below V_{SS} for NMOS's or over V_{DD} for PMOS's) . The input node has triply stacked structure since this node swings between V_{SS} and V_{DD}. The other nodes have doubly stacked structure since they only handle the signal around V_{SS}. Each gate width of stacked switches is twice or three times wider than that of conventional switches to obtain same on-state resistance which limits bandwidth. For example, the gate of M_{3a} is driven by Φ_2 clock that swings between V_{SS} and V_{DD}, and slightly leaky during the off phase of Φ_2. The gate of M_{3b} is driven by Φ_{2l} clock that swings between V_{SSL} and V_{DD} at the same timing of Φ_2. During the off phase of Φ_2, the node between the source of M_{3a} and the drain of M_{3b} is biased at intermediate voltage below the V_{DD}. Hence, M_{3b} is completely cut off without gate-oxide stress.

Although this scheme uses less than V_{SS} and more than V_{DD} voltage, the gate oxide of all the transistors is biased less than V_{DD} for ensuring oxide reliability. Figure 4 shows simulation results of V_{GS}–$|V_{GD}|$ trajectories of the negatively biased switches to show that the oxide is not over-stressed. V_{DD} is 0.5V and V_{SSL} is -0.2V that is equivalent to 0.3-V V_{TH} during the off-state and 0.1-V V_{TH} during the on-state. The GIDL (Gate-Induced Barrier Lowering) effect is not an issue since the V_{TH} is rather low. The $|V_{GD}|$ of negatively biased switch without the stacked structure exceeds 0.5-V V_{DD}. On the other hand, $|V_{GD}|$ of the proposed switch with a stacked structure is always below 0.5-V V_{DD}.

Figure 5 depicts an example of a level shifter which was introduced in [5] and which is applicable to a Φ_1 and Φ_2 generator. V_{DDH} and V_{SSL} can be generated by charge pumping circuit which was introduced in [5]. Again in these clock generation circuits, even though the circuit handles voltages outside the power supply rails, each transistor is free from oxide over-stress.

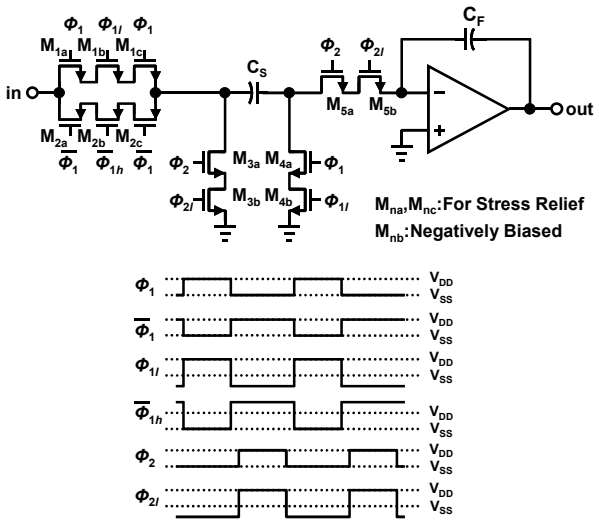

Figure 3. Proposed schematic of SC integrator based on SCCMOS.

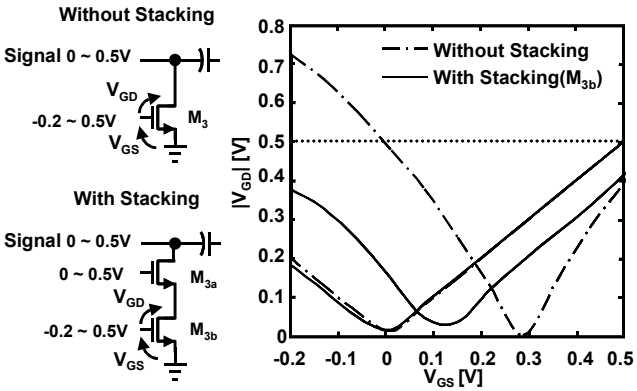

Figure 4. Simulation results of VGS-|VGD| trajectory of negatively biased switches.

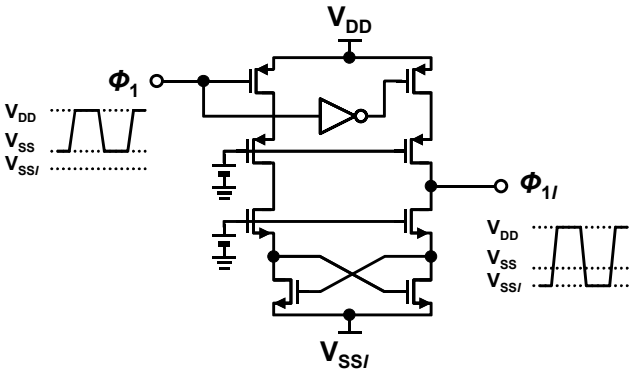

Figure 5. An example of oxide-stress relaxed level shifter applicable to clock generator.

3. EXPERIMENTAL RESULTS

Figure 6 shows a schematic of a 1st-order sigma-delta modulator using the proposed scheme. The proposed and the conventional sigma-delta modulators are implemented in the afore-mentioned 0.15μm FD-SOI technology. The parameters for the modulator and the layout are the same for both of the conventional and proposed circuit except for the SC circuit in order to fairly compare the two SC circuits.

Die micrographs of the proposed and the conventional sigma-delta modulators are shown in Fig. 7 and Fig. 8, respectively, and the area is 130μm×190μm. Since low-V_{TH} MOS can reduce the size of switches, switch array occupies less than 5% of the total area in spite of the increase in the number of MOS switches for proposed scheme. Additional level shifters increase only 3% of the total area.

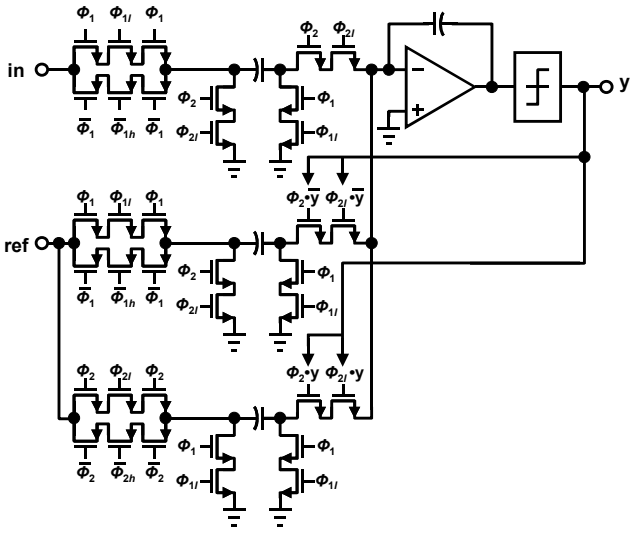

Figure 6. Schematic of 1st-order sigma-delta modulator using proposed scheme.

The circuits are measured with 0.5-V V_{DD} and other conditions are listed in TABLE I. V_{DD}+0.2V and V_{SS}-0.2V are chosen for V_{DDH} and V_{SSL} respectively to cut off switches sufficiently in this experiment. The output bit streams are processed using Matlab.

TABLE I
CONDITIONS FOR MEASUREMENT

Supply Voltage: V_{DD}	0.5V
Negatively biased Voltage: V_{DDH}, V_{SSL}	V_{DD}+0.2V, V_{SS}-0.2V
Sampling Frequency: F_S	2MHz
Band Width: BW	200Hz to 8kHz
Input Signal	1.5kHz

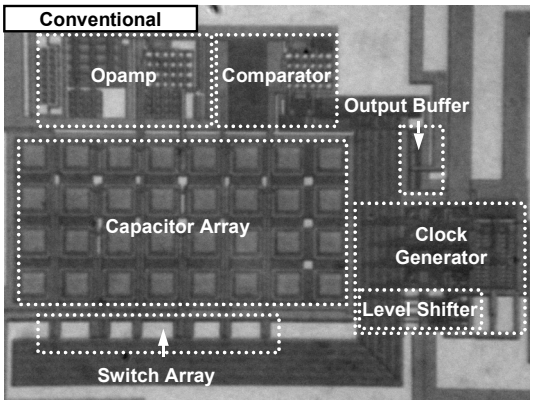

Figure 7. Die micrograph of the conventional sigma-delta modulator. Level shifter for the proposed scheme is implemented but not in use for this conventional modulator.

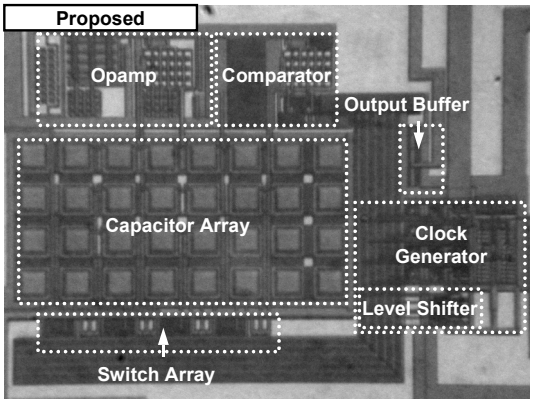

Figure 8. Die micrograph of the proposed sigma-delta modulator. Switch array is implemented in the same area although slightly complicate.

Figure 9 shows measured output power spectrum of the conventional leaky modulator. This spectrum is taken at the input level of –6dB and the large harmonic tones that degrade SNDR are observed. This is due to the leakage current that introduces non-linear errors. On the other hand, the proposed scheme shows the peak SNDR at the input level of –6dB. Although the second-harmonic tone is observed, other higher-order tones are greatly suppressed compared with the conventional circuit as shown in Fig. 10. This can be considered as a result of the suppression of the non-linear noise introduced by the subthreshold leakage.

Measured SNR's and SNDR's are shown in Fig. 11. The conventional scheme achieves the peak SNR of 44dB. The SNDR of the conventional scheme, however, is degraded to 31.5dB. The maximum power consumption of the conventional circuit is 71µW. The proposed scheme achieves the peak SNDR of 33.8dB with the maximum power consumption of 68µW and improves dynamic range over 6dB than the conventional approach.

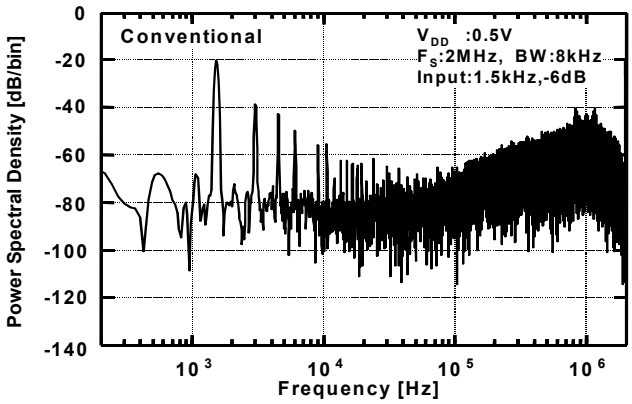

Figure 9. Measured output power spectrum of the conventional modulator. Large harmonic tones that degrade SNDR are observed.

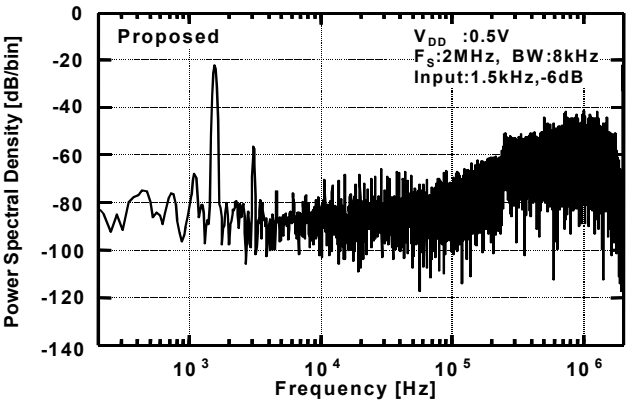

Figure 10. Measured output power spectrum of the proposed modulator. Although the second-harmonic tone is observed, other higher-order tones are suppressed.

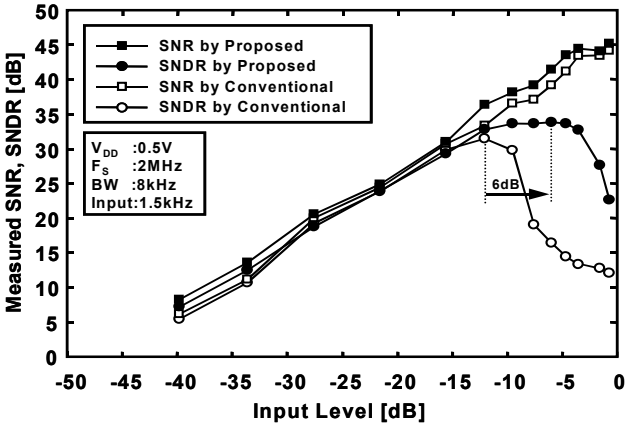

Figure 11. Measured SNR's and SNDR's. The proposed modulator reduces harmonic distortion and greatly improves dynamic range.

4. CONCLUSION

Leakage suppression scheme for switched capacitor circuits based on super-cut-off CMOS is presented. The advantage of the scheme was verified by a 0.5-V sigma-delta modulator implemented in 0.15-µm FD-SOI with 0.1-V V_{THN}. The manufactured sigma-delta modulator suppresses harmonic distortions caused by non-linear leakage-current effects, and improves dynamic range as the result. This scheme suppresses subthreshold-leakage current and realizes analog building blocks with low supply voltage required by ubiquitous sensor network applications.

5. ACKNOWLEDGEMENT

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6. REFERENCES

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