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A Flexible Baseband Processor with Multi-Resolution Spectrum-Sensing Functionality

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Abstract

In this paper, we propose a reconfigurable baseband processor for a cognitive radio that has multi-resolution bandpass filters. By applying the distributed arithmetic algorithm to the reconfigurable baseband processor and rewriting SRAM data in it, a channel center frequency and bandwidth are reconfigurable. The filter bandwidth can be changed from 40 kHz to 240 kHz with a 10 kHz resolution on our prototype processor. The power is 13 mW at a supply voltage of 1.8 V in a 0.18-μm CMOS process.

1. INTRODUCTION

Recently, a wireless communication system like a cellular phone or wireless LAN terminal has been widely spread for comfortable living. With the popularization of the wireless devices, various standards and services have been established and provided; however, it is very inconvenient that a user has many wireless terminals for many wireless services. Thus, a flexible wireless terminal that can adapt to various specifications is increasingly demanded. For a low-cost multi-spectrum wireless terminal, silicon CMOS integrated circuits are suitable; a programmable functionality with analog circuits and/or digital signal processing can be implemented on silicon LSI [1-3].

Fig. 1 (a) shows a block diagram of a general multi-standard low-IF wireless receiver [4]. A signal is down-converted with the mixers and then passes through the low-pass filters. Next, the signal is quantized by the analog-to-digital converters (ADCs). The channel selection is made by digital signal processing in the baseband processor; it can be said that the conventional baseband processor is a kind of channel selection filters for a fixed narrow channel.

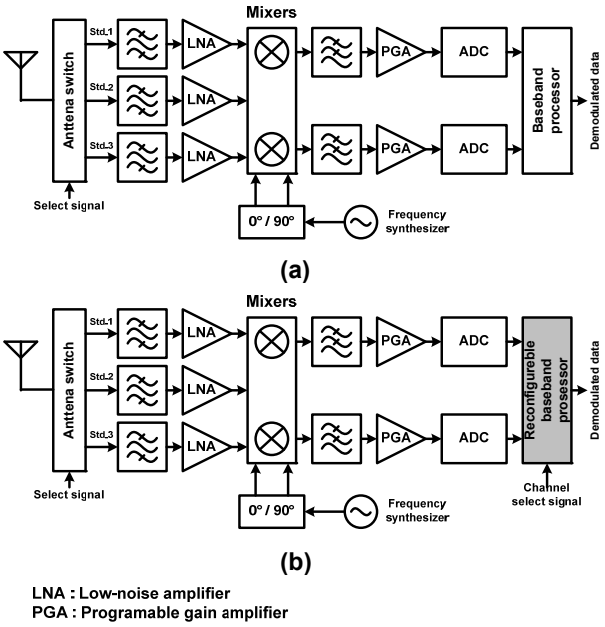

Fig. 1. (a) General multi-standard low-IF wireless receiver and (b) multi-standard receiver with multi-resolution bandpass filter.

In this paper, we describe a baseband processor for a dynamically reconfigurable wireless receiver shown in Fig. 1 (b); the channel selection is made by a reconfigurable filter comprised of delay units, adders, and multipliers. We adopt the distributed arithmetic (DA) algorithm [5] and built-in SRAM for it to reconfigure the filter characteristics (channel center frequency and bandwidth). By rewriting other values in the SRAM, the filter characteristics can be dynamically changed.

2. DISTRIBUTED ARITHMETIC (DA) ALGORITHM

The DA algorithm is for a bit-serial digital filter, and thus high energy efficient [6]. Partial products are stored in the SRAM so that the calculation is carried out only by adders; any multiplier is not needed.

Fig. 2 shows an example of a second-order FIR filter. Now, assume that an input datum is a two's complement, X_k. X_k is expressed as

$$X_k = -b_{kN} + \sum_{n=1}^{N-1} b_{kn} 2^{-(n-N)} , \quad (1)$$

where n is a bit length of one word (n=1…, N), b_{kn} is n-th bit of the two's complement (i.e., 0 or 1): b_{kN} is a sign bit, and b_{k1} is the least significant bit (LSB). Then, an output, Y, is expressed as

$$Y = \sum_{k=1}^{3} A_k X_k$$
$$= \sum_{k=1}^{3} A_k [-b_{kN} + \sum_{n=1}^{N-1} b_{kn} 2^{-(n-N)}] . \quad (2)$$

By reversing the order of the summations, we obtain

$$Y = \sum_{n=1}^{N-1} [\sum_{k=1}^{3} A_k b_{kn}] 2^{-(n-N)} + \sum_{k=1}^{3} A_k (-b_{kN}) , \quad (3)$$

where a partial sum, S_n, is

$$S_n = \sum_{k=1}^{3} A_k b_{kn} . \quad (4)$$

Because A_k is a fixed coefficient and b_{kn} is expressed as 0 or 1, the number of patterns in partial sums is limited to 2^k. This means that, we can prepare the partial sums in advance, and can memorize them in SRAM, as illustrated in Table 1. The input data are used as an address of the SRAM. Consequently, it is possible to directly output the partial sum, S_n, from the SRAM with X_k as the address. By substituting the partial sum, S_n, for (3), the output, Y, can be obtained.

By the way, we can transform (3) as

$$Y = \sum_{m=1}^{N/2} [\sum_{k=1}^{3} A_k b_{k(2m-1)}] 2^{-(2m-1-N)} + \sum_{m=1}^{N/2-1} [\sum_{k=1}^{3} A_k b_{k(2m)}] 2^{-(2m-N)}$$
$$+ \sum_{k=1}^{3} A_k (-b_{kN}) . \quad (5)$$

In this case, we can set an odd partial sum, S_{2m-1}, and even partial sum, S_{2m}, as follows:

$$S_{2m-1} = \sum_{k=1}^{3} A_k b_{k(2m-1)} , \quad (6)$$

$$S_{2m} = \sum_{k=1}^{3} A_k b_{k(2m)} . \quad (7)$$

By reading both the partial sums of the serial two bits from two SRAMs, the clock frequency can be halved. In this paper, we exploit a dual-port SRAM for the dual readouts.

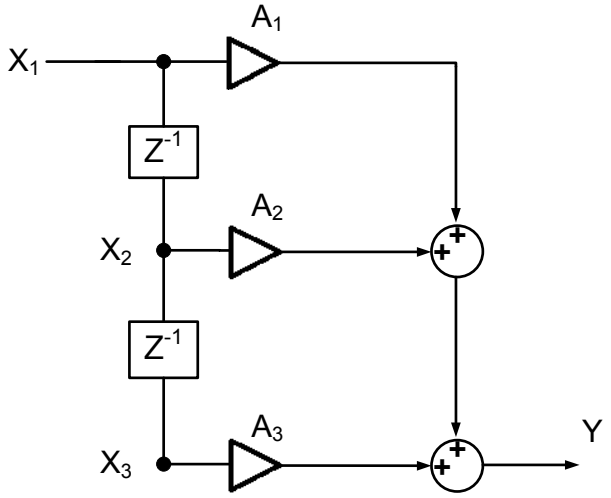

Fig. 2. Second-order FIR filter.

Table 1. Partial sum in SRAM

Address (X_3,X_2,X_1)	Partial sum (S_n)
000	0
001	A_1
010	A_2
011	A_1+A_2
100	A_3
101	A_1+A_3
110	A_2+A_3
111	A_1+A_2+A_3

3. ARCHITECTURE

3.1. Baseband Processor

Fig. 3 shows the block diagram of our baseband processor. In this paper, we treat signals demodulated by frequency shift keying (FSK). So, we need to implement, at least, two band-pass filters (BPFs); the baseband processor is composed by the two BPFs, SRAMs for the DA algorithm, and FSK demodulator. As the multi-resolution BPS, we adopt a fourth-order IIR filter. The signal flow is shown in Fig. 4, where X is a 10-bit input of IIR filter, A_1, A_2, …, A_5 and B_1, B_2, …, B_5 are 16-bit coefficients, t_0, t_1, …, t_4 are 14-bit temporary results stored in registers, and Y is a 15-bit output. X is extended to 14 bits from 10 bits in the calculation to match with the bit length of t_0, t_1, …, t_4. Note that all values are fixed points.

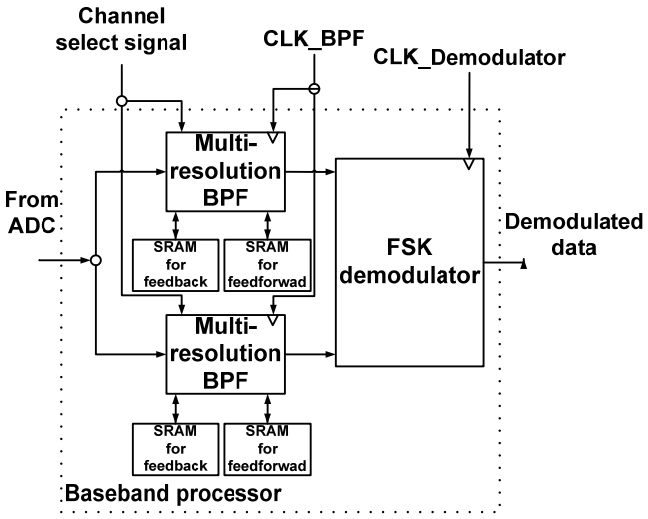

Fig. 3. Block diagram of the proposed baseband processor.

3.2. Implementation of DA Algorithm

As illustrated in Fig. 4, the IIR filter is comprised by a feedback and feed-forward blocks. Implementation of the DA algorithm in each block is achieved by one SRAM. Namely, one multi-resolution BPF requires two SRAMs (see Fig. 3). In the feedback block, the DA algorithm is executed by multiplying X, t_1, …, t_4 by A_1, A_2, …, A_5. On one hand, in the feed-forward block, we use t_0, t_1, …, t_4 and B_1, B_2, …, B_5.

• Feedback block: For executing a subtraction with only adder, in Fig. 4, we memorize partial sums which are obtained by using inverted $A_2,\ldots,A_5$ in SRAM. As the address of the feedback block's SRAM, X, t_1, …, t_4 need to be divided to obtain respective odd and even partial sums, S_{2m-1} and S_{2m} (m=1, …, 7). Note that X is right-shifted by four bits before it is input to the IIR filter because 10-bit X is extended to 14 bits as already mentioned. Odd bits of X, t_1, …, t_4 are for the odd partial sum, and even bits of X, t_1, …, t_4 are for the even partial sum:

$$Addr\_odd\_b = (X[2m-1], t_1[2m-1], \cdots, t_4[2m-1])$$

$$Addr\_even\_b = (X[2m], t_1[2m], \cdots, t_4[2m])$$

• Feed-forward block: As well, for the address of the feed-forward block's SRAM, odd bits of X, t_1, …, t_4 are used to obtain the odd partial sum, and even bits of X, t_1, …, t_4 are used to obtain the odd partial sum:

$$Addr\_odd\_f = (t_0[2m-1], \cdots, t_4[2m-1])$$

$$Addr\_even\_f = (t_0[2m], \cdots, t_4[2m])$$

• Combined address generators: Because t_1, …, t_4 are commonly utilized for both the feedback and feed-forward blocks, the respective address generators becomes compact

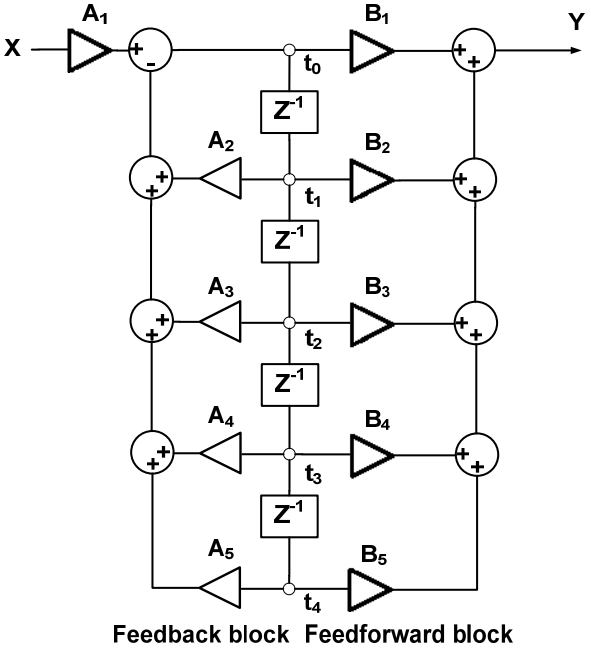

Fig. 4. Fourth-order IIR filter for channel selection.

to calculate the odd and even partial sums. Fig. 5 is the combined address generators.

Fig. 6 illustrates the flow charts of the multi-resolution BPFs for the feedback and feed-forward blocks. The SRAM is a dual-port SRAM, which accepts both the even and odd addressed.

In the feedback block, at first, m is equal to 1; S_1 and S_2 are read from the dual-port SRAM by *Addr_odd_b* and *Addr_even_b*, and then they are stored in registers. The data are added with fixed-point arithmetic; its result is stored to

register. Next, the result is right-shifted by two bits and accumulated.

When m is increased to 2, S_3 and S_4 are read and accumulated in the same way. This procedure is repeated until m becomes seven. From (5), however, we have to invert S_{14}because the most significant bit (MSB) is treated as a sign bit. So, we add a two's complement of S_{14} to the previous result. Finally, we obtain t_0 by pulling out the top 14 bits from the last result.

As well as in the feed-back loops, we make the same calculation with another SRAM.

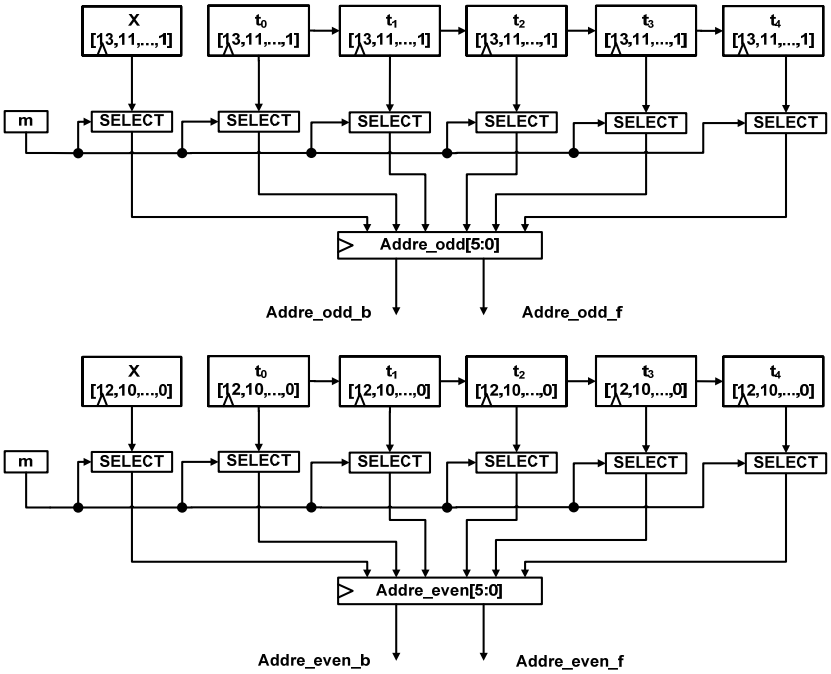

Fig. 5. Address generators for odd and even partial sums.

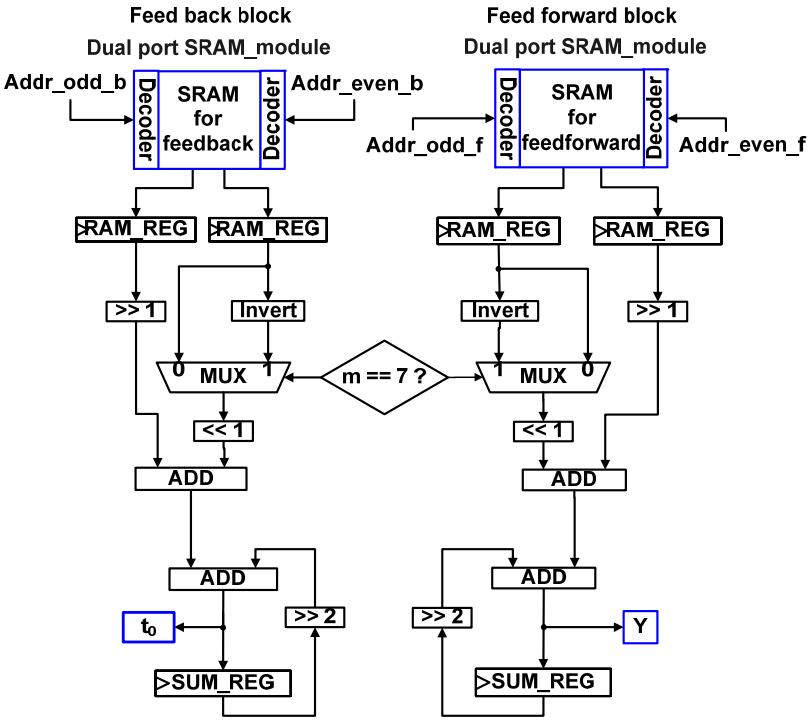

Fig. 6. Flow charts of feedback and feed-forward blocks.

Table. 2. The four filters' coefficients, and their characteristics

	Pattern1	Pattern2	Pattern3	Pattern4
A_1	1.000000000000	1.000000000000	1.000000000000	1.000000000000
A_2	0.000000000000	1.750000000000	0.000000000000	-1.006835937500
A_3	1.863037109375	2.632812500000	1.621582031250	1.305664062500
A_4	0.000000000000	1.640625000000	0.000000000000	-0.656982421875
A_5	0.878906250000	0.878906250000	0.715332031250	0.473876953125
B_1	0.012207031250	0.012695312500	0.047363281250	0.134277343750
B_2	0.000000000000	0.016601562500	0.000000000000	-0.046875000000
B_3	0.010498046875	0.018554687500	0.010986328125	-0.112060546875
B_4	0.000000000000	0.016601562500	0.000000000000	-0.046875000000
B_5	0.012207031250	0.012695312500	0.047363281250	0.134277343750
channel center frequency [kHz]	500	650	500	400
bandwidth [kHz]	40	40	100	240
dynamic range [dB]	40	40	30	25

4. Simulation Results and Design

To verify the reconfigurable filter characteristics, we designed a baseband processor (Fig. 7). First, we simulated four band-pass filters that have different channel center frequencies and bandwidths with MATLAB Filter Design Toolbox. Then, we described the baseband processor circuits including the dual-port SRAMs with Verilog-HDL. Table. 2 summarizes the four filters' coefficients, and their characteristics in Fig. 8. The channel center frequency of Pattern1 is 500 kHz, and that of Pattern2 is 650 kHz; however, both bandwidths are 40 kHz. Meanwhile, the channel center frequency of Pattern1 and Pattern3 are both 500 kHz, but their respective bandwidths are 40 kHz and 100 kHz. Like this, we can reconfigure a channel center frequency and bandwidth by rewriting data in the SRAMs.

The power was also estimated using Synopsys Power Compiler. Table 3 shows the chip area and power including an FSK demodulator. The function of the FSK demodulator is to demodulate FSK-modulated signals with a counting method.

When a clock frequency is 16 MHz and a supply voltage is 1.8 V, the power is 13.5 mW on a whole baseband processor in a 0.18-um process. As compared in Table 4, the power is less than 8% of [7], while achieving the dynamic range improvement of 10 dB.

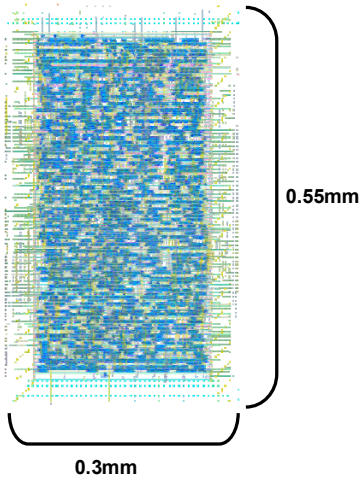

Fig. 7. Layout plot image of baseband processor.

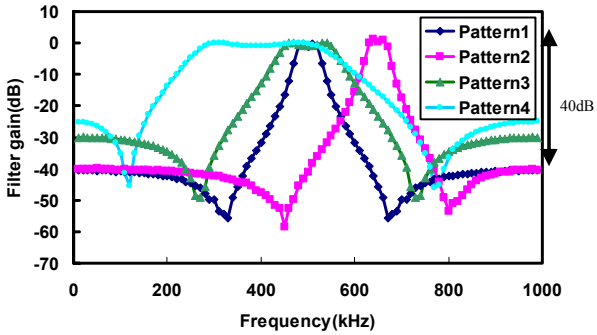

Fig. 8. Filter characteristics.

Table 3. Chip area and power.

Units		Area (um^2)	Power (mW)
Channel selection filter	logic	48891	0.45834
	SRAM	376136	13
FSK-demodulator		8303	0.00977
Total		433331	13.46811

Table 4. Comparison with other reconfigurable architecture [7].

	dynamic range [dB]	power [mW]	Area [um^2]	Max clock frequency [MHz]
Our channel selection filter	**40**	**13**	**433331**	**16**
[7]	**30**	**180**	**-**	**38.4**

5. CONCLUSION

In this paper, we proposed a reconfigurable multi-resolution BPF using the distributed arithmetic algorithm. By rewriting data in SRAMs, filter characteristics can be changed. The total power is 13.5 mW in a 0.18-um process, and it is less than 8% of the conventional scheme, although the dynamic range is improved by 10 dB.

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