Low-Power CMOS Design through V_{TH} Control and Low-Swing Circuits

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Abstract

This paper describes some of the circuit level techniques for low-power CMOS designs. V_{TH} control circuits are necessary for achieving low-threshold voltage in high-speed low-voltage applications. As for the low-swing circuit techniques, applications to a clock system, logic part, and I/O's are discussed.

1. Introduction

CMOS power dissipation and delay are given by[1,2]

$$\text{Power} = p_t \cdot C_L \cdot V_S \cdot V_{DD} \cdot f_{CLK} + I_0 \cdot 10^{\frac{V_{TH}}{S}} \cdot V_{DD} . \quad (1)$$

The first term, in (1) represents dynamic power dissipation due to charging and discharging of the load capacitance, where p_t is the switching probability, C_L is the load capacitance, V_S is the voltage swing of a signal, and f_{CLK} is the clock frequency. The second term is the subthreshold leak term and S is typically about 100mV/decade.

Figure 1 shows the plot for power and delay assuming 0.5μm design rule. As seen from the figure, lowering V_{DD} is effective in decreasing power but delay increases. Fig.1(b) shows equi-delay curves and the delay can be maintained if the V_{TH} is lowered as V_{DD} is reduced. Lowering V_{TH}, however, increases subthreshold leakage. In order to cope with this problem, V_{TH} control schemes have been proposed which are covered in Section 2.

In most cases, V_S in (1) is the same as V_{DD}, but in low-swing circuits V_S is smaller than V_{DD}. As seen from Eq.(1), reducing V_S can be one promising way to decrease power consumption. As for the low-swing circuit techniques, applications to a clock system, logic part, and I/O's are discussed in Section 3, 4, and 5, respectively

2. V_{TH} control techniques

To maintain throughput while lowering supply voltage to decrease power consumption, it is effective to lower the threshold voltage of MOSFET's. There are, however, issues associated with low V_{TH} in low V_{DD} environments.

First, delay fluctuates intolerably with V_{TH} fluctuation in low V_{DD} regime. For example, delay increase by 3 times for ΔV_{TH} = +0.15V at V_{DD} of 1V. The second issue is the subthreshold leakage increase. The leakage increases by 10 times for every ΔV_{TH} of - 0.1V. The third problem is the inability for I_{DDQ} test. I_{DDQ} test is necessary to screen out LSI's with defects and micro-shorts which develop to a failure in a long run.

In order to cope with these issues, V_{TH} control techniques have been proposed which are summarized in TABLE 1. Multi-Threshold V_{TH} CMOS[3,4], MTCMOS in short, tries to decrease the subthreshold leak in standby mode by inserting high V_{TH} MOSFET in series to normal circuitry. The high-V_{TH} device is turned off in standby mode and completely cut-off the leakage path. The drawback is the large inserted MOSFET which increases area and delay.

While the MTCMOS can solve only the standby leakage problem, the Variable Threshold CMOS[5-9] (VT CMOS) can solve all the three problems. It dynamically varies V_{TH} through substrate-bias, V_{BB}. Typically, V_{BB} is controlled so as to compensate V_{TH} fluctuations in the active mode, while in the standby mode and in the I_{DDQ} testing, deep V_{BB} is applied to increase V_{TH} and cut off the subthreshold leakage current. The idea to control the V_{BB} so as to minimize the subthreshold leakage under the condition that a representative circuit shows sufficient speed was also proposed (Frequency adaptive Threshold CMOS, FTCMOS[10]).

The Elastic V_{TH} CMOS[11], EVTCMOS in short, controls both V_{DD} and V_{BB} such that when V_{DD} is lowered VBB becomes that much deeper to raise V_{TH} and further reduce power dissipation. Note that internal V_{DD} and VSS are provided by source-follower n- and p- transistors, respectively, whose gate voltages are controlled. In order to control the internal power supply voltage independent from the power current, the source-follower transistors should operate near the threshold. This requires very large transistors.

In VTCMOS, it has been experimentally evaluated that the number of substrate (well) contacts can be greatly reduced in low voltage environments [7-9]. Using a phase-locked loop and an SRAM in a VTCMOS gate-array [8], the substrate noise influence has been shown to be negligible even with 1/400 of the contact frequency compared with the conventional gate-array. A DCT (Discrete Cosine Transform) macro made with the VTCMOS [7] has also been manufactured with substrate- and well- contacts only at the periphery of the macro and it worked without problems realizing more than one order of magnitude smaller power dissipation than a DCT macro in the conventional CMOS design.

3. Low-swing circuit for clock system

The four pie charts in Fig.2 shows power distribution in VLSI's. As seen from the charts, the power distribution of VLSI's differs from product to product. However, it is interesting to note that a clock system and a logic part itself consume almost the same power in various chips, and the clock system consumes 20% to 45% of the total chip power. One of the reasons for this large power consumption of the clock system is that the transition ratio of the clock net is

one while that of the ordinary logic is about one third on average.

In order to reduce the clock system power, it is effective to reduce a clock voltage swing. Such idea is embodied in the Reduced Clock Swing Flip-Flop (RCSFF)[12]. Figure 3 shows circuit diagrams of the RCSFF. The RCSFF is composed of a current-latch sense amplifier and cross-coupled NAND gates which act as a slave latch. This type of flip-flop was first introduced in 1994[14] and extensively used in a microprocessor design[13]. The sense-amplifying F/F is often used with low-swing circuits because there is no DC leakage path even if the input is not full swing being different from the conventional gates or F/F's.

The salient feature of the RCSFF is to accept a reduced voltage swing clock. The voltage swing, Vclk, can be as low as 1V. When a clock driver Type A in Fig. 4 is used, power improvement is proportional to $Vclk^1$, while it is $Vclk^2$ if Type B driver is used. Type A is easy to implement but less efficient. Type B needs either an external Vclk supply or a DC-DC converter.

The issue of the RCSFF is that when a clock is high to Vclk, P1 and P2 do not switch off completely, leaving leak current flowing through either P1 or P2. The power consumption by this leak current turns out to be permissible for some cases (see next section), but further power improvement is possible by reducing the leak current. One way is to apply backgate bias to P1 and P2 and increase the threshold voltage. The other way is to increase the V_{TH} of P1 and P2 by ion-implant, which needs process modification and is usually prohibitive. When the clock is to be stopped, it should be stopped at V_{SS}. Then there is no leak current.

A. Area & Speed

The area of the RCSFF is about 20% smaller than the conventional F/F as seen from Fig. 5 even when the well for the precharge PMOS is separated.

As for delay, SPICE analysis is carried out assuming typical parameters of a generic 0.5μm double metal CMOS process. The delay depends on Wclk (Wclk is defined in Fig.3). Since delay improvement is saturated at Wclk = 10μm, this value of Wclk is used in the area and power estimation. Clock-to-Q delay is improved by a factor of 20% over the conventional F/F even when Vclk = 2.2V, which can be easily realized by a clock driver of the Type A1. Data setup time and hold time in reference to clock are 0.04ns and 0ns , respectively being independent from Vclk, compared to 0.1ns and 0ns for the conventional F/F.

B. Power

The power in the Fig.6 includes clock system power per F/F and the power of a F/F itself. The power consumption is reduced to about 1/2~1/3 compared to the conventional F/F depending on the type of the clock driver and V_{WELL}. In the best case studied here, 63% power reduction is observed. TABLE 2 summarizes typical performance improvement.

C. Application to reduced swing bus

For the RCSFF, the D and $\bar{D}$ input can also be small voltage swing signals. Using this characteristics, the RCSFF can be used to speed up RC delay of long buses. By placing the RCSFF at the end of a long bus and by sense-amplifying the slowly changing D input, RC delay can be reduced to 1/3 compared to the conventional F/F case (see Fig.7).

Let us consider what amount of power gain is observed when a distributed RC line is driven in full swing[15] at one end and switched off when the other terminal becomes V_2.

$$\frac{V(x,t)}{V_{DD}} = 1 + \frac{2}{\pi}\sum_{k=1}^{\infty}\frac{(-1)^k}{k-\frac{1}{2}}\cos\left\{\left(k-\frac{1}{2}\right)\pi\left(1-\frac{x}{L}\right)\right\}e^{-\left(k-\frac{1}{2}\right)^2\pi^2\frac{t}{RC}}$$

$$Q = \int_0^L cv(x,t)\,dx = CV_{DD}\left\{1-\frac{2}{\pi}\sum_{k=1}^{\infty}\frac{1}{\left(k-\frac{1}{2}\right)^2\pi^2}e^{-\left(k-\frac{1}{2}\right)^2\pi^2\frac{t}{RC}}\right\}$$

If the energy per cycle, E (=QV_{DD}), is expressed in terms of the terminal voltage, V_2 (=V(L,t)), E≈0.36+0.64V_2. This means that about 50% power saving is possible if an RC interconnect is driven when the voltage swing of V_2 is $0.2V_{DD}$.

4. Low-swing circuit for logic

A pass transistor logic is known to provide a low-power design style. An attempt has been made to further reduce the power•delay product by reducing the signal voltage swing. A Sense-Amplifying Pass-transistor Logic (SAPL) [14] is such a circuit. In the SAPL, a reduced output signal of NMOS pass-transistor logic is amplified by a current latch sense-amplifier to gain speed and save power dissipation as shown in Fig. 9 and Fig.10. The SAPL has been applied to a 1.5ns 20bit carry skip adder in a Discrete Cosine Transform (DCT) macro whose circuit diagram is shown in Fig. 11. 50% speed, 30% area, and 50% power advantage were observed compared with the conventional static CMOS design.

The SAPL is also applied to a 0.9ns 64bit to 32bit double barrel shifter. In this case, 100% speed, 50% area, and 50% power advantage were observed. The MPEG2 decoder LSI which utilizes the DCT and VLD macro with SAPL operates under 0.9V supply voltage.

5. Low-swing circuit for I/O

Application of low-swing circuit to I/O's is also possible. The circuit diagram is shown in Fig.14. The transmitted signal is differential and again is received by a current-latch type sense-amplifier F/F. The two chips are put side by side and bonded directly with minimum capacitance and inductance. The photos of the system are shown in Figs.15 and 16.

At the frequency of 500MHz, the power consumption is 13mW per bonding which includes output and input power (see Fig. 17).

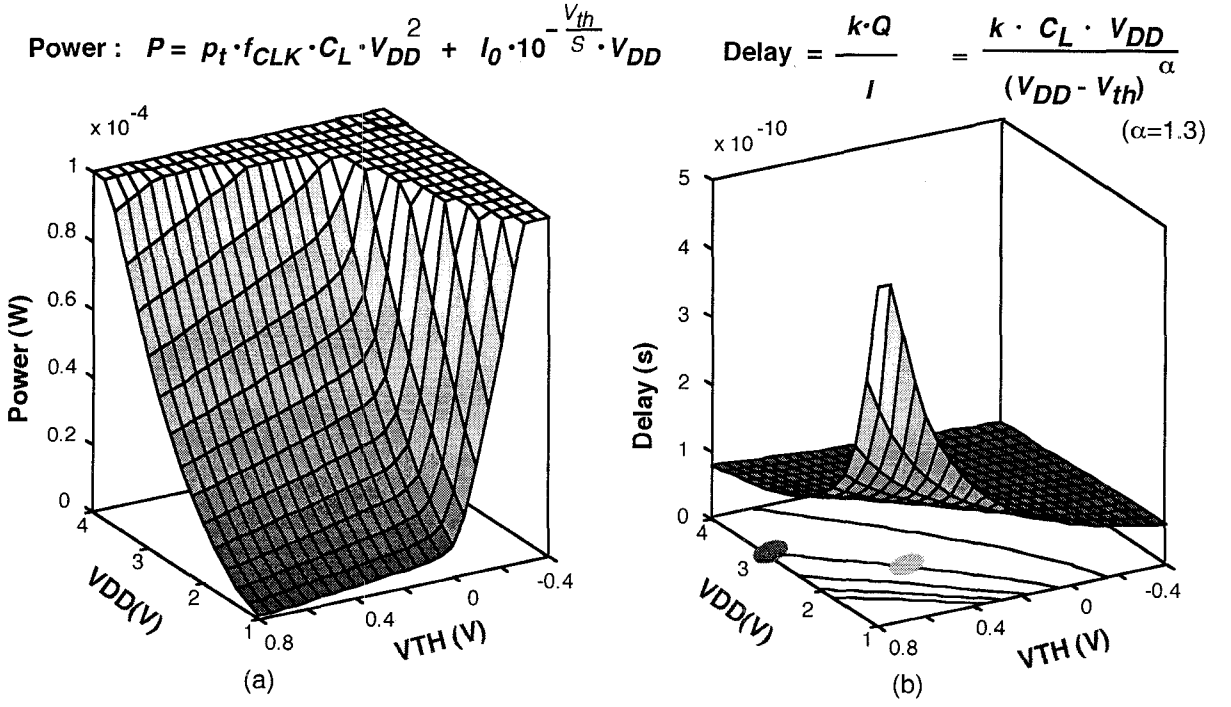


Fig.1 Dependence of (a) power and (b) delay on the supply voltage, V_{DD} and the threshold voltage, V_{TH}.

TABLE 1 Comparison of various V_{TH} control techniques

	MTCMOS	VTCMOS	EVTCMOS
Scheme	St'by *High-Vth V_{DD} V_{DD}' Low-Vth V_{SS} Ref.[3,4]	n-well St'by control (SSB) V_{DD} V_{SS} p-well Ref.[5-9]	St'by control (DLL) * V_{DD} V_{DD}' * V_{SS}' V_{SS} Ref.[11]
	V_{DD} on-off	V_{BB} control	V_{DD}&V_{BB} control
Effect	+ $I_{st'by}$ reduction	+ ΔV_{th} compensation + $I_{st'by}$ reduction + I_{DDQ} test	+ ΔV_{th} compensation + $I_{st'by}$ reduction + I_{DDQ} test
Penalty	- large serial MOSFET(*) slower,larger,lower yield - special latch	- triple well (desirable)	- large serial MOSFET operating near threshold(*)

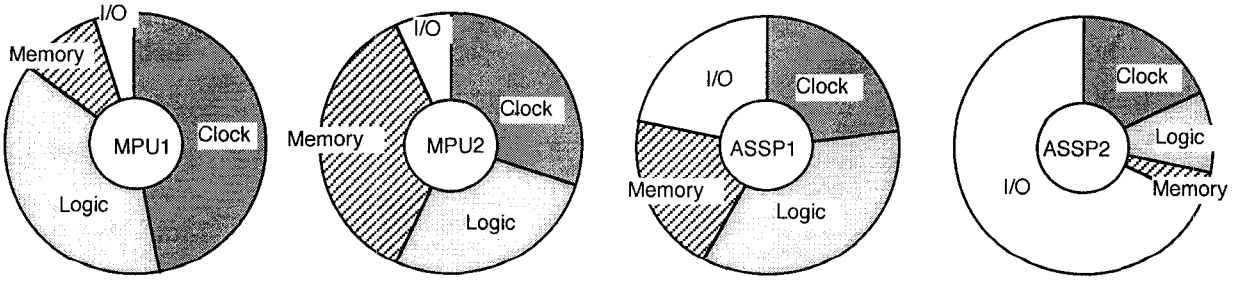
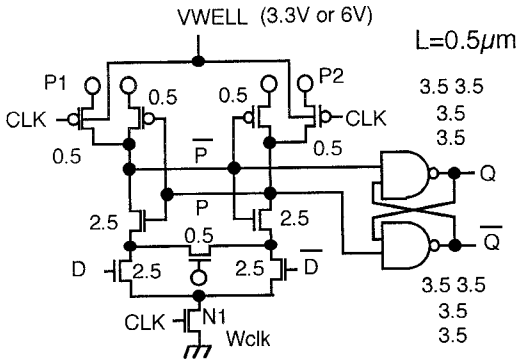
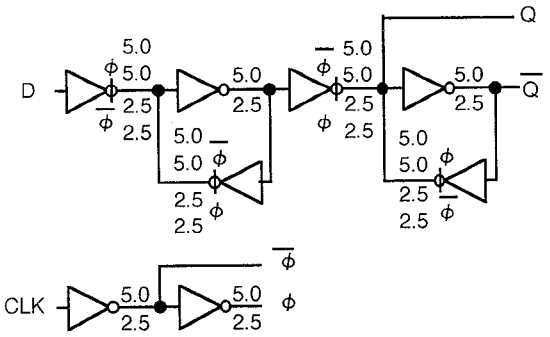


Fig. 2 Power distribution in VLSI's. MPU1 is a low-end microprocessor for embedded use, MPU2 is a high-end CPU with large amount of cache, ASSP1 is a MPEG2 decoder and ASSP2 is an ATM switch.

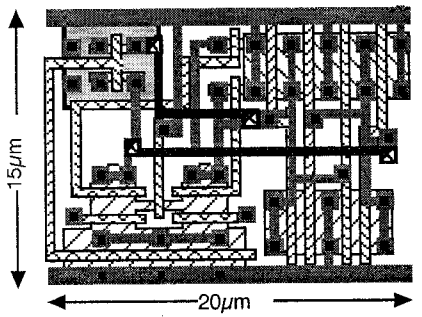


(a) RCSFF. Voltage swing of CLK is reduced toVclk

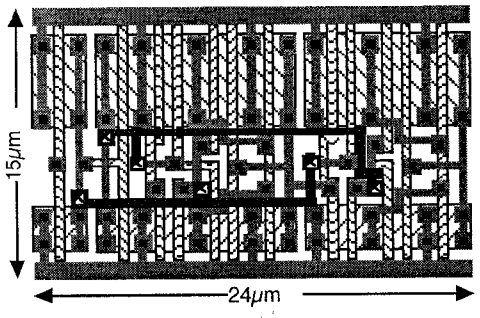


(b) Conventional F/F

Fig. 3 Circuit diagram of (a) the Reduced Clock Swing Flip-Flop (RCSFF) and (b) the conventional F/F. Numbers in the figure signify MOSFET gate width. Wclk is the gate width of N1



(a) RCSFF (N-well for P1 & P2 separated)



(b) Conventional F/F

Fig. 5 Layout of (a) the Reduced Clock Swing Flip-Flop (RCSFF) with Wclk being 10μm and (b) the conventional F/F.

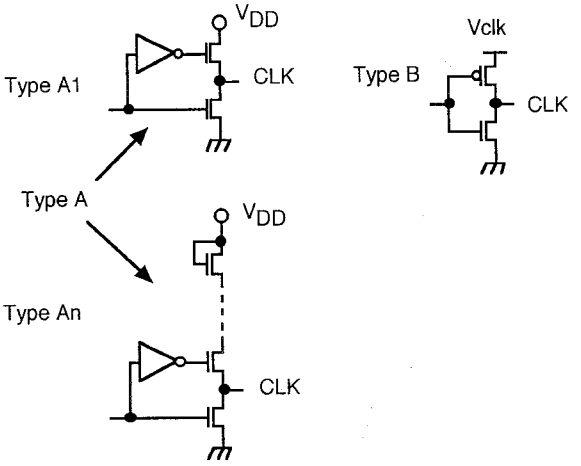


Fig. 4 Types of clock drivers. Type A1 and Type An are grouped as Type A. In Type B, Vclk is supplied by externally.

TABLE 2 Performance comparison of RCSFF and Conventional F/F

	Driver	Vclk[V]	Power	Delay	Area
Conventional		3.3	100%	100%	100%
RCSFF	Type A1	2.2	59%	82%	83%
V_{well} =6.6V	Type A2	1.3	48%	123%	83%
W_{clk} =10μm	Type B	2.2	48%	82%	83%
f clk =100MHz	Type B	1.3	37%	123%	83%

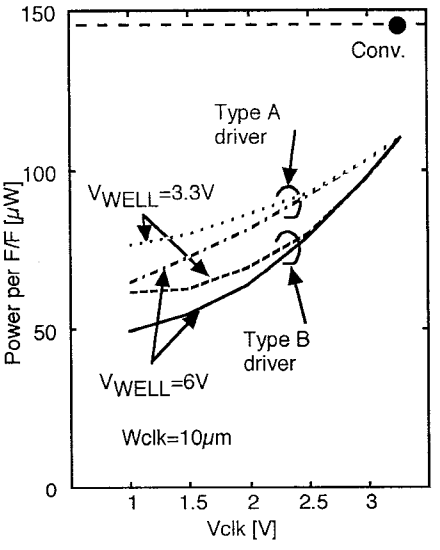


Fig 6. Power consumption for one F/F. Clock interconnection length per one F/F is assumed to be 200μm and data activation ratio is assumed to be 30%. $f$clk is 100MHz. By applying 6V well bias, the initial Vth of P1 and P2 (0.6V) increases to 1.4V.

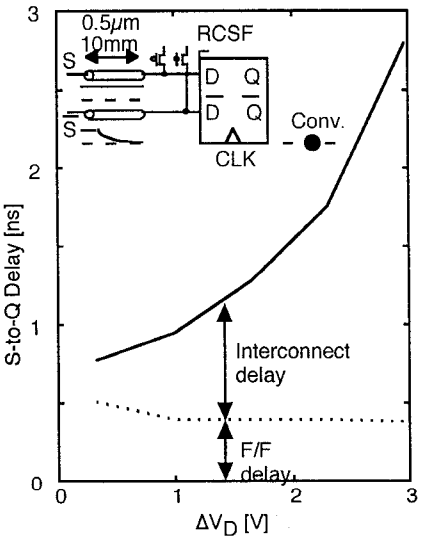


Fig. 7 Delay improvement of a long RC bus by RCSFF. Wclk=10μm and Type A1 clock driver is used. Bus is differential and precharged to VDD first and then CLK is asserted when the voltage difference of D and D becomes ΔVD.

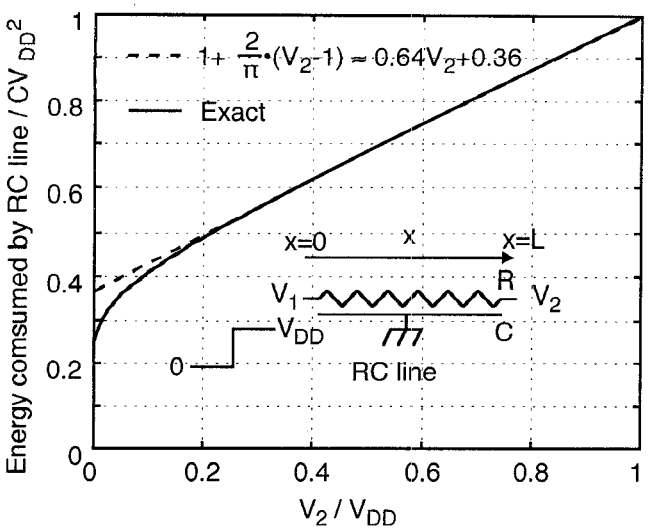


Fig.8 Energy consumed by RC interconnect if the voltage swing of V2 is reduced.

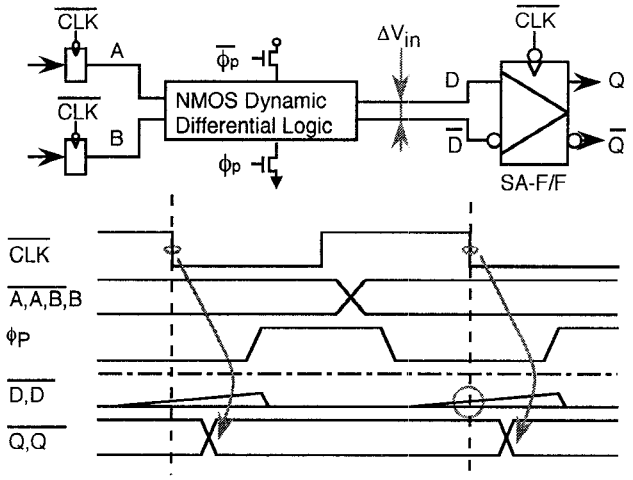


Fig.10 Timing chart of SAPL

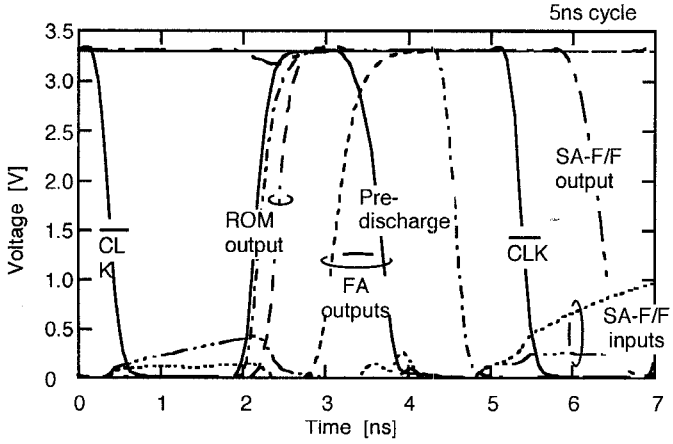


Fig.12 Waveforms for SAPL adder of Fig. 11

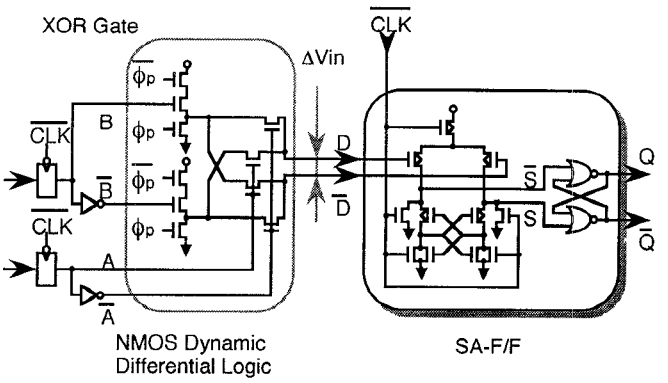


Fig.9 Sense-Amplifying Pass-Transistor (SAPL) logic concept.. The reduced swing signal is amplified by sense-amplifying flip-flop.

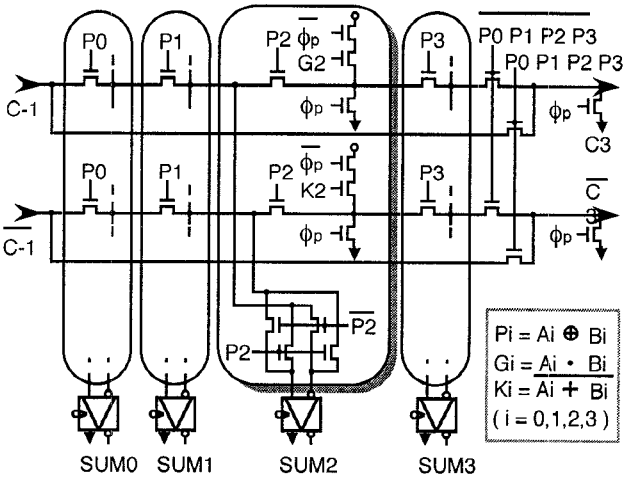


Fig.11 Sense-Amplifying Pass-Transistor (SAPL) applied to 20bit skip-carry adder. The adder was used in a Descrete Cosine Transform macro in a MPEG2 decoder chip which worked under 0.9V.

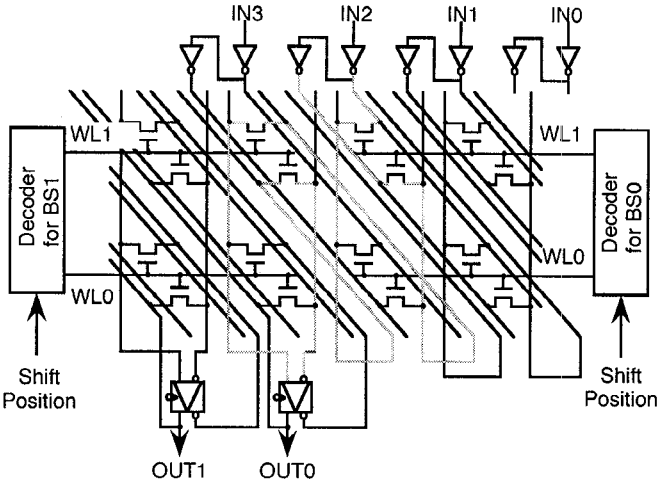


Fig.13 Sense-Amplifying Pass-Transistor (SAPL) applied to a 32bit barrel shifter. The shifter was used in a Variable Length Decoder macro in a MPEG2 decoder chip which worked under 0.9V.

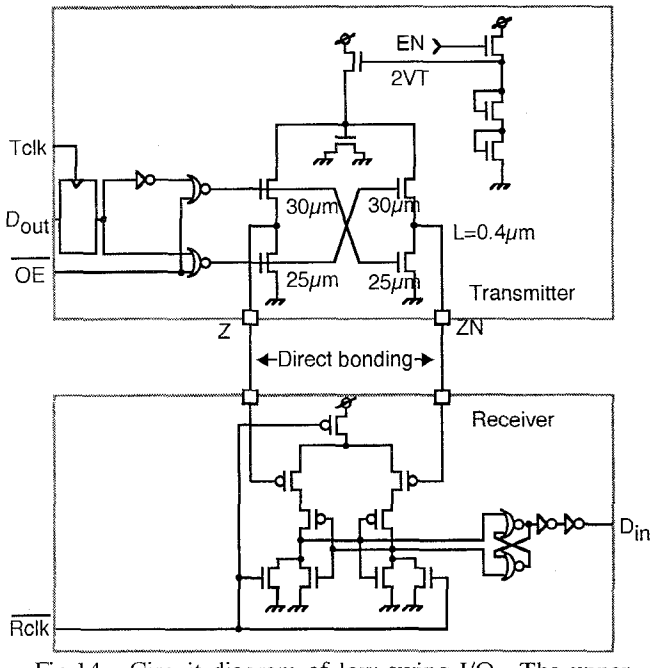


Fig.14 Circuit diagram of low-swing I/O. The upper half is a transmitter side and the lower half is a receiver side.

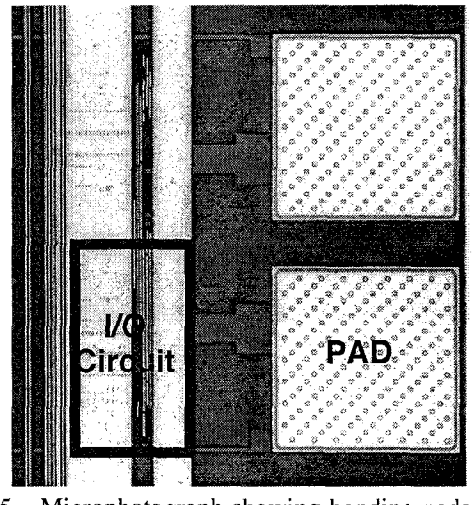


Fig.15 Microphotograph showing bonding pads and I/O circuits (mostly under Al lines). The I/O circuit includes input and output circuit and is smaller than a pad.

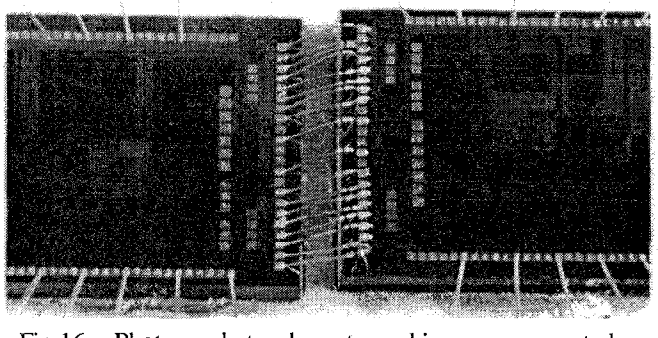


Fig.16 Photograph to show two chips are connected by bonding wires directly.

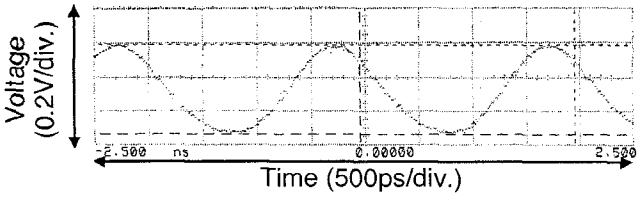


Fig.17 Measured waveform on the bonding pads. The frequency is 500MHz.

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