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Quality of a Bit (QoB): A New Concept in Dependable SRAM

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Abstract

We propose a novel dependable SRAM with 7T memory cells, and introduce a new concept, "quality of a bit (QoB)" for it. The proposed SRAM has three modes: a typical mode, high-speed mode, and dependable mode, in which the QoB is scalable. That is, the area, speed, reliability, and/or power of one-bit information can be controlled. In the typical mode, assignment of information is as usual as one memory cell has one bit. On the other hand, in the high-speed or dependable mode, one-bit information is stored in two memory cells, which boosts the speed or increases the reliability. By carrying out Monte Carlo simulation of dynamic cell stability in a 90-nm process technology, we confirmed the advantage of the proposed SRAM.

1. Introduction

These days, they have paid attention to dependable computing systems, as silicon LSIs support massive infrastructure in society. However, the advanced process technology tends to cause accidental errors like a soft error and negative bias temperature instability (NBTI), more frequently. In addition, there might be some errors left in a design, manufacturing, or test phase. It is supposed to be almost impossible to perfectly eliminate these human-induced errors in a future complicated LSI. That is, a product will be shipped with some errors, and accidentally malfunction. We no longer expect error-free LSIs with sufficient operating margins.

Since reliability is varied with operating conditions (speed, supply voltage, temperature, and even altitude corresponding to a soft error), it is desirable to dynamically improve the reliability on worse conditions. In addition, required reliability depends on an application software, which indicates that the reliability should be changed in accordance with the application.

Considering this background, we propose an SRAM that can dynamically control its reliability. An SRAM has recently dominated operating margins of a chip due to a large number of transistors [1-6]. Other than the reliability, the proposed SRAM also achieves fast operation and/or low-power operation, with the same reliability kept as the conventional SRAM. Namely, the proposed SRAM can change quality of its information, in terms of reliability, speed, and/or power.

In the next section, we mention the overview of the proposed SRAM. In Section 3, we propose a novel 7T memory cells to dynamically improve the quality of information, and introduce a new concept called "quality of a bit" (QoB). In Section 4, we discuss the reliability of the proposed memory cell, from a viewpoint of a bit error rate. The final section summarizes this paper.

2. Dependable SRAM: overview

Operating conditions affect reliability of an SRAM, while the reliability depends on an application software that uses the SRAM. An encryption program and a screen saver program demand different levels of reliability. This means that the reliability is changed by the operating conditions, and is dependent on the application. In our proposed SRAM, the reliability of an SRAM can be dynamically changed on a block-by-block basis, as illustrated in Figure 1. In the typical-dependability blocks (Blocks 0–3), assignment is as usual as one memory cell has one bit. On the other hand, in the high-dependability blocks (Blocks 4–5), one-bit information is stored in two memory cells by combining a pair of memory cells. This mechanism realizes the high dependability, while the memory capacity becomes a half in the high-dependability blocks.

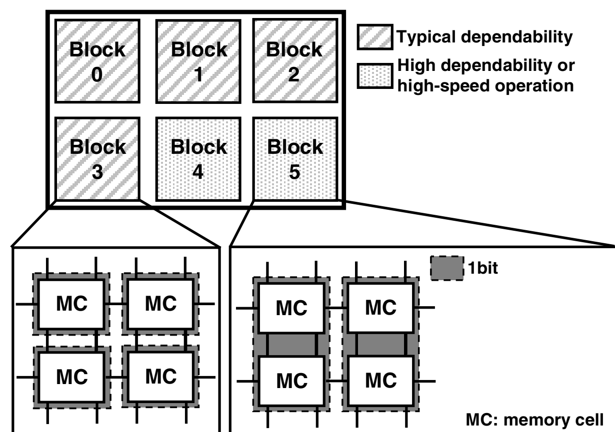

Figure 1. A dependable SRAM.

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However, this dynamic switching between the typical dependability and high dependability opens up new resource allocation in an SRAM. For instance, an operating system (OS) can allocate an encryption program to the high-dependability block. An application software can also change the reliability of its data by a system call. Encryption data or personal information should be in the high-dependability block. If memory utilization of programs and data is 50% or less, the high-dependability mode can be aggressively exploited by the OS, without the memory-capacity overhead. A small code with small data always runs in the high-dependability mode.

In the next section, we explain how to achieve the proposed dependable SRAM on the circuit level.

3. Dependable memory cell and the concept of the quality of a bit (QoB)

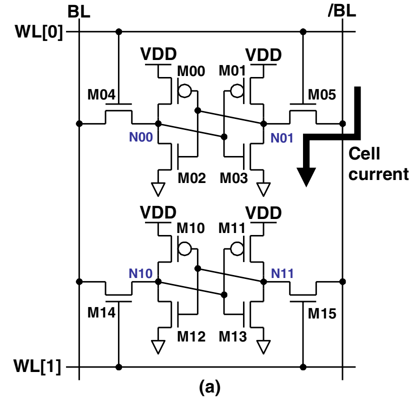
3.1. Conventional 6T memory cell

Figure 2 is a pair of the conventional 6T memory cells. Usually, only one memory cell (MC) is accessed (for instance, WL[0] = “H”, WL[1] = “L”) in write and read operations. We call this conventional scheme “a 1-MC mode”.

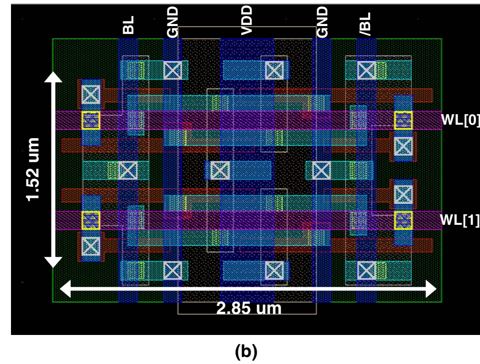
As well, we can set both WL[0] and WL[1] to “H” at the same time, in which case, we can write a same datum to the two memory cells (2-MC mode). After that, a larger cell current can be obtained in read operation by enabling the two wordlines. This means that we can trade off the speed against the cell area.

Figure 3 shows the advantages of the 2-MC mode in the conventional 6T memory cell. The cell current in the 2-MC mode is increased by 142%. Statistically, it is very unlikely that a pair of memory cell is both the worst case. This is the reason why the cell current is more than double. In other words, a local variation (random variation) is suppressed by combining a pair of memory cells. The 2-MC mode achieves a faster access time in read operation.

Another merit in the 2-MC mode is a self-recovery effect. In the 1-MC mode, if a memory cell has a large variation and is not marginal (bad cell), datum stored in it is sometimes flipped in read operation [4]. On the other hand, in the 2-MC mode, the datum in the bad cell is recovered by another good cell in a pair. Figure 3 (b) illustrates the self-recovery effect in the 2-MC mode. Even if the bad cell is not marginal and is once flipped, the storage data is sustained after all, and can be properly read out. The operating margin is determined by the good cell in the pair.

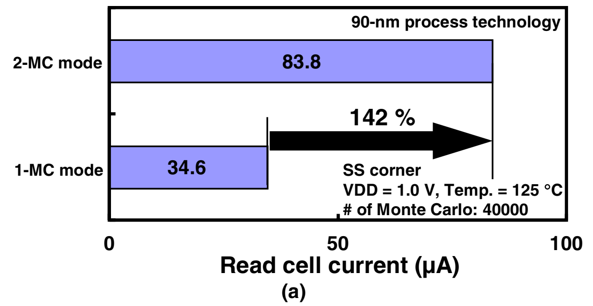


(a)

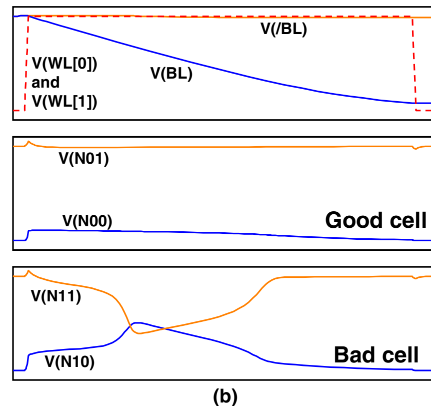


(b)

Figure 2. A pair of the conventional 6T memory cells. (a) Schematic and (b) layout.



(a)



(b)

Figure 3. (a) Worst-case cell current and (b) self-recovery effect in the 2-MC mode.

However, please note that the self recovery takes long time in the conventional 6T memory cell, because the internal nodes in the bad cell are slowly recovered by the good cell through the two access transistors and bitline. After the voltage difference opens significantly between the differential bitlines, the self recovery takes place. This infers that the cycle time becomes slow for the proper operation, even if the access time is high speed. In the next subsection, we proposed a novel memory cell, in which the internal nodes are directly connected with additional transistors.

3.2. Dependable 7T memory cell

Figure 4 is the proposed 7T memory cells. Two nMOSes connect the internal nodes in the pair of memory cells ("N00 and N10", "N01 and N11"). As well, pMOSes can be utilized instead, as shown in Figure 5. Compared with the conventional 6T memory cell, the respective area overheads are 30% and 12%, in the nMOS and pMOS additional cases. Another option is a transmission gate (nMOS + pMOS) for the connecting switch, although we do not take it for the design choice. A transmission gate results in a significantly larger area overhead.

3.2.1. Typical mode

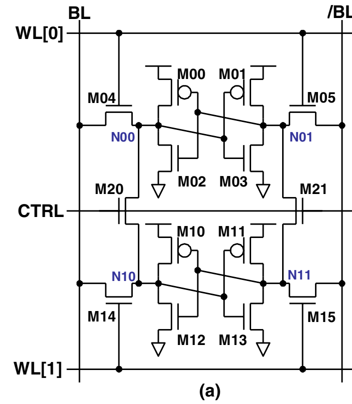
If the additional transistors are not activated (CTRL = "L" or /CTRL = "H"), the proposed 7T memory cell acts as the conventional 6T memory cell. This is called "a typical mode" in this paper.

3.2.2. High-speed mode

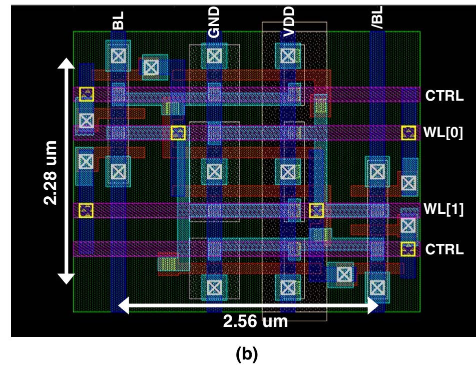
Alternatively, if the additional transistors are asserted, the internal nodes are shared by the pair of memory cells. The high speed is achieved when both WL[0] and WL[1] are on. The access time is as same as the 2-MC mode in the conventional 6T memory cell, but the cycle time is much faster because a marginal cell in a pair prevents another bad cell from being flipped.

3.2.3. Dependable mode

The most significant usage of the proposed 7T memory cell is the dependable mode. The additional transistors are activated (CTRL = "H" or /CTRL = "L"), but either WL[0] or WL[1] is asserted. Thus, only one wordline is asserted. By doing so, a sufficient β ratio and read margin can be obtained because the dependable mode has two access transistor but four drive transistors in a memory cell.

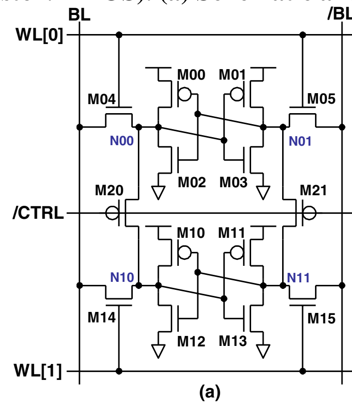


(a)

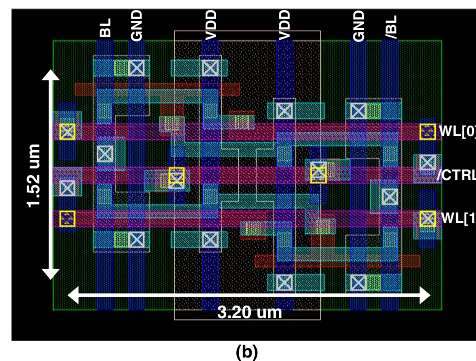


(b)

Figure 4. Dependable 7T memory cells (additional transistor: nMOS). (a) Schematic and (b) layout.



(a)



(b)

Figure 5. Dependable 7T memory cells (additional transistor: pMOS). (a) Schematic and (b) layout.

3.3. Quality of a bit (QoB)

As mentioned above, we have three modes in the proposed 7T memory cell. Table I summarizes the modes. In the typical mode, one-bit datum is stored in one memory cell, which is the most area-efficient. In the high-speed mode and dependable mode, one-bit datum is stored in two memory cells although the quality of the information is different from the typical mode. The “higher-speed” or “more dependable” information can be obtained. We call this concept “quality of a bit (QoB)”. The quality of the information is scalable in our proposed memory cell.

Table I. Three modes in the proposed 7T memory cell.

	# of MCs comprising 1bit	# of WL drive	CTRL (/CTRL)
Typical	1	1	“L” (“H”)
High-speed	2	2	“H” (“L”)
Dependable	2	1	“H” (“L”)

4. Dependability Simulation

In this section, we discuss the dependability of our proposed memory cell by means of a bit error rate (BER). We carried out Monte Carlo simulation of dynamic cell stability in a 90-nm process technology [5]. The followings are pass conditions in the simulation.

- In read operation,

$$\begin{cases} V(/BL) \geq V(BL)+50mV \cdots (1) \\ \text{and} \\ V(N00) < V(N01) \cdots (2) \\ \text{and/or} \\ V(N10) < V(N11) \cdots (3) \end{cases}$$

- In write operation,

$$\begin{cases} V(N00) > V(N01) \cdots (4) \\ \text{and/or} \\ V(N10) > V(N11) \cdots (5) \end{cases}$$

Figure 6 illustrates waveform examples. Figure 6 (a) is the case of the high-speed mode in read operation. Please note that both (2) and (3) are evaluated in the 2-MC, high-speed, and dependable modes while either (2) or (3) is evaluated in the 1-MC and typical modes. As well as in write operation, (4) and/or (5) are/is evaluated, depending on the modes. Figure 6 (b) is the case of the write operation.

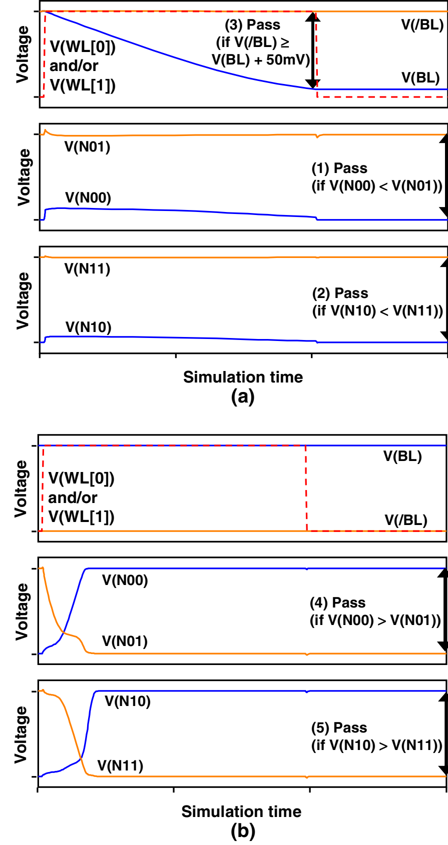


Figure 6. Simulation waveforms in (a) read operation and (b) write operation.

Figure 7 shows the BERs in the read operation. It is at the FS corner since the stability is determined by the static noise margin. (2) and/or (3) govern(s) the static noise margin [6].

In Figure 7 (a), the wordline pulse width is short (1 ns). The 2-MC mode and high-speed mode operate in a low VDD region, which demonstrates that they are superior in a fast operation. In the 2-MC mode, the self-recovery effect can not be expected because of the short wordline pulse width.

On the other hand, in Figure 7 (b), the wordline pulse width is long (20 ns). The high-speed mode and 2-MC mode have almost the same reliability, which represents the self-recovery effect in the 2-MC mode. The dependable mode of the proposed memory cell works fine below 0.5 V with a BER of 10^{-3} kept. This is because the static noise margin is larger than any other modes. The dependable mode is the most stable.

The BERs in write operation is in Figure 8. The 2-MC mode is worse than the 1-MC mode. This is reasonable because it is more difficult to write to two memory cells at the same time, than one memory cell. Neither, the dependable mode is suitable for the write operation. The conductance of the access transistors is lower in the

dependable mode. Instead, in the write operation, the high-speed mode should be utilized even in the usage of the dependable mode. In the high-speed mode, the conductance of the access transistors is higher, and thus the write margin is larger.

In the proposed dependable SRAM, we can select an appropriate mode, in terms of area overhead, speed, or dependability. The proposed SRAM is also suitable to fine-grain dynamic voltage scaling for low-power operation because it works in a low-VDD region.

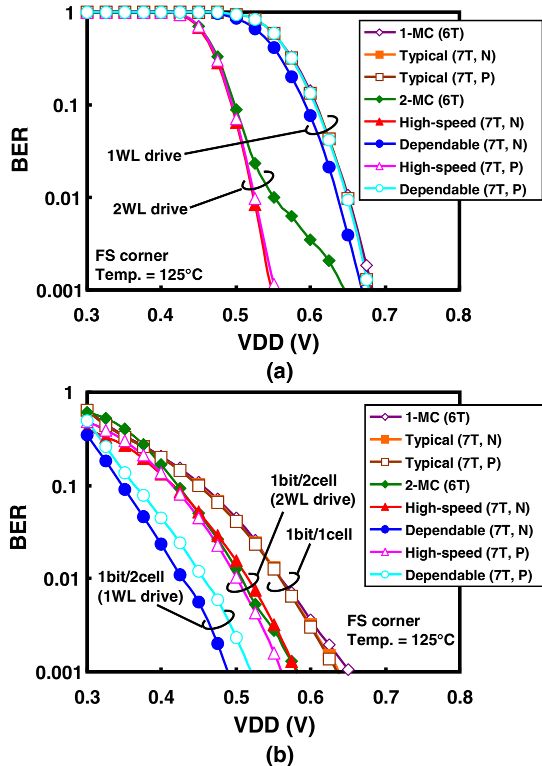


Figure 7. Bit error rates in read operation. The wordline pulse widths are (a) 1 ns and (b) 20 ns. In the legend, "6T"/"7T" signify the conventional/proposed memory cells. "N"/"P" mean that the additional transistors are nMOSes/pMOSes in the proposed memory cell. "1WL"/"2WL" are the numbers of activated wordlines.

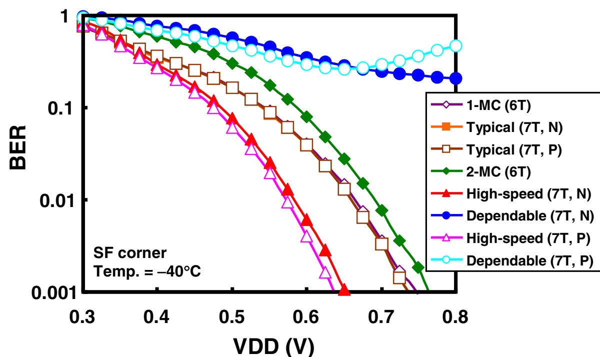


Figure 8. Bit error rates in write operation. The wordline pulse width is 20ns.

5. Summary

We designed a dependable SRAM with 7T memory cells. The proposed SRAM can dynamically change its speed and dependability, based on the concept of "quality of a bit (QoB)". The high speed and high dependability are achieved by connecting a pair of the memory cells with the additional transistors. In the dependable mode, the proposed SRAM operates below 0.5 V with a BER of 10^{-3} kept. The proposed SRAM is also suitable to fine-grain dynamic voltage scaling for low-power operation, and thus is scalable in terms of speed, dependability, and power.

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