A 0.56-V 128kb 10T SRAM Using Column Line Assist (CLA) Scheme

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Abstract

We present a small-area 10T SRAM cell without half selection problem. As well, the proposed 10T cell achieves a faster access time and low voltage operation. The cell area is reduced by 25%, and the cell current is increased by 21%, compared with the prior 10T cell. The minimum operating voltage is lowered by the column line assist (CLA) scheme that suppresses write margin degradation. By measurement, we confirmed that the proposed 128-kb SRAM works at 0.56 V.

Keywords

SRAM, low-voltage operation

1. Introduction

As process technology is scaled down, threshold voltage variation is increased. In particular, degradation of operating margins (both of read and write margins) in an SRAM memory cell becomes a serious problem. In the classic 6T cell, it is difficult to find an optimum design because the both read and write margins must be considered; at low supply voltage, a small drive transistor in the 6T cell worsens a static noise margin, whereas a large drive transistor decreases a write margin.

At a 45 nm node and later, an 8T cell will be smaller than the classic 6T cell [1]. However, the 8T cell has a readout speed penalty due to its single read bitline structure. Even if a hierarchical bitline structure is adopted to improve the readout speed, the additional peripheral circuits cause an area overhead. Besides, in the post-classic SRAM cells including the 8T cell, the divided-wordline structure or write-back scheme is needed to address the half-selection problem in the write operation [1-5]; the bit-interleaving scheme [6] to cope with multiple-bit soft errors cannot be utilized in these cells.

As a novel SRAM cell, a 10T cell, which does not have to consider the half-selection problem in nature even below a sub-threshold voltage, has been proposed [7]; the cell size is, however, large due to complicated interconnects. In this paper, we propose a smaller 10T cell without the half-selection problem. As well, the proposed 10T cell draws a larger cell current, which achieves faster readout operation.

2. Proposed 10T Memory Cell

Figures 1 and 2 show the schematics and layouts of the prior [7] and proposed 10T cells, respectively. In the both 10T cells, four nMOS transistors (N4, N5, N6, and N7) are appended to the classic 6T cell. The layouts (Figures 1 (b) and 2 (b)) are based on a 45-nm logic rule. The proposed 10T cell (0.49 μm x 1.57 μm) saves 25% cell area, compared to the prior one (0.65 μm x 1.58 μm), in both of which all transistors are minimum. In the prior 10T cell, it is difficult to make a small layout, in particular in the parts of nMOSes, because interconnections are complicated; although the gate of N4 (N5) is connected to the gates of P1 and N1 (P0 and N0), the drain of N4 (N5) is connected to N2 and N6 (N3 and N7), which increase the interconnects and makes the cell height tall.

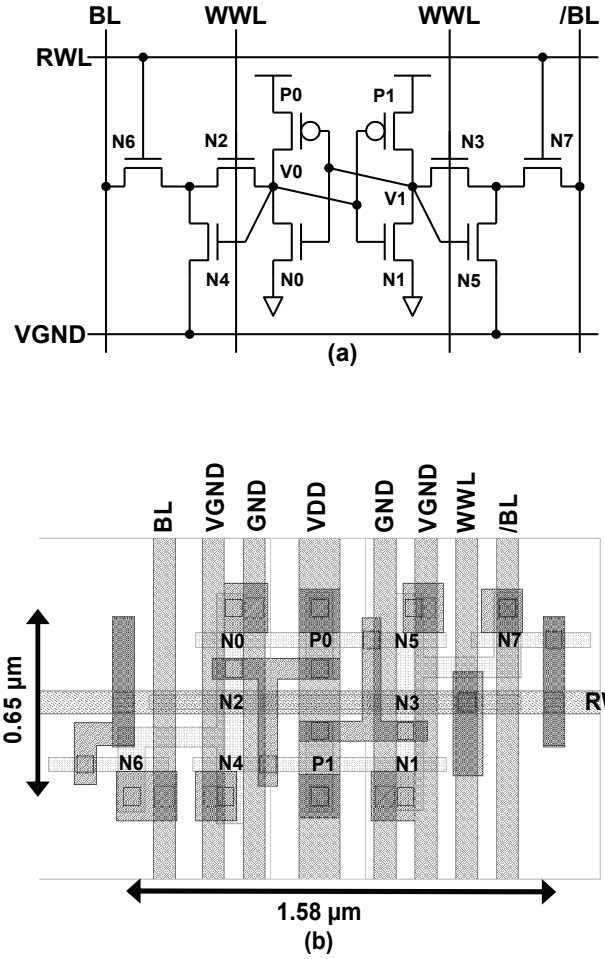

Figure 1: Prior 10T cell: (a) schematic and (b) layout.

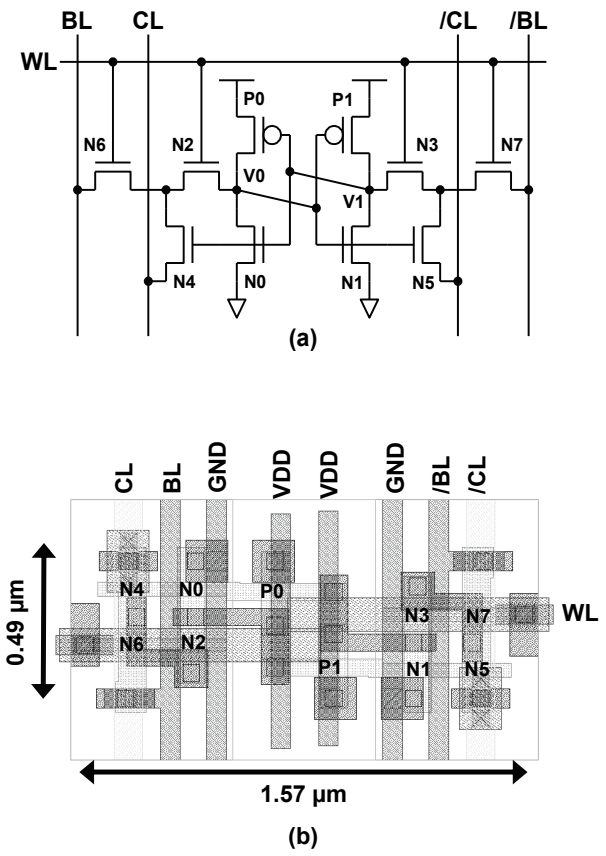

Figure 2: Proposed 10T cell: (a) schematic and (b) layout.

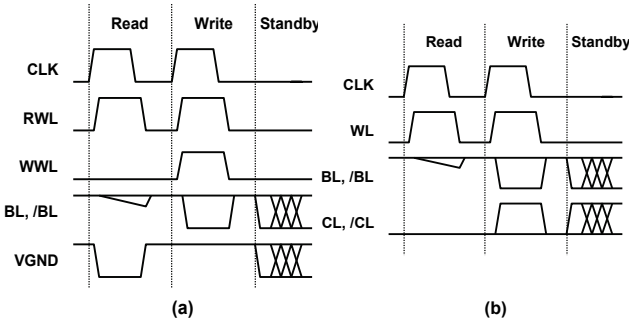

Figure 3: Operation waveforms: (a) prior and (b) proposed 10T cells.

In Figure 3, the operation waveforms of the prior and proposed 10T cells are illustrated. Figure 4 compares cell currents in read operation. In the prior 10T cell, RWL is enabled, WWL is disabled, and VGND is grounded; a cell current flows through the outside access transistor (N6 or N7) to VGND. On the other hand, in the proposed 10T cell, WL is activated, and both CL and /CL are set to the ground level, which is alike as the read operation in the prior 10T cell. However, the readout cell current is larger than the prior 10T cell; note that, in the proposed 10T cell, there is two current paths as illustrated in Figure 4 (b): solid line, BL (or /BL) to CL (or /CL), and dotted line, BL (or /BL) to GND. This high-speed operation is achieved by our proposed column lines assist (CLA) scheme using CL and /CL.

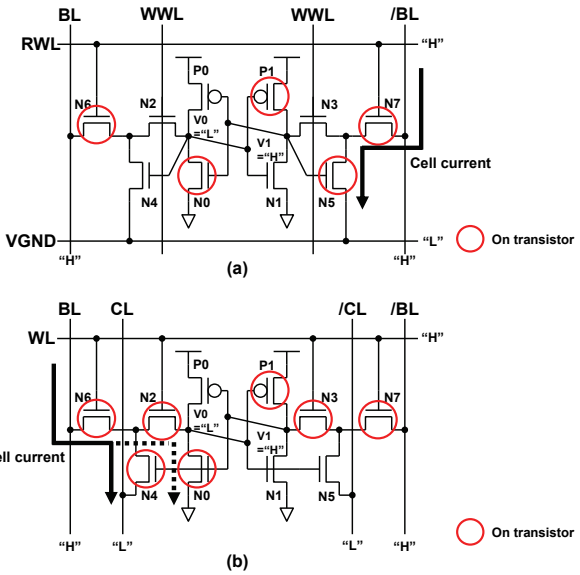

Figure 4: Cell currents in read operation: (a) prior and (b) proposed 10T cells.

The current paths in the write operation are shown in Figure 5. Now, the internal nodes, "V0" and "V1", are "L" and "H", and then we try to write them over. So, "V0" (= "L") and "V1" (= "H") are respectively charged and discharged through the access transistors (solid lines in Figure 5). In addition to the prior 10T cell, another current from CL (or /CL) (dotted line) helps the write margin enlarge in the proposed 10T cell; we can set CL and /CL to the equal voltage of BL and /BL, respectively, in the write operation. CL and /CL are exploited as write assist, too.

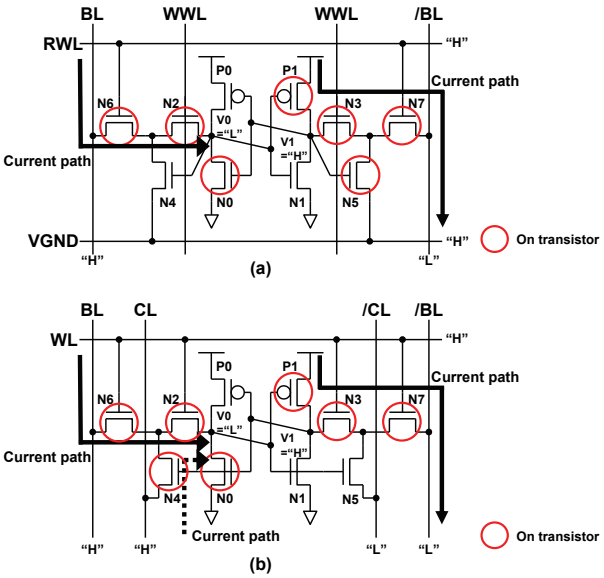

Figure 5: Cell currents in write operation: (a) prior and (b) proposed 10T cells.

In a standby mode, BL and /BL in the both cells are floated to reduce bitline leakage from BL and /BL to GND through the access transistors. As well, CL and /CL in the

proposed 10T cell and VGND in the prior one become floating state in the standby mode.

Figure 6 portrays the block diagram of the proposed 10T cells. WLs are horizontally interconnected, whereas BLs, /BLs, CLs and /CLs are vertically interconnected. CL and /CL are changed in accordance with operations, which best explains the CLA scheme: CL and /CL are sustained at GND in the read operation to improve the readout current, as mentioned before. In contrast, in the write operation, CL (/CL) has the same value as BL (/BL), which assists the write operation itself; data are written from the both paths of the bitline and column line.

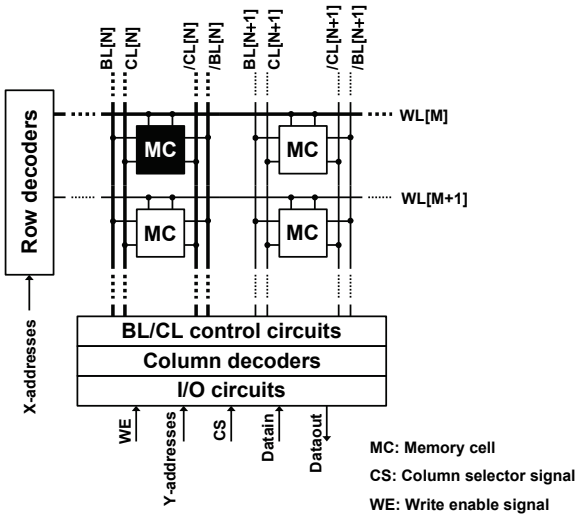

Figure 6: Block diagram of proposed 10T SRAM.

3. Quantitative Comparison of 10T Cells

The following subsections make comparisons between the prior and proposed 10T cells, from the standpoints of static noise margin (SNM) [9], write trip point (WTP) [10], readout cell current, and standby leakage current. Note that, as previously mentioned, the proposed 10T cell is 25% smaller than the prior one, with respect to the cell size.

3.1. Static Noise Margin (SNM)

Figure 7 shows the SNMs. The prior 10T cell has a larger SNM, because only the outside access transistors are activated, which improves a β ratio. In the proposed one, all the access transistors are asserted as already illustrated in Figure 4. However, minimum operating voltages of the both cells are determined by write operation margins but not the SNMs; this is because they both have series-connected access transistors (N2 + N6, and N3 + N7) that degrade the write operation margins.

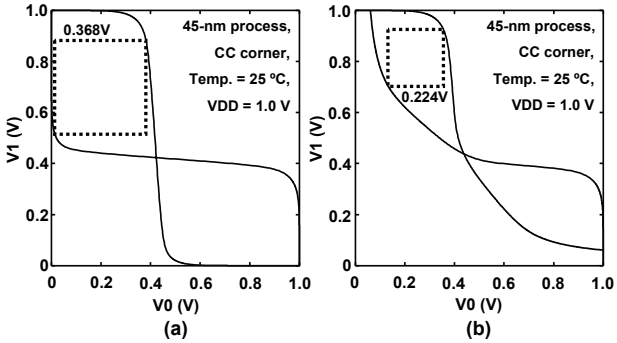

Figure 7: Static noise margins (SNMs): (a) prior and (b) proposed 10T cells.

3.2. Write Trip Point (WTP)

In a case where a cell topology is the same as the proposed 10T cell yet CL and /CL are always grounded (see Figure 8 (b)), the WTP is 0.256 V and smaller than that of the prior one (= 0.271 V). By introducing the CLA scheme, the proposed 10T cell gains a larger WTP (= 0.285 V) than the prior one. This simulation demonstrates that the proposed 10T cell achieves a lower minimum operating voltage, because it is limited by write operating margin as mentioned in the previous subsection.

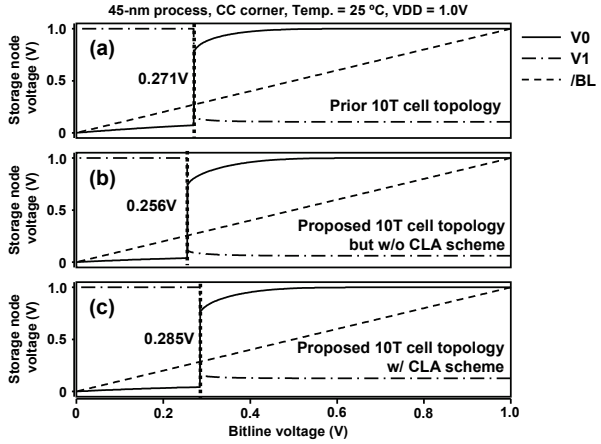

Figure 8: Write trip points (WTPss): (a) prior and (b) without and (c) with CLA schemes in proposed 10T cell topology.

3.3. Readout Cell Current

Figure 9 makes comparison of readout cell currents. The proposed 10T cell improves the readout cell current by 21% over the prior one, because both the outside and inside access transistors are asserted in the read operation (see Figure 4 (b)). Thus, the proposed 10T cell achieves a faster access time than the prior one on a same voltage condition; Figure 10 exhibits bitline delays. The proposed 10T cell shortens the bitline delay by 34%, compared to the prior one, when ΔV on a bitline is set to 0.1 V.

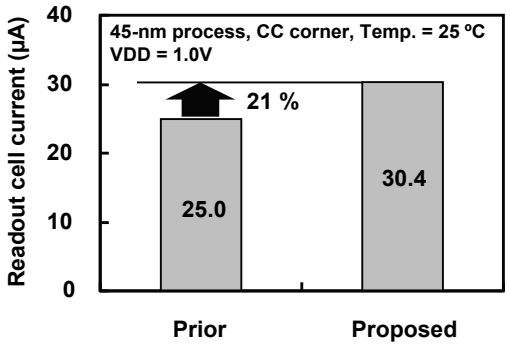

Figure 9: Readout cell currents.

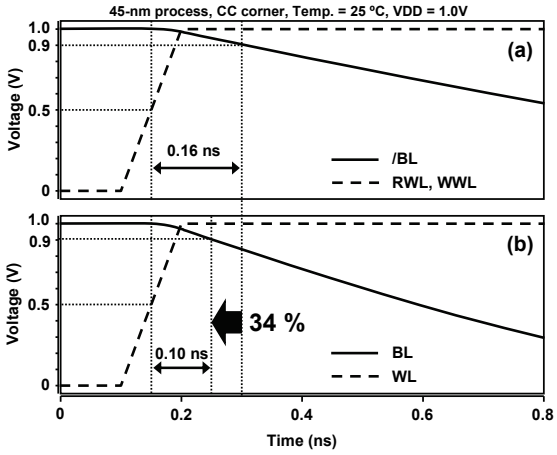

Figure 10: Bitline delay simulation: (a) prior and (b) proposed 10T cells.

3.3. Standby Leakage Current

Figure 11 illustrates standby leakage currents. The standby leakage current of the proposed 10T cell is almost same as that of the prior one.

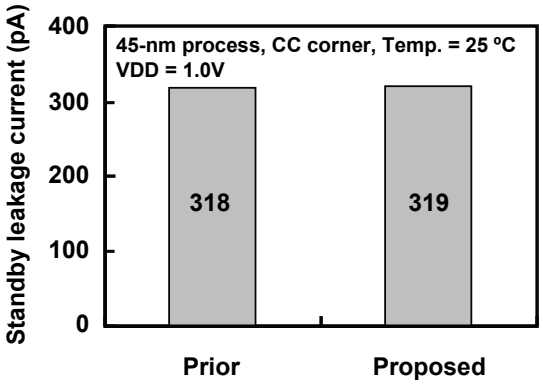

Figure 11: Standby leakage currents.

4. Chip Measurement Results

Figure 12 shows a micrograph of a 128-kb SRAM test chip and SEM micrograph of the proposed 10T cell, both in a 45-nm process technology.

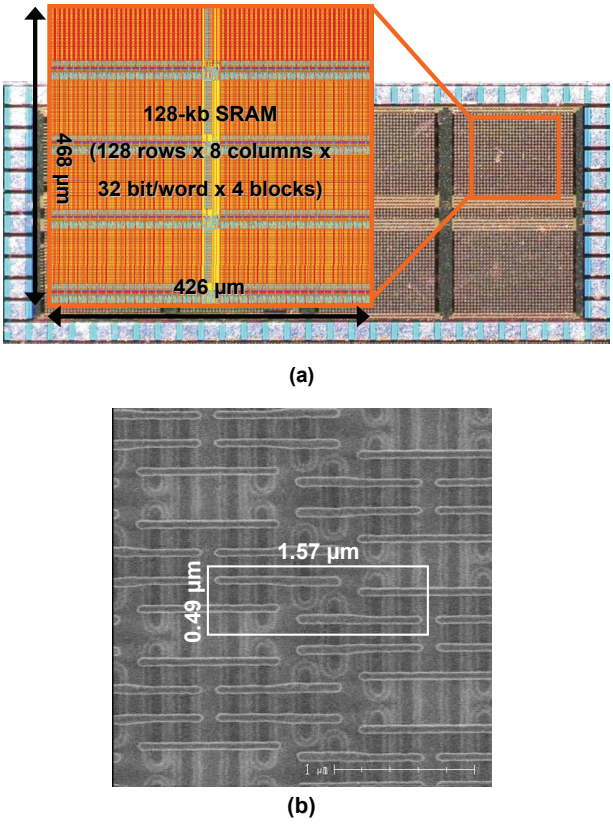

Figure 12: (a) Micrograph of 128-kb test chip, and (b) SEM micrographs of proposed 10T cell.

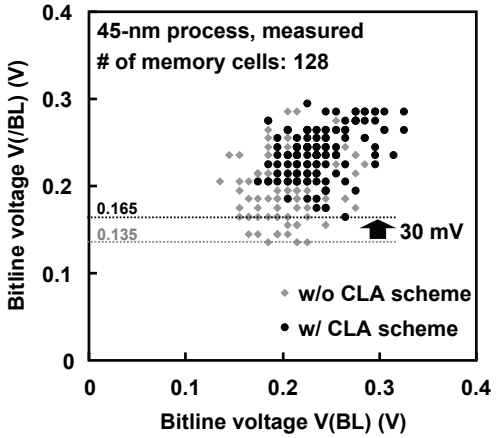

Figure 13: Measured write trip points (WTPs).

Figure 13 shows measurement results of the WTPs. We confirmed that the CLA scheme improves the worst-case WTP by 30 mV. Figure 14 shows measured fail bit counts (FBCs). The minimum operating voltage is limited by the write operation, as previously described. The proposed 128-kb SRAM works fine at 0.56 V (the first error bit is at 0.55 V) without a voltage boost technique that improves an operating margin. We also confirmed that the CLA scheme lowers the write operating voltage by 90 mV, over the prior one.

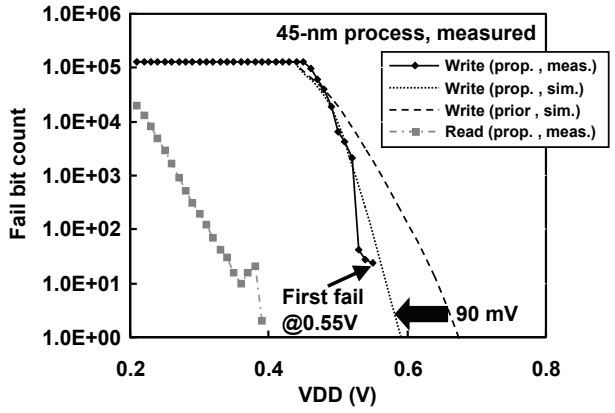

Figure 14: Fail bit counts (FBCs).

5. Summary

We proposed a high-speed and small-area 10T SRAM cell that does not causes the half selection problem. The cell area is reduced, by 25%, compared to the prior 10T cell. The cell current and bitline delay are improved by 21% and 34%, respectively. Furthermore, we verified that the proposed 10T cell extends the minimum operating voltage by using the novel column line assist (CLA) scheme; the fabricated 128-kb SRAM works fine at 0.56 V in a 45-nm process technology.

6. References

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