Outline

- Background of this work
- Abnormal leakage suppression scheme
- Circuit design
- Measurement results
- Summary
Backgrounds

Portable equipments
    Notebook PC, Phone, etc.
    → Long lifetime of batteries

SRAM = key component
    Cache / main memory, etc.
    → Low standby current SRAM

Leakage current due to cell defects has not been eliminated.
How to eliminate abnormal leakage

Systematically isolate error cells from

- $V_{DD}$ lines
- or
- $V_{SS}$ lines

However...

$V_{SS}$ lines are usually structured as a mesh.

→ Difficult to cut off selectively
Possible leakage sources in standby mode

- Word lines are fixed to ground.
- Bit lines are precharged to $V_{DD}$.

Leakage current sources

1. Cell $V_{DD}$ lines
2. Bit lines
3. N wells
Leakage paths from cell $V_{DD}$ lines (1)

WL driver

$V_{DD}$

Word line (=low)

Cell $V_{DD}$

Bit line

$M5$

$M3$

$M4$

Bit line

$M6$

$LP5$

$X$ Defect

..... Leakage path(LP)
Leakage paths from cell $V_{DD}$ lines (2)

- Defect
- Leakage path (LP)

Diagram showing leakage paths through transistor M3 and M4 from the word line to the bit line with $V_{DD}$.
Leakage paths from bit lines

- Defect
- Leakage path (LP)

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Abnormal Leakage Suppression (ALS) scheme

- Monitor current through each cell V_{DD} line and bit line with a leakage sensor.
  - Sensors output 1(error) or 0(normal).

- Read out the bit pattern by a shift register.
  - Identify the location of errors.

- Isolate error cells from V_{DD} by blowing additional fuses.
Whole structure of ALS SRAM

- **Shift register**
- **Row sensors output**
- **DFF**
- **Sensor**
- **Bit lines**
- **Fuse**
- **Cell V_{DD}**
- **Column sensors output**

Diagram shows a circuit with V_{DD} connections, a shift register, DFFs, sensors, and cell V_{DD} connections.
Microphotograph of SRAM chip

Row leakage sensors + shift register

Column leakage sensors + shift register

256 rows

256 columns

Memory cells

3.0mm

2.7mm

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Microphotograph of sensors and fuses

Leakage sensor and DFF        Fuse        Cell $V_{DD}$ line

Leakage sensor : one per 2 rows/columns
Chip design and technology

- Technology
  - 0.6µm CMOS
  - 3 Metals
  - 3.3V Power Supply

- ALS SRAM design
  - 64kb (256 rows and 256 columns)
  - Total area : 8.1mm$^2$
  - ALS area overhead : 7%
For 4M bit SRAM, area overhead is less than 1%.
Schematic of ALS circuits

Leakage sensor

\( V_{\text{LEAK MONITOR}} \)

\( V_{\text{DD}} \)

\( \text{M7} \)

\( \text{M8} \)

Test

Enable

Leakage sensor

\( (=voltage\ comparator) \)

Sensor Output #1

DFF

Sensor Output #2

Control signals

\( V_{\text{REF}} \)

to bit lines or cell \( V_{\text{DD}} \)
Circuit schematic of leakage sensor

V_{LEAK MONITOR} → Leakage sensor → N2

Test Enable

V_{DD} → N1

φ_{transfer} → DFF

Hold

V_{REF} → Hold

output #1 → fuse → shift register

output #2 → to bit lines or cell V_{DD}
Operation of leakage sensor

Control signals for sensors

Hold
SE
\( \phi_{transfer} \)

Non-overlapping clock for shift register
Shift register circuit and operation

Control signals for shift registers

Shift register output

"1" error

"0" normal

Measured sensor sensitivity

<Leakage sensor>
Measured leakage reduction

- Leakage current: \[ \mu \mu \mu \mu A \]
- Number of blown fuses:
  - 12340
  - 100
  - 50
  - 0
- Measurement: \( \approx 40 \mu A \)

Diagram:
- V_{DD}
- Cell V_{DD}
- Normal memory cell
- Error cell (made intentionally)

Graph:
- Leakage current [\mu A]
- Number of blown fuses
- Measurement
  - \( \approx 40 \mu A \)
Conclusion

- ALS scheme for low standby current SRAMs is proposed.
- Leakage current due to device defects is detected and eliminated by using leakage sensors, shift registers, and fuses.
- Test chip fabricated by 0.6µm design rule
  - ALS detects 1µA order leakage current.
  - Area overhead is about 1% in 4Mb SRAM.