Outline

- Background of this work
- Abnormal leakage suppression scheme
- Circuit design
- Measurement results
- Summary

Backgrounds

Portable equipments

Notebook PC, Phone, etc.

➡ **Long lifetime of batteries**

SRAM = key component

Cache / main memory, etc.

➡ **Low standby current SRAM**

Leakage current due to cell defects has not been eliminated.

How to eliminate abnormal leakage

Systematically isolate error cells from

- V_{DD} lines

or

- V_{SS} lines

However…

V_{SS} lines are usually structured as a mesh.

➡ Difficult to cut off selectively

Possible leakage sources in standby mode

- Word lines are fixed to ground.
- Bit lines are precharged to V_{DD}.

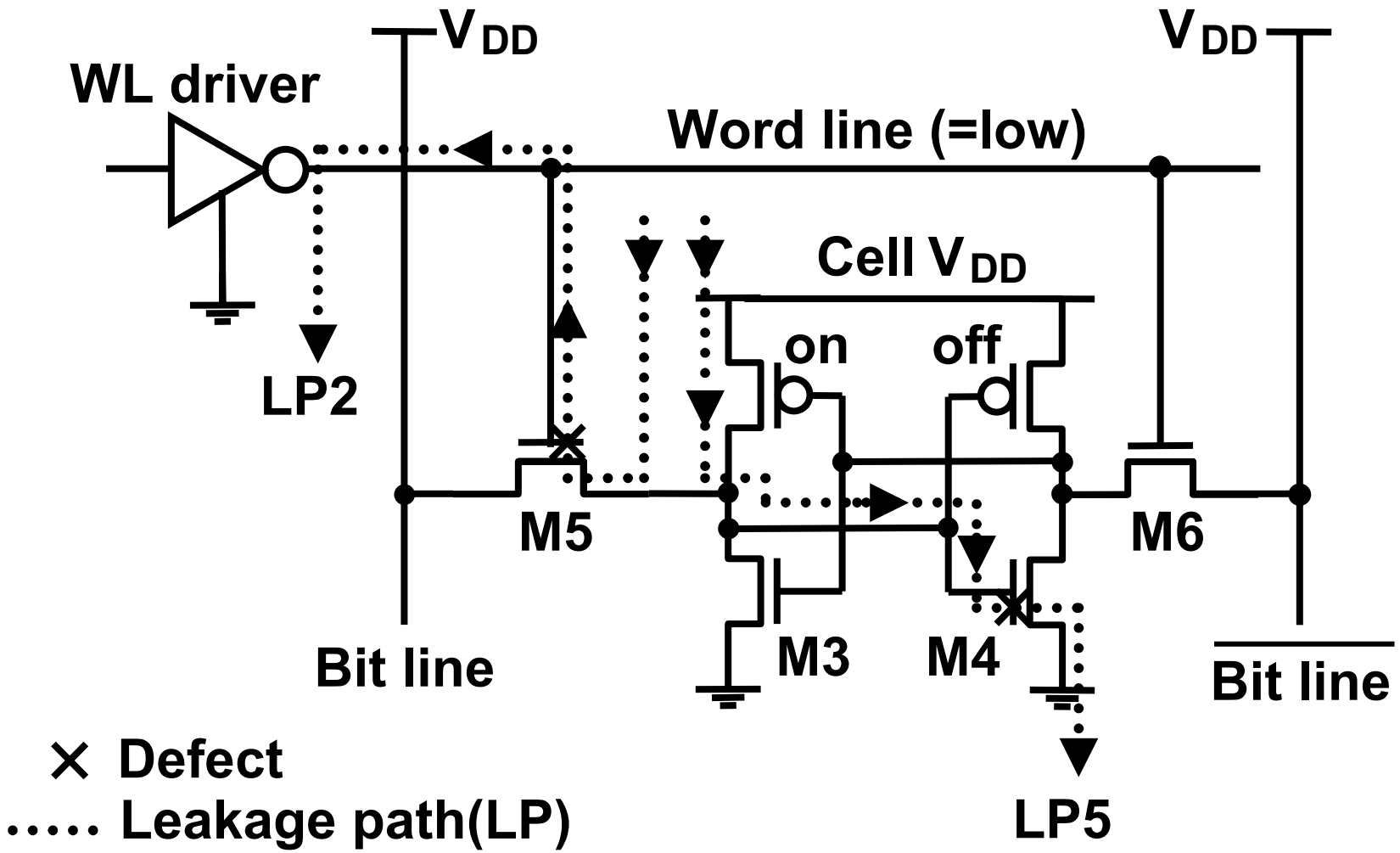
→ Leakage current sources

1 Cell V_{DD} lines

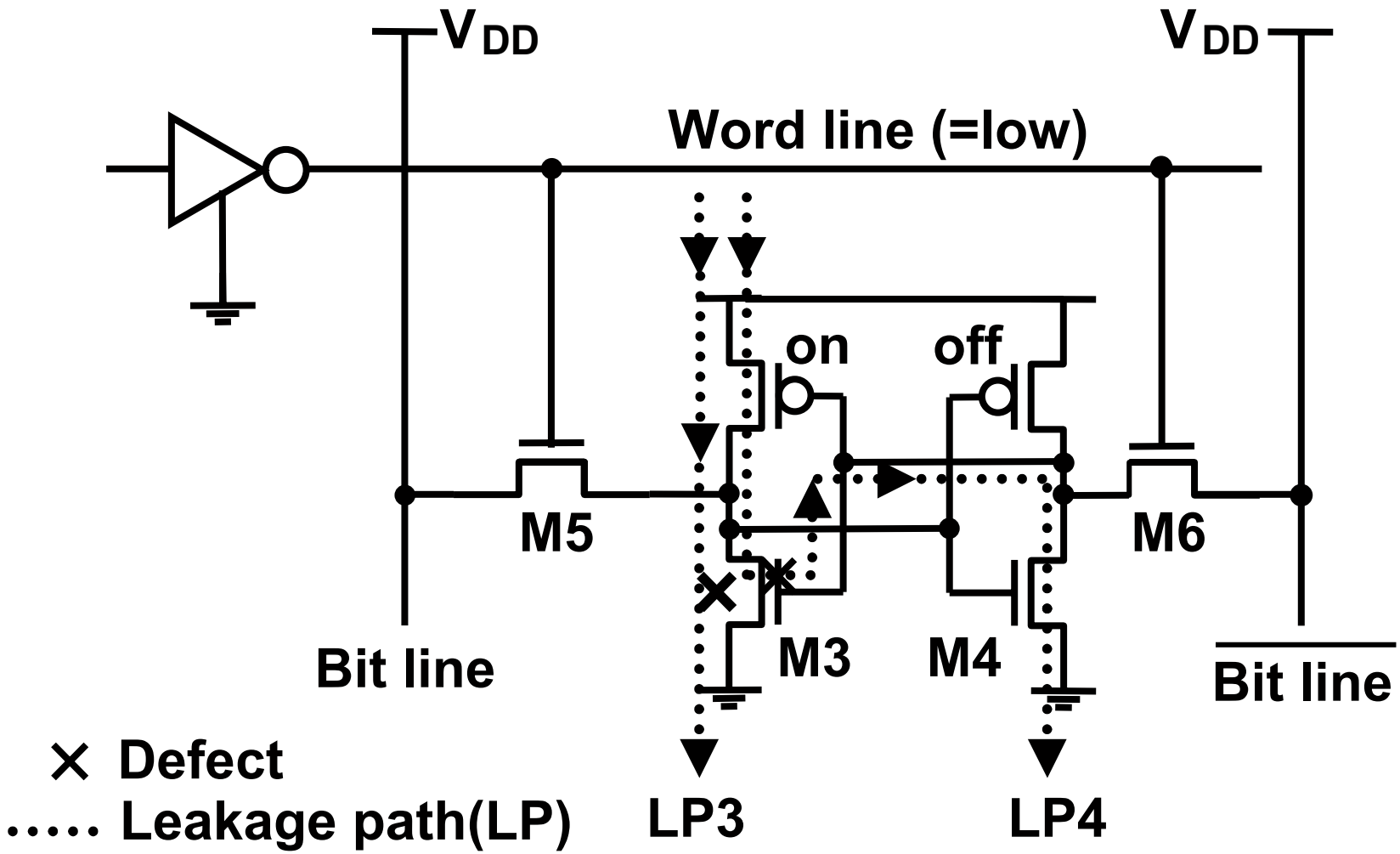
2 Bit lines

3 N wells

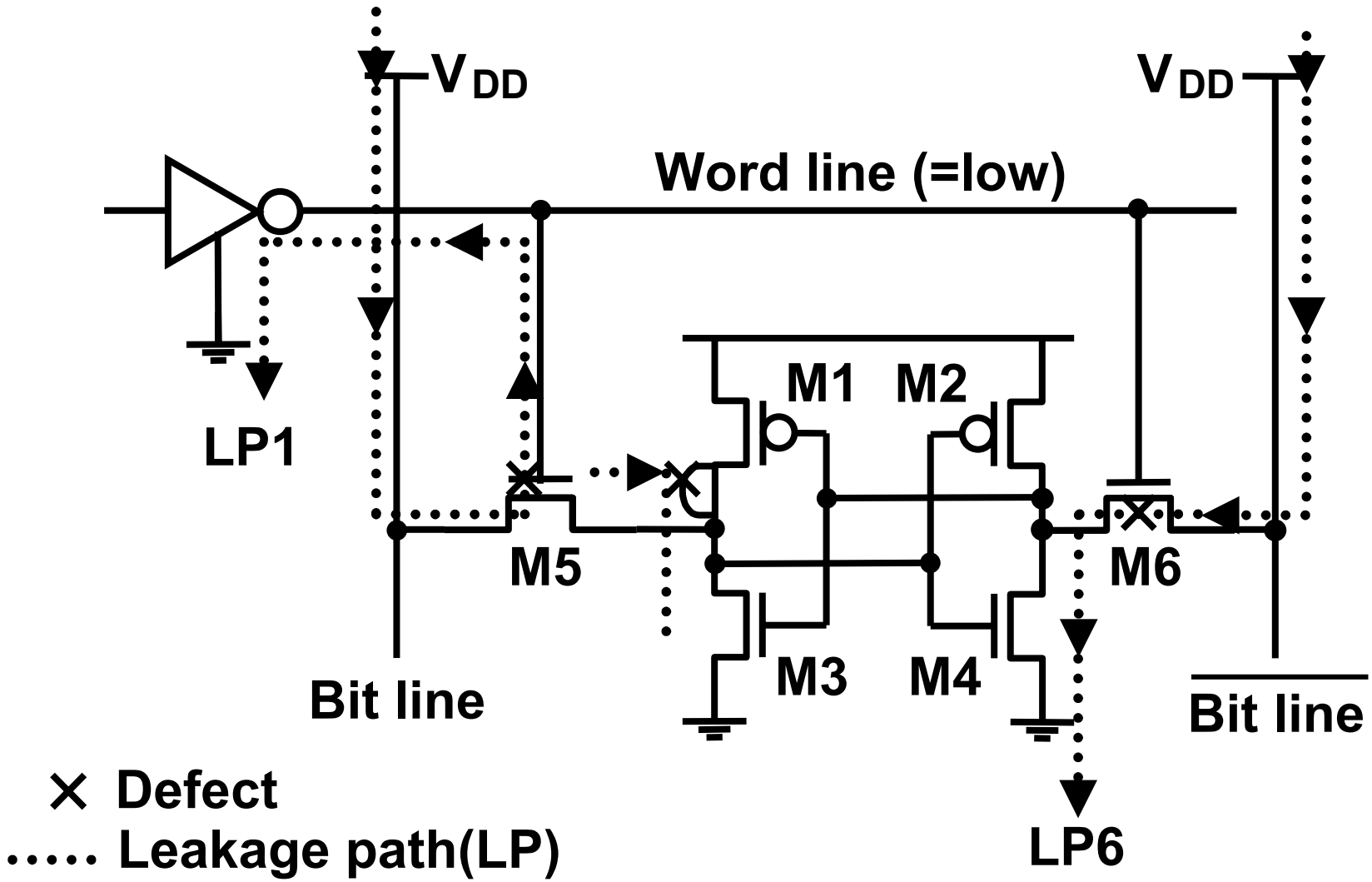
Leakage paths from cell V_{DD} lines (1)



Leakage paths from cell V_{DD} lines (2)



Leakage paths from bit lines



Abnormal Leakage Suppression (ALS) scheme

- Monitor current through each cell V_{DD} line and bit line with a leakage sensor.

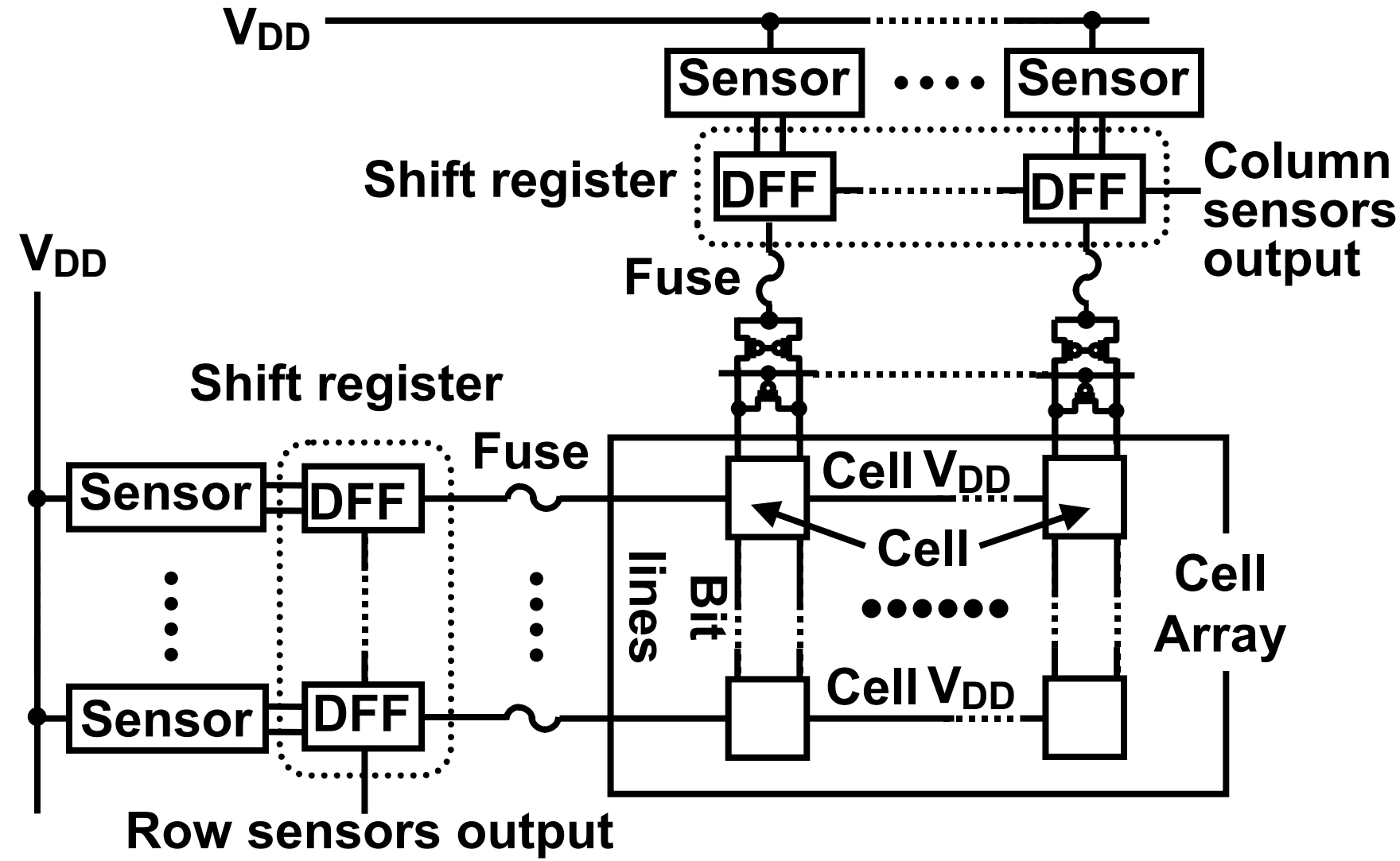
  → Sensors output 1(error) or 0(normal).

- Read out the bit pattern by a shift register.

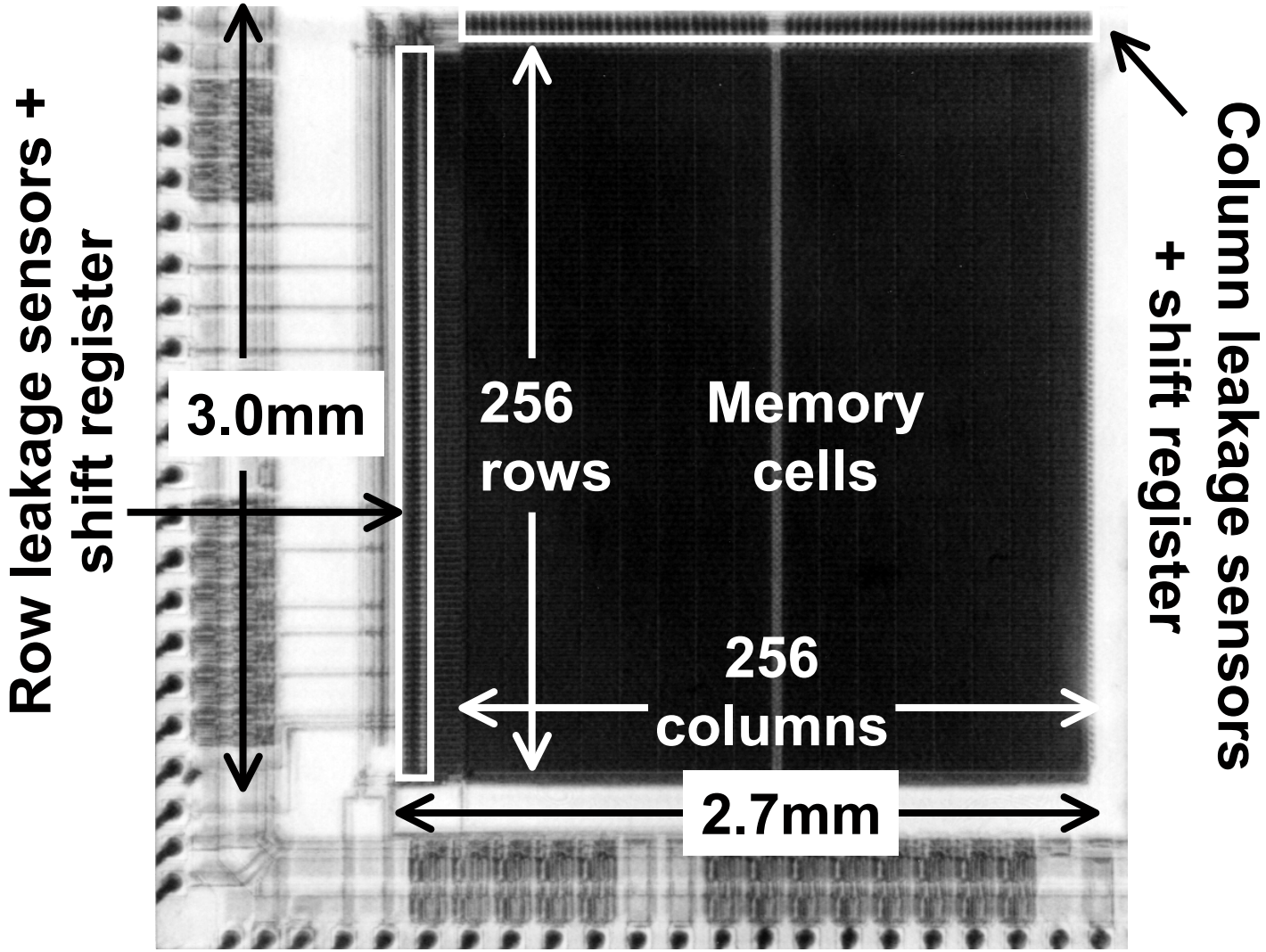
  → Identify the location of errors.

- Isolate error cells from V_{DD} by blowing additional fuses.

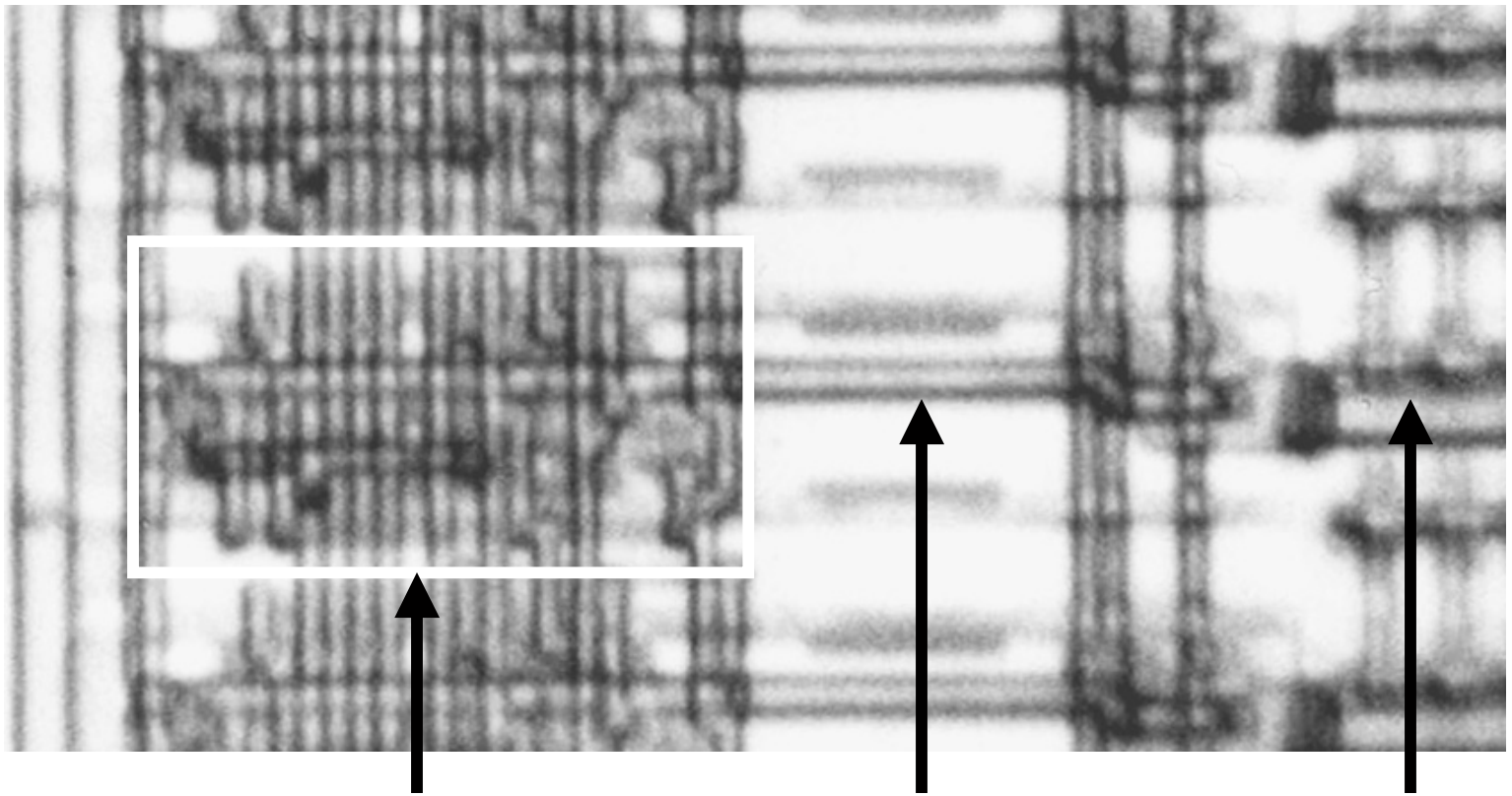
Whole structure of ALS SRAM



Microphotograph of SRAM chip



Microphotograph of sensors and fuses

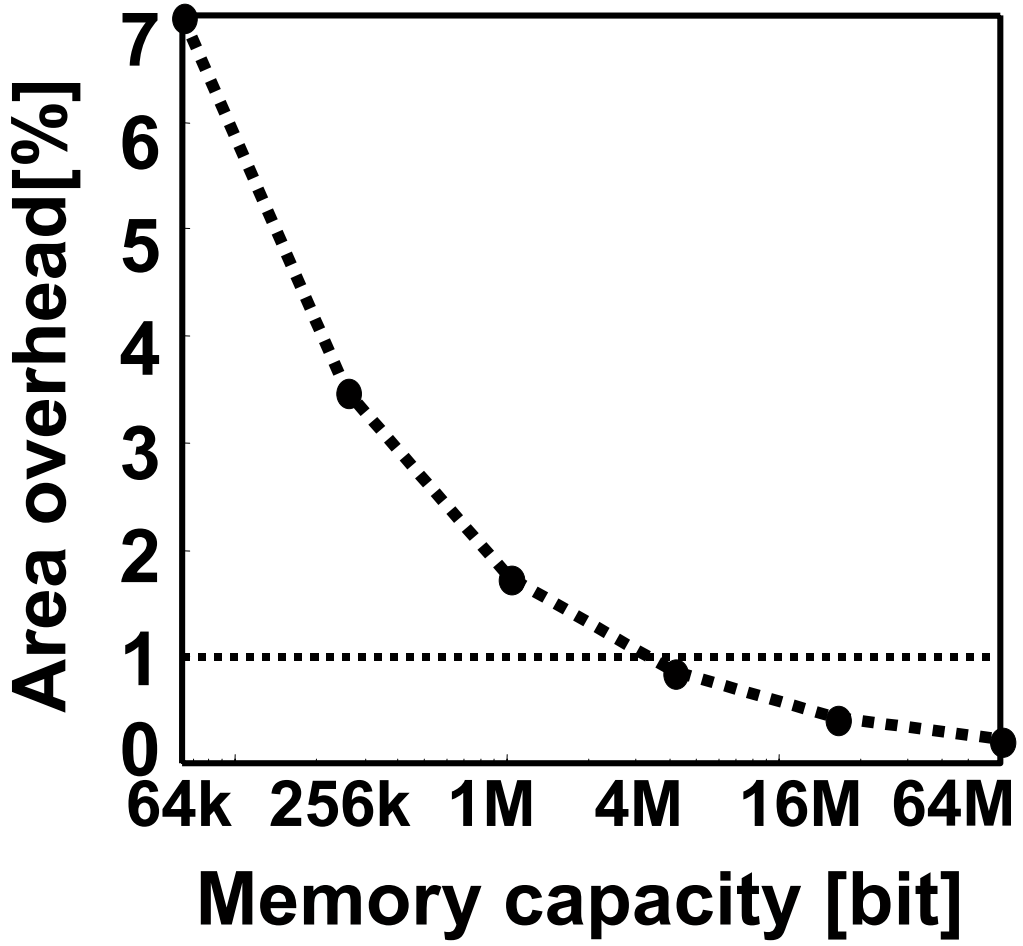


Leakage sensor : one per 2 rows/columns

Chip design and technology

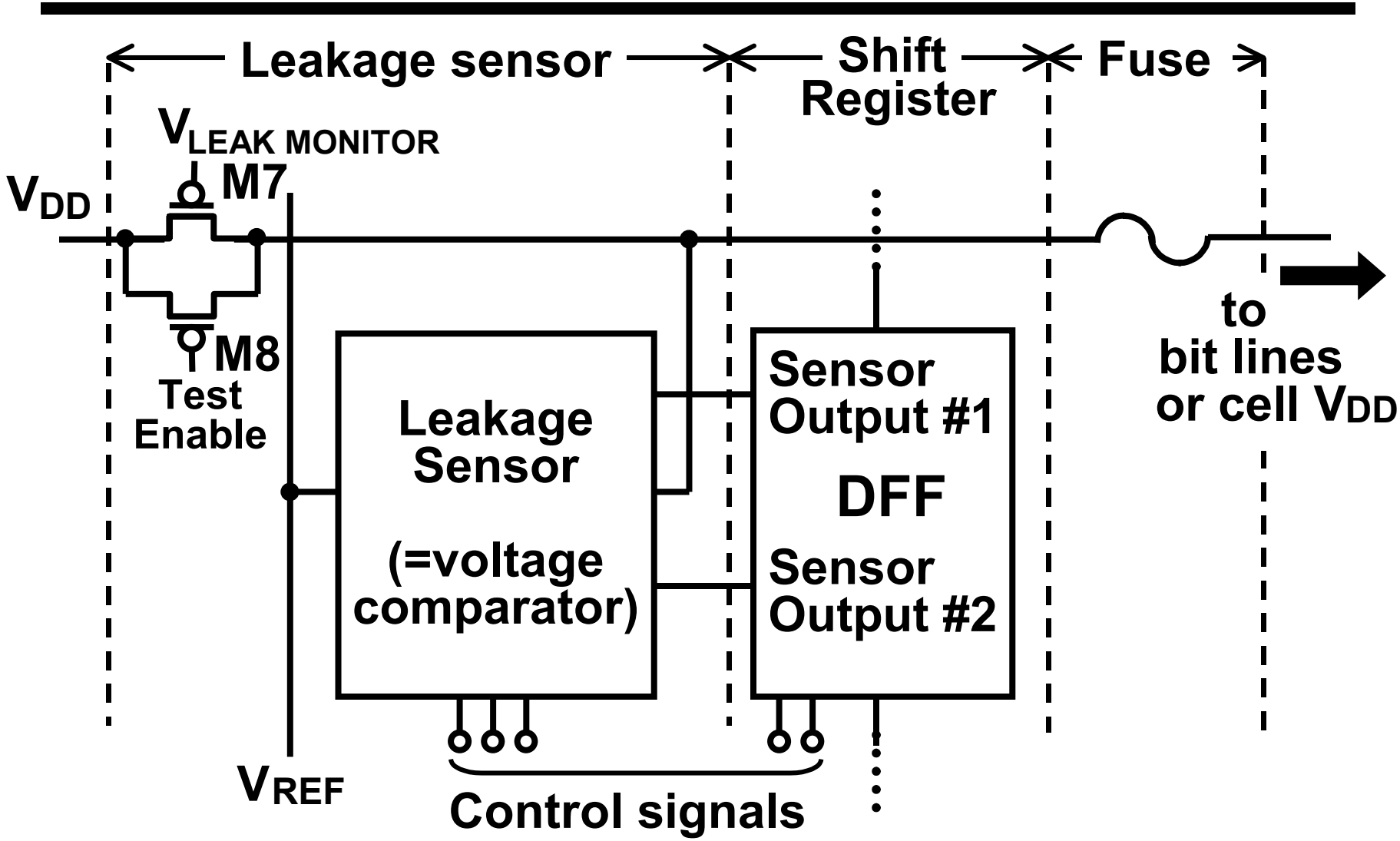
- **Technology**
  - 0.6μm CMOS
  - 3 Metals
  - 3.3V Power Supply
- **ALS SRAM design**
  - 64kb (256 rows and 256 columns)
  - Total area : 8.1mm^2
  - ALS area overhead : 7%

Area overhead vs memory capacity

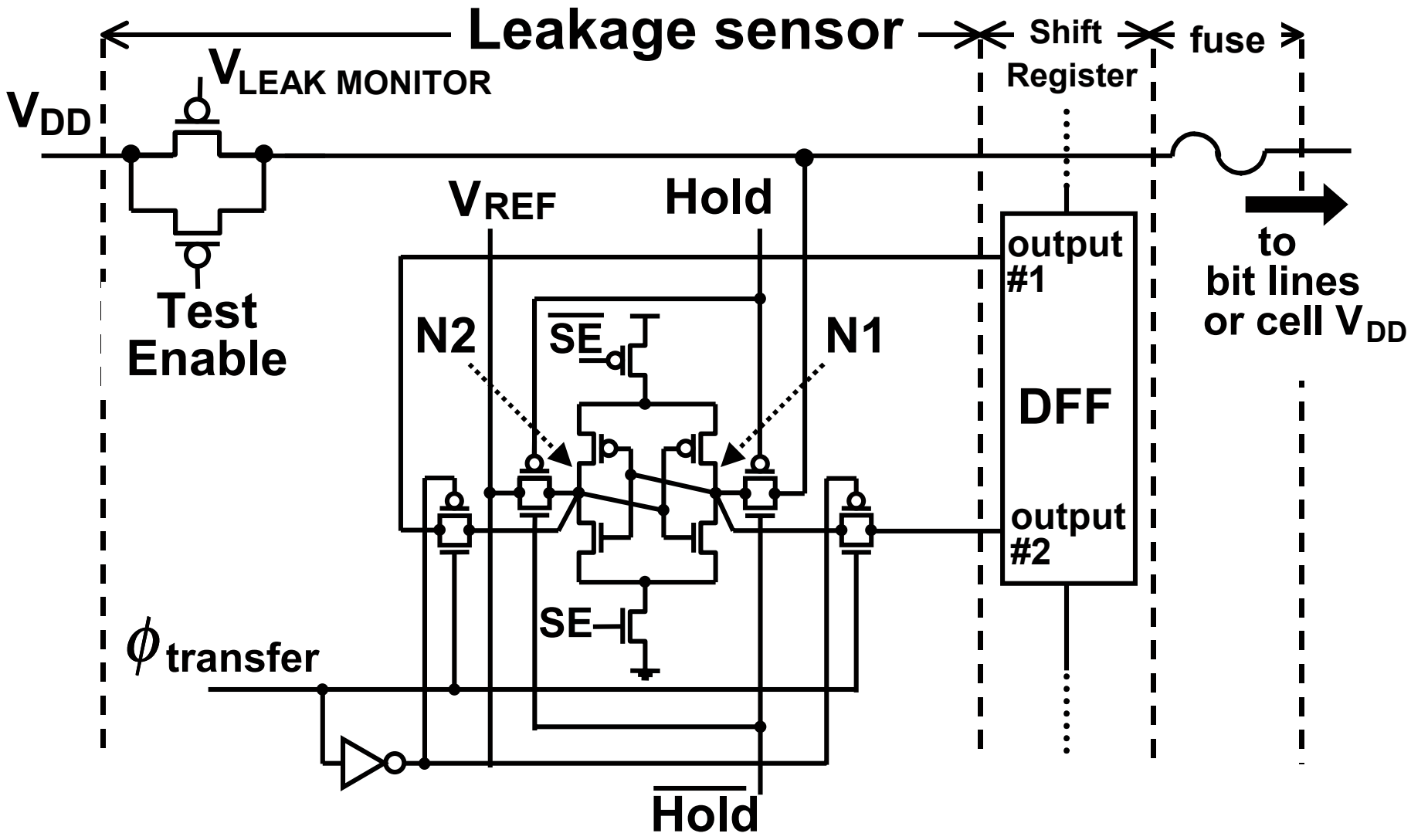


For 4M bit SRAM, area overhead is less than 1%.

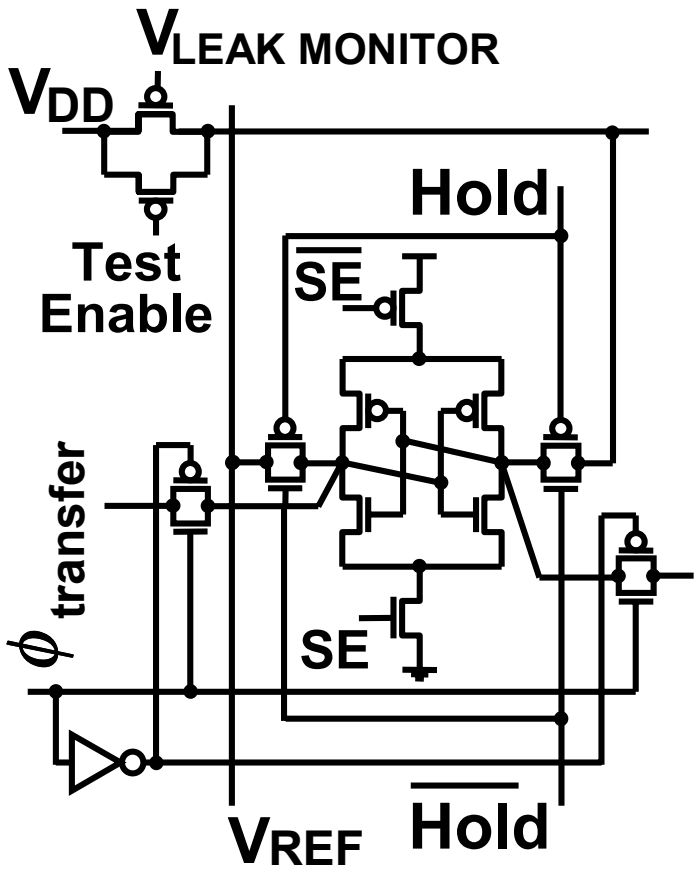
Schematic of ALS circuits



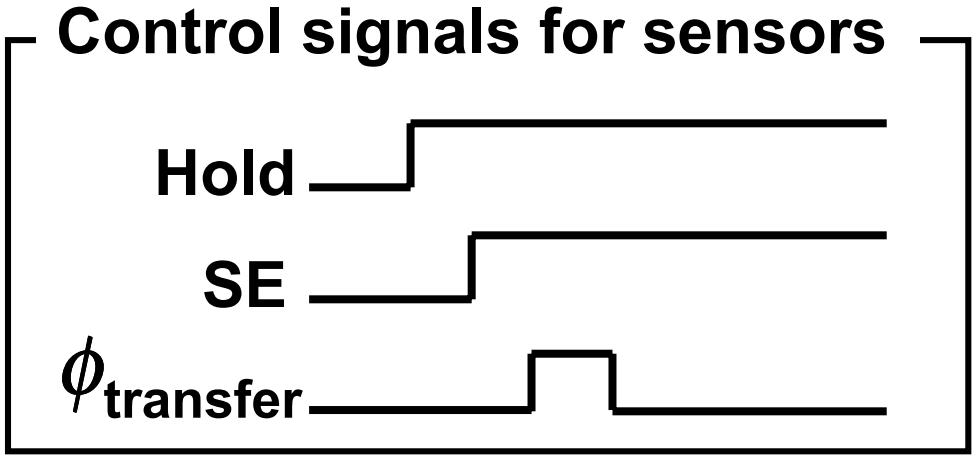
Circuit schematic of leakage sensor

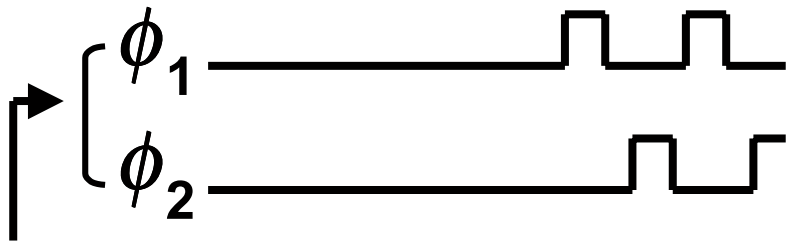


Operation of leakage sensor



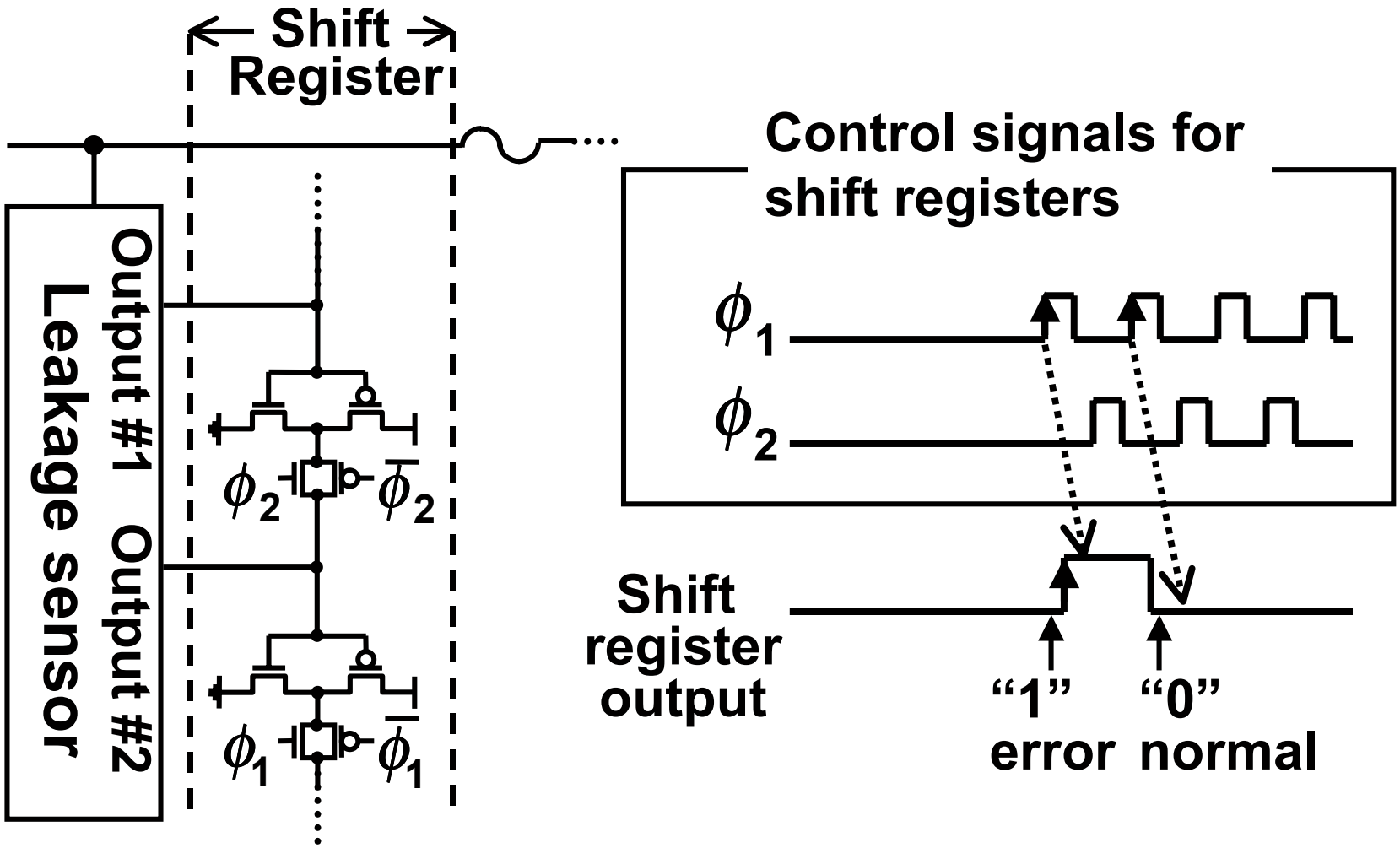
<Leakage sensor>



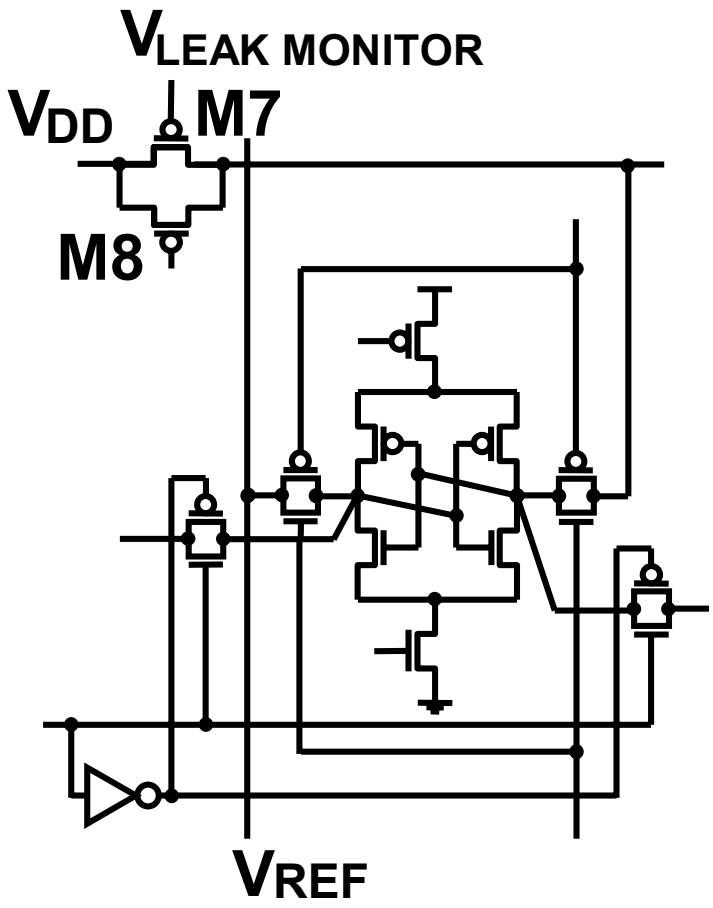


Non-overlapping clock for shift register

Shift register circuit and operation



Measured sensor sensitivity



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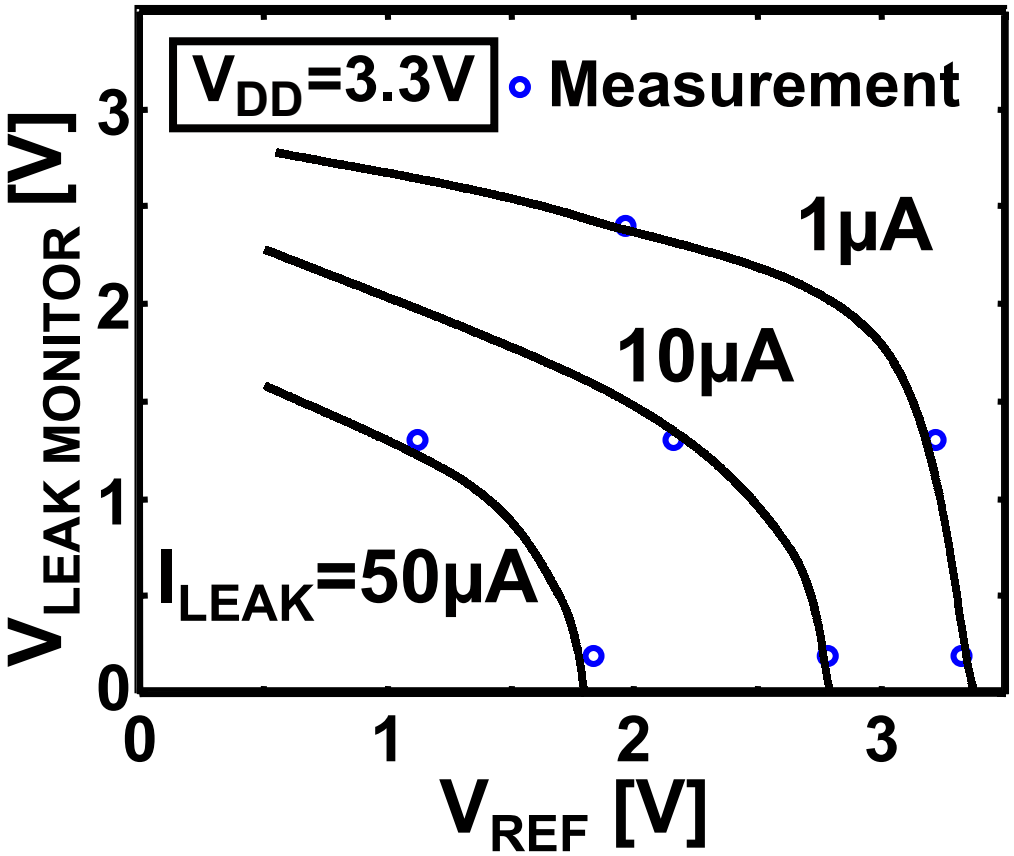
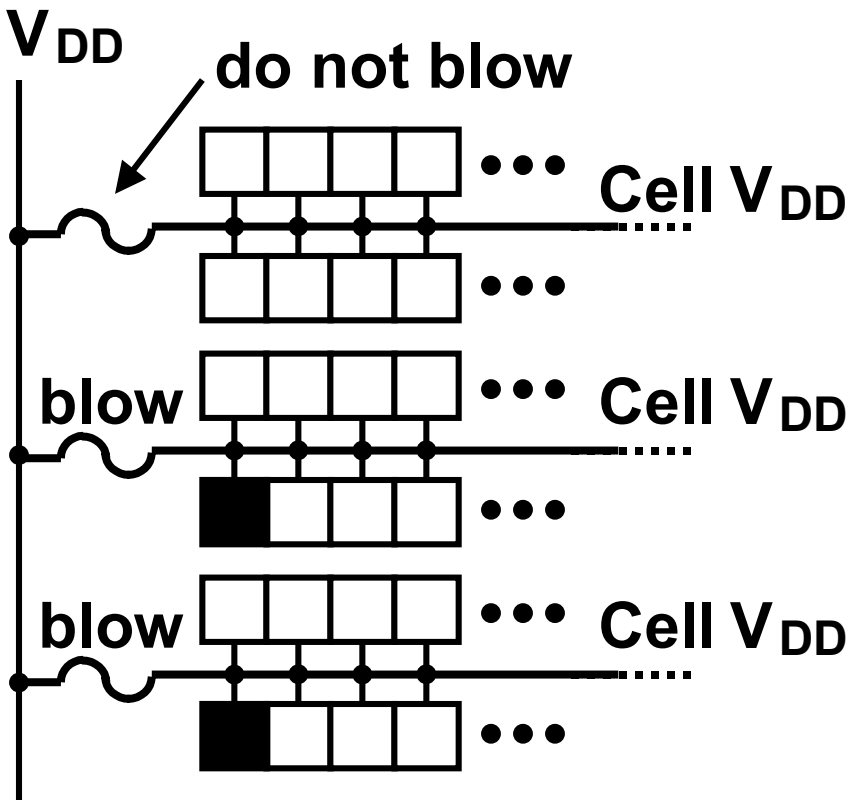
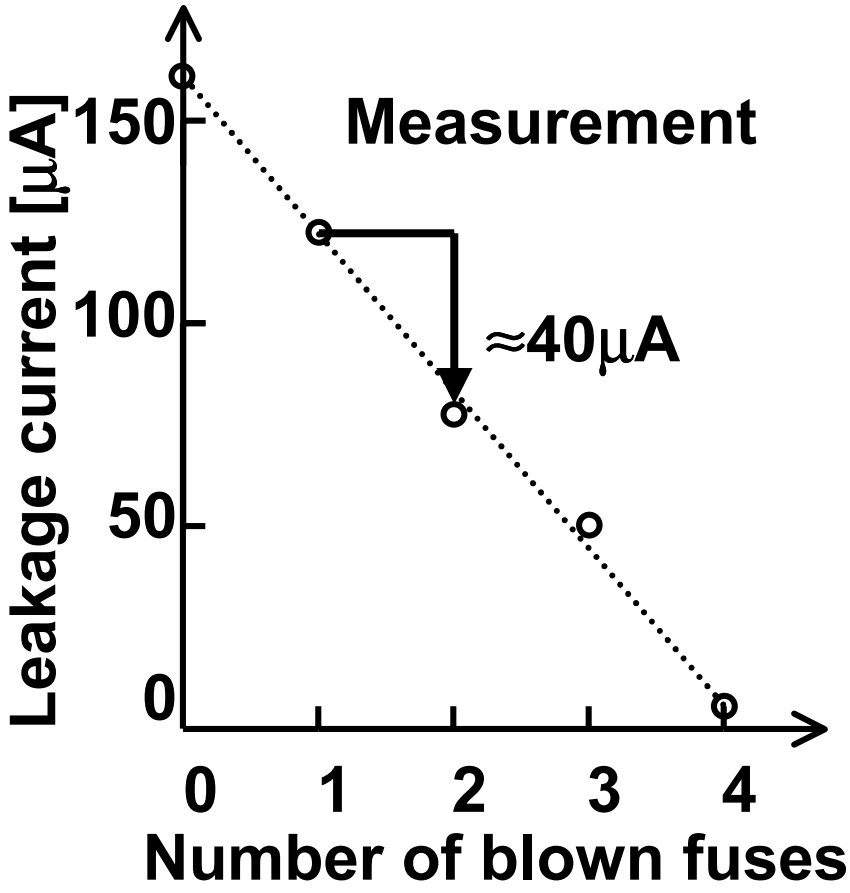


Measured leakage reduction



Normal memory cell

Error cell
(made intentionally)



Conclusion

- ALS scheme for low standby current SRAMs is proposed.
- Leakage current due to device defects is detected and eliminated by using leakage sensors, shift registers, and fuses.
- Test chip fabricated by 0.6μm design rule
  - ALS detects 1μA order leakage current.
  - Area overhead is about 1% in 4Mb SRAM.