6.3 A 0.5V, 400MHz, V_{DD}-Hopping Processor with Zero-V_{TH} FD-SOI Technology

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Fully-depleted silicon-on-insulator (FD-SOI) technology is promising because of its scalability. A 0.5V 100MHz adder and SRAM in FD-SOI has been previously reported [1]. A much faster 0.5V 400MHz FD-SOI processor is presented with power consumption of the 3.5mW. High-speed operation is achieved with zero threshold voltage (V_{TH}). To suppress leakage, memories accounting for 85% of transistor count are built with a higher V_{TH} of 0.3V. A higher speed of 800MHz is achieved with a 0.9V supply voltage (V_{DD}) through the V_{DD}-hopping scheme [2], where the higher V_{DD} is applied only when higher performance is needed. It is demonstrated that V_{DD}-hopping is effective even in leakage dominant environments.

The block diagram of the 16b RISC processor is shown in Fig. 6.3.1. A low V_{DD} and V_{TH} denoted as V_{DDL} and V_{THL} are used in the logic part to achieve high-speed operation. V_{THL} is 0V, and V_{DDL} varies from 0.5V to 1V. A higher V_{DD} (V_{DDH}) and V_{TH} (V_{THH}) are used in the instruction memory, data memory, and register files. V_{THH} is 0.3V, V_{DDH} varies from 1V to 2V under the condition that V_{DDH} is twice V_{DDL} achieving a balance between the critical paths in the logic and memories. The capacity of the memory is 2kb (128words x 16b) for each of the instruction and data memories. The register files have 16 words based on a 2-read/1-write port cell. For high-speed operation, a voltage-controlled oscillator (VCO) is implemented on chip to generate up to a 1GHz clock. By checking 1/64 of the VCO output, the internal operation frequency can be known.

An ALU based on a 16b Brent-Kung binary adder as shown in Fig. 6.3.2 is employed to achieve the highest speed. The delay of this adder is determined by a path consisting of six gates, and is 1.5ns at 0.5V V_{DDL}. The ALU also includes a shifter and a bit operator.

Figure 6.3.3a is the block diagram of SRAMs. If zero V_{TH} is used for the SRAMs, leakage in the SRAM cells increases total power. Since memory core power is determined by leakage of dormant memory cells, a higher V_{DD} applied to the memory core only increases power consumption slightly. To assure stable operation, word and bit lines are also operated at V_{DDH}. Row decoders, however, are operated at V_{DDL} to decrease dynamic power since the decoder lines are highly capacitive. The row decoders take V_{DDL}, to drive the word lines whose swing is V_{DDH} using level-up converters.

The level-up converter utilizes a normally-on load as shown in Fig. 6.3.3b. This is twice as fast as the conventional cross-coupled level converters [3] because the decoding function is incorporated, and the slow cross-coupled configuration is eliminated. This type of normally-on load level converter, however, suffers from higher dissipation when an NMOS path turns on, and has a smaller operation margin due to the interaction of a load and discharging transistors. This is not an issue in the row decoders since only one decoder is activated. A replica-biasing scheme compensates for the fluctuation of PMOS and NMOS strength, and keeps the switching point in the middle of V_{DDL}.

At 400MHz, the processor consumes 3.5mW, but 400MHz is sometimes too slow so the processor supports an 800MHz mode. In the high-speed mode, 0.9V is applied to V_{DDL}, 1.8V is applied to V_{DDH}, and the operating power increases to 29mW. V_{DD} hops between two voltages depending on required performance. It has been shown that the higher performance is only required 6% of the time to encode a typical MPEG4 bitstream and the V_{DD}-hopping processor effectively reduces power consumption [2]. In both the 400MHz and 800MHz modes, memory read-out time is the critical path. Figure 6.3.4a shows the delay breakdowns in SRAM cycle time at the two hopping frequencies. It is understood from Fig. 6.3.4b that V_{DDH} should track the change of V_{DDL} as $V_{DDH} = 2 \times V_{DDL}$. V_{DDH} should not be fixed at 1.8V because the level-up converter fails to convert when V_{DDL} is 0.5V.

Figure 6.3.5 shows leakage characteristics of V_{DDL} when the clock is stopped. It should be noted that the leakage is a strong function of V_{DDL} at both room temperature and the high ambient temperature of 100°C. This is due to the Drain Induced Barrier Lowering (DIBL) effect. Without DIBL, the leakage should be constant even if V_{DD} is changed. To effectively control leakage, a V_{TH}-hopping scheme has been proposed [4], but it is not applicable to FD-SOI because backgate biasing that is basis of V_{TH}-hopping is not available. Thus only V_{DD}-hopping is considered to be an effective low-power technique for FD-SOI.

Figure 6.3.6 shows measured characteristics of operating frequency, total power and leakage power at room and high temperature. Total power (P_{TOTAL}) is a sum of static leakage power (P_{LEAK}) and dynamic power. Both P_{TOTAL} and P_{LEAK} show similar dependence on V_{DDL}. Thus, by changing only V_{DD} and not V_{TH}, it is possible to effectively scale the power consumption. This in turn demonstrates the effectiveness of the V_{DD}-hopping in sub-1V FD-SOI. Another interesting point is that the delay shows a positive temperature coefficient. In previous work circuit delay showed a negative temperature coefficient in sub-1V designs with a moderate V_{TH} [5]. The zero V_{TH} utilized on this processor causes the positive temperature coefficient.

Figure 6.3.7 shows the chip microphotograph. The logic part is synthesized with standard cell design methodology. The number of the gates in the cell library is 20. The size ratio of PMOS and NMOS in each gate is critically important in low-V_{TH} designs since on/off ratio is smaller compared to conventional designs. The small number of the gates makes it possible to carefully optimize transistor sizes for worst-case operation [6].

Acknowledgements
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[6] N. D. Minh, et al., "Compact yet High-Performance (CyHP) Library for Short Time-to-Market with New Technologies," *ASPDAC*, pp. 475-480, 2000.

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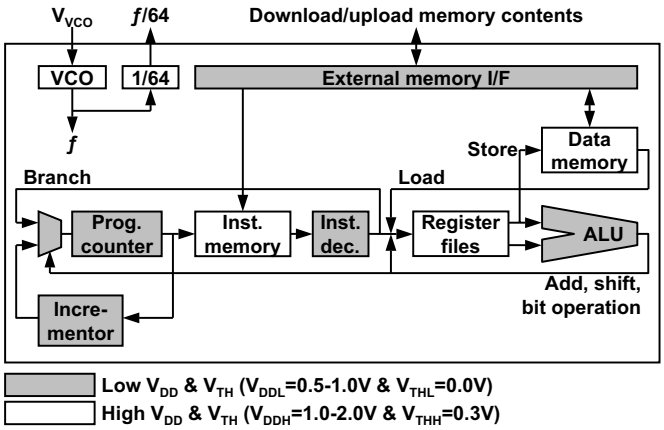

Figure 6.3.1: Block diagram of processor.

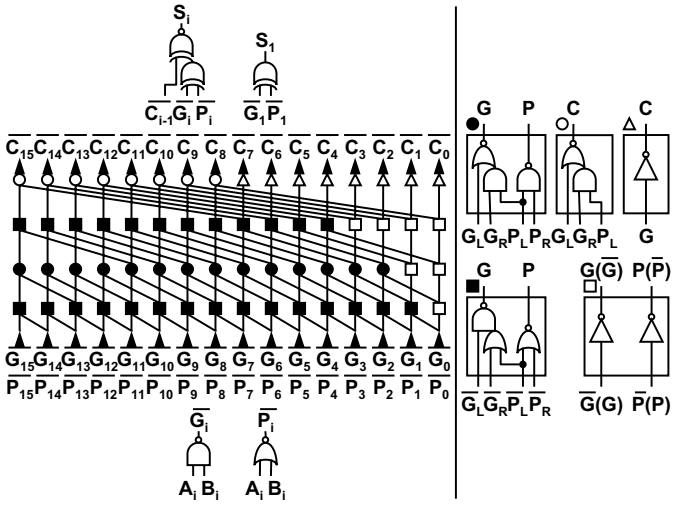

Figure 6.3.2: Schematic of adder in ALU.

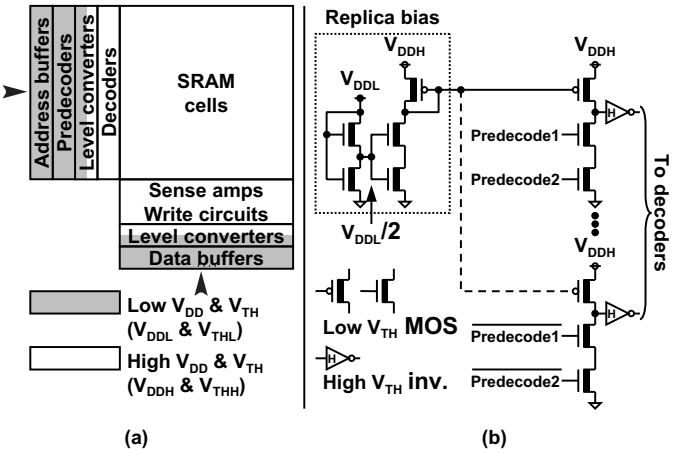

Figure 6.3.3: (a) Block diagram of SRAM. (b) Schematic of replica-biasing level-up converter.

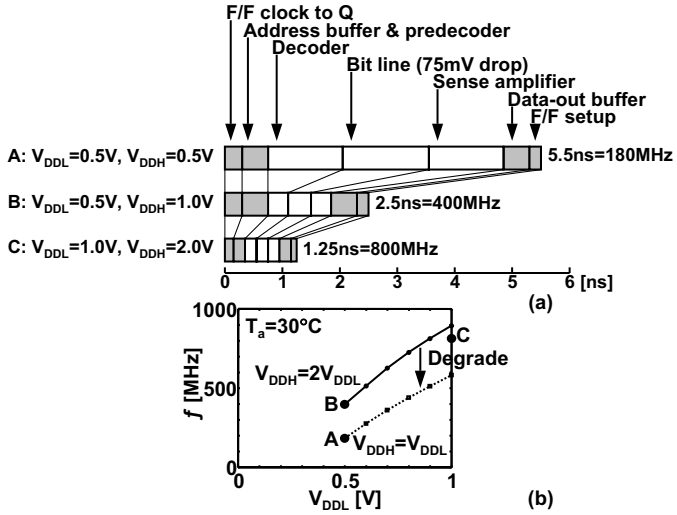

Figure 6.3.4: (a) Simulated delay breakdowns in SRAM cycle time. (b) Measured characteristics of operation frequency.

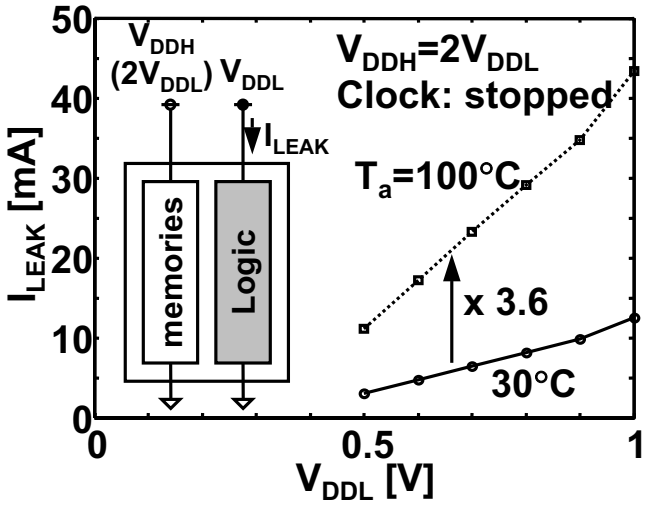

Figure 6.3.5: Measured leakage dependence on V_{DDL}.

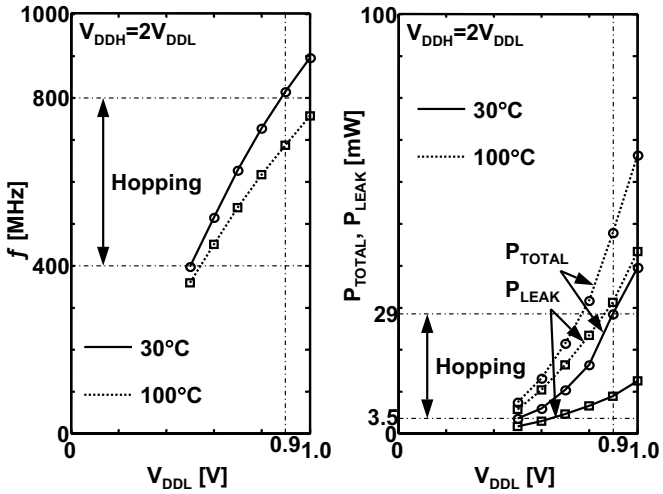

Figure 6.3.6: Measured characteristics of operation frequency, total power and leakage power at room and high temperatures.

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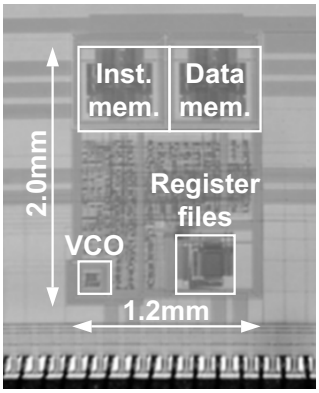

- 0.25-μm, 3-metal FD-SOI
- Dual-V_{TH}
  (V_{THL}=0.0V, V_{THH}=0.3V)

Figure 6.3.7: Chip micrograph.

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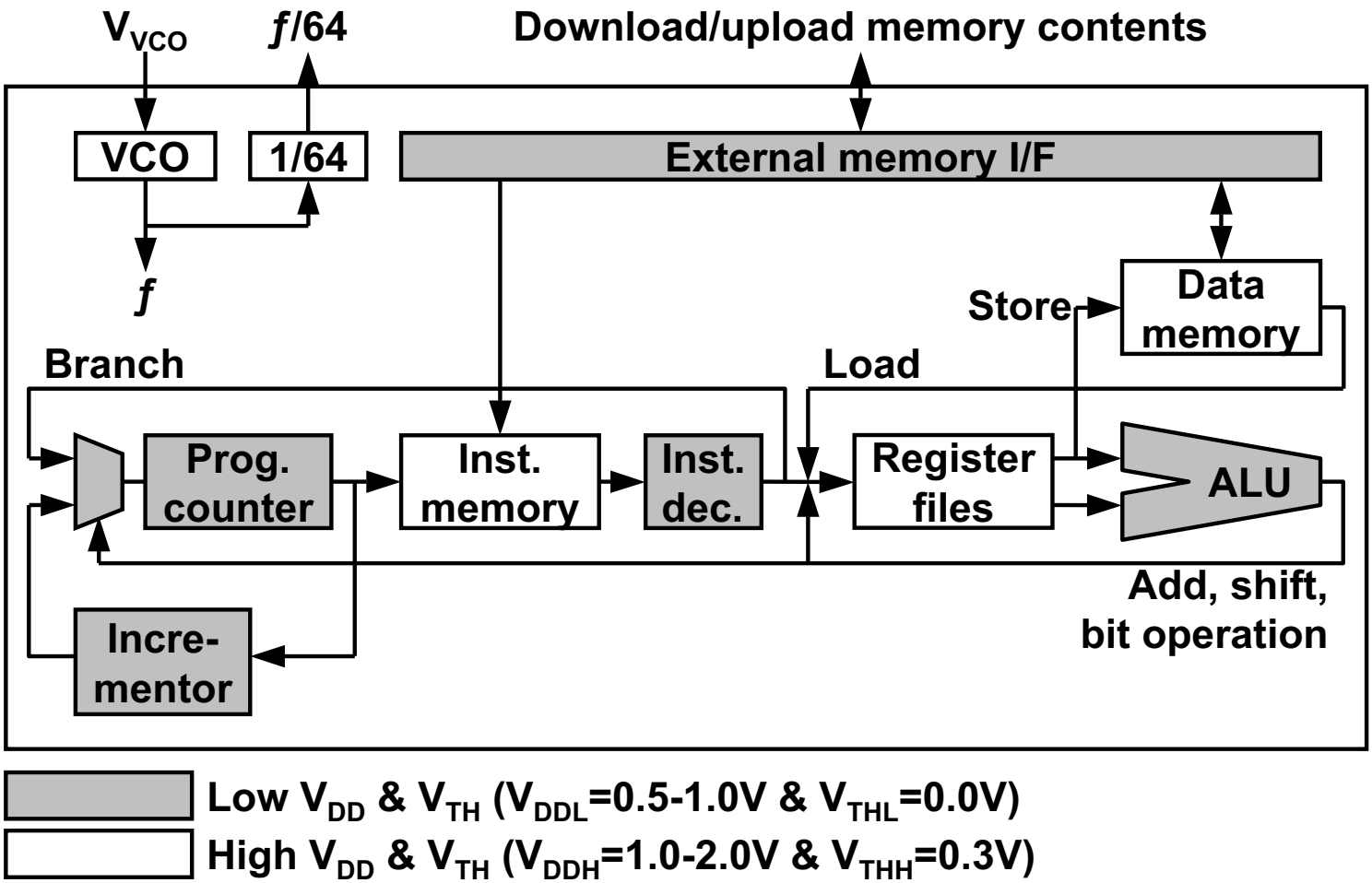

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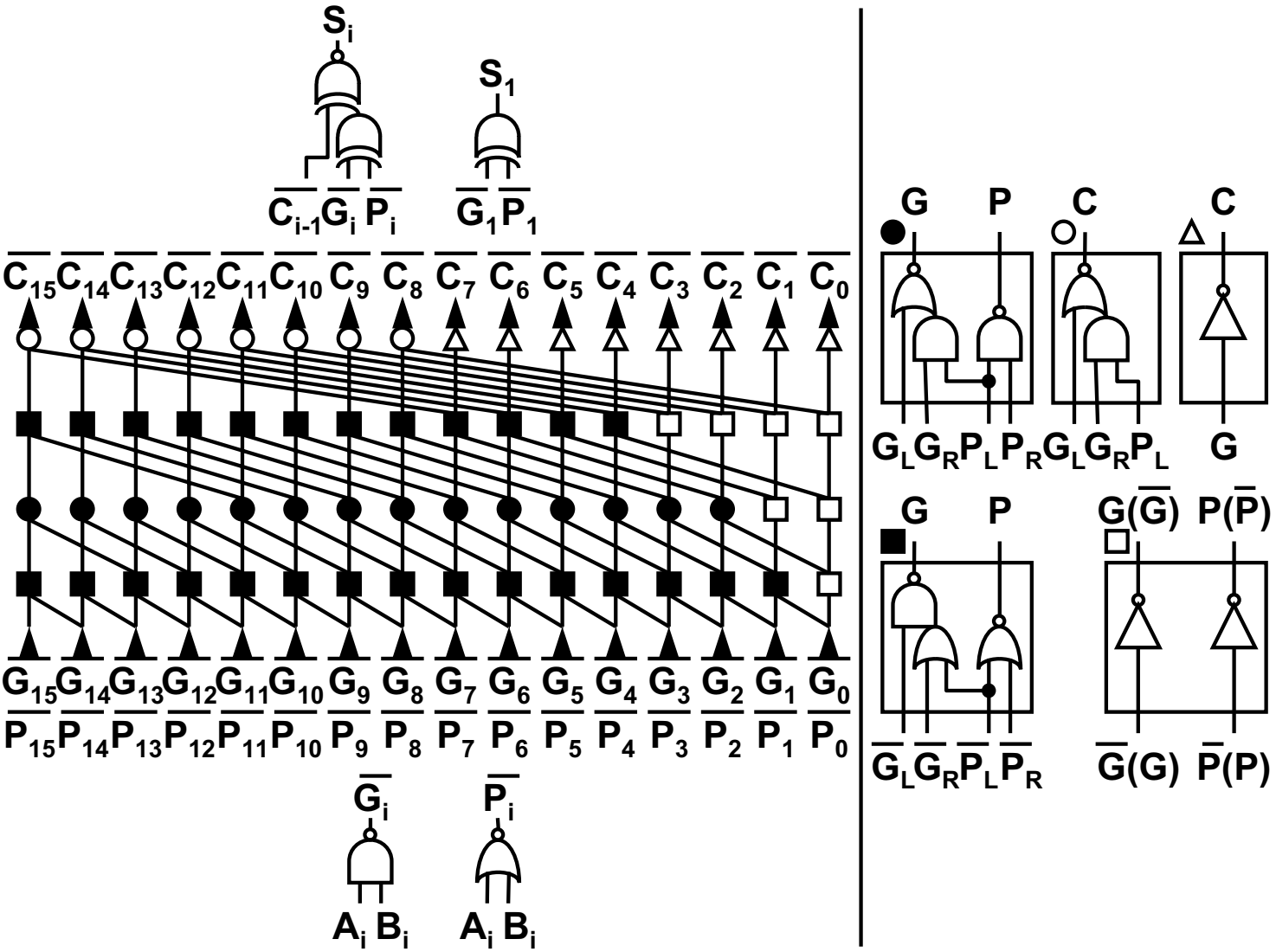

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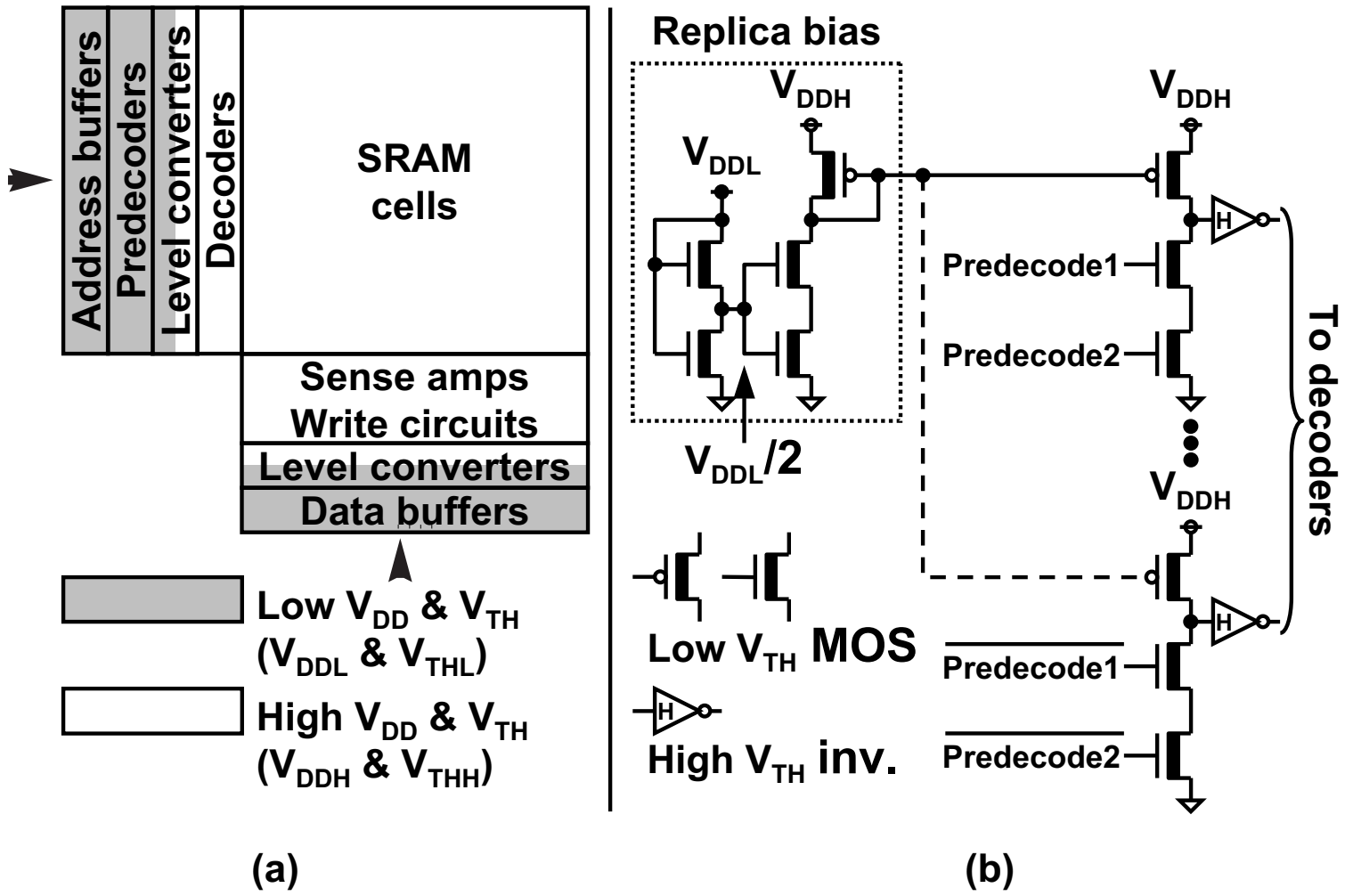

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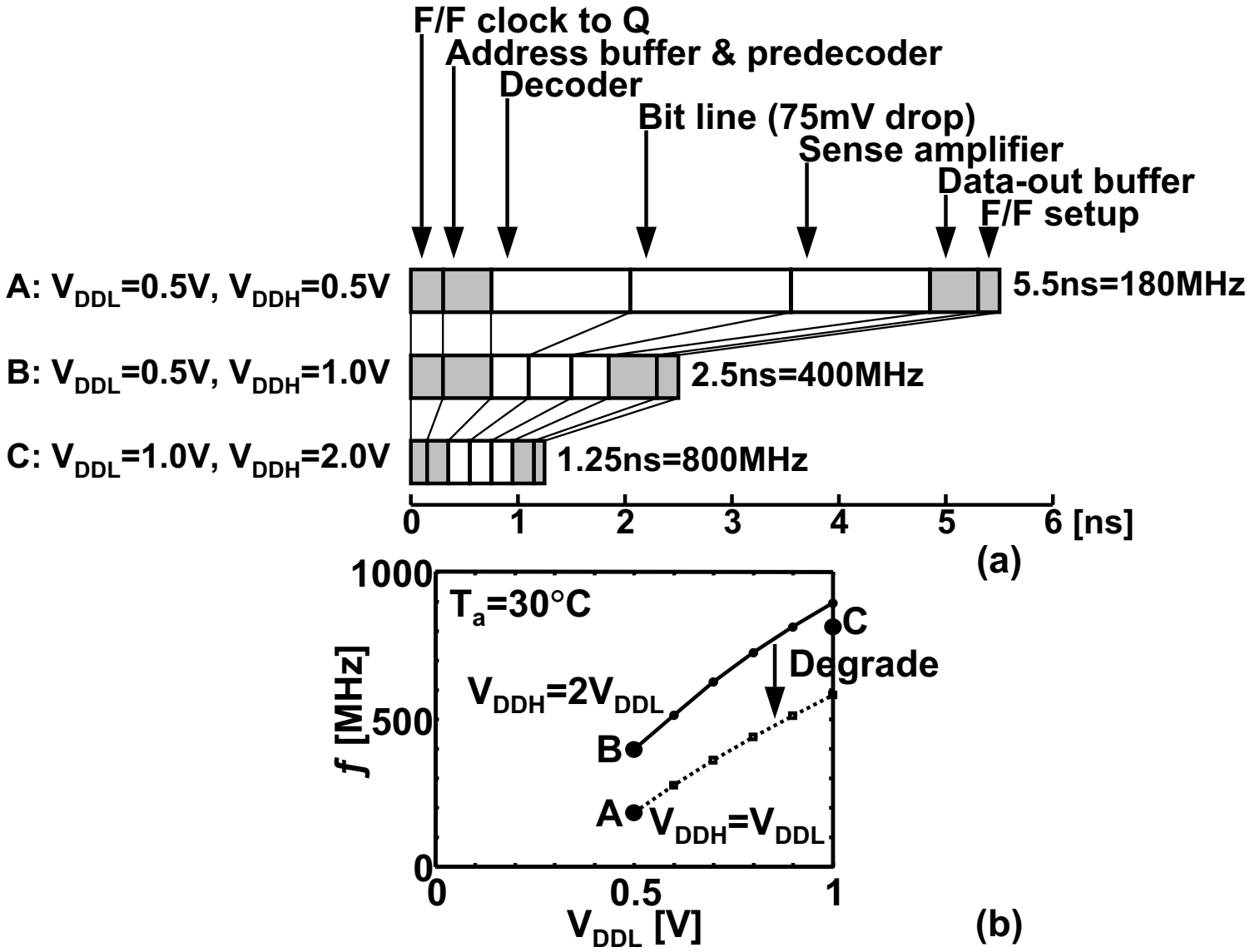

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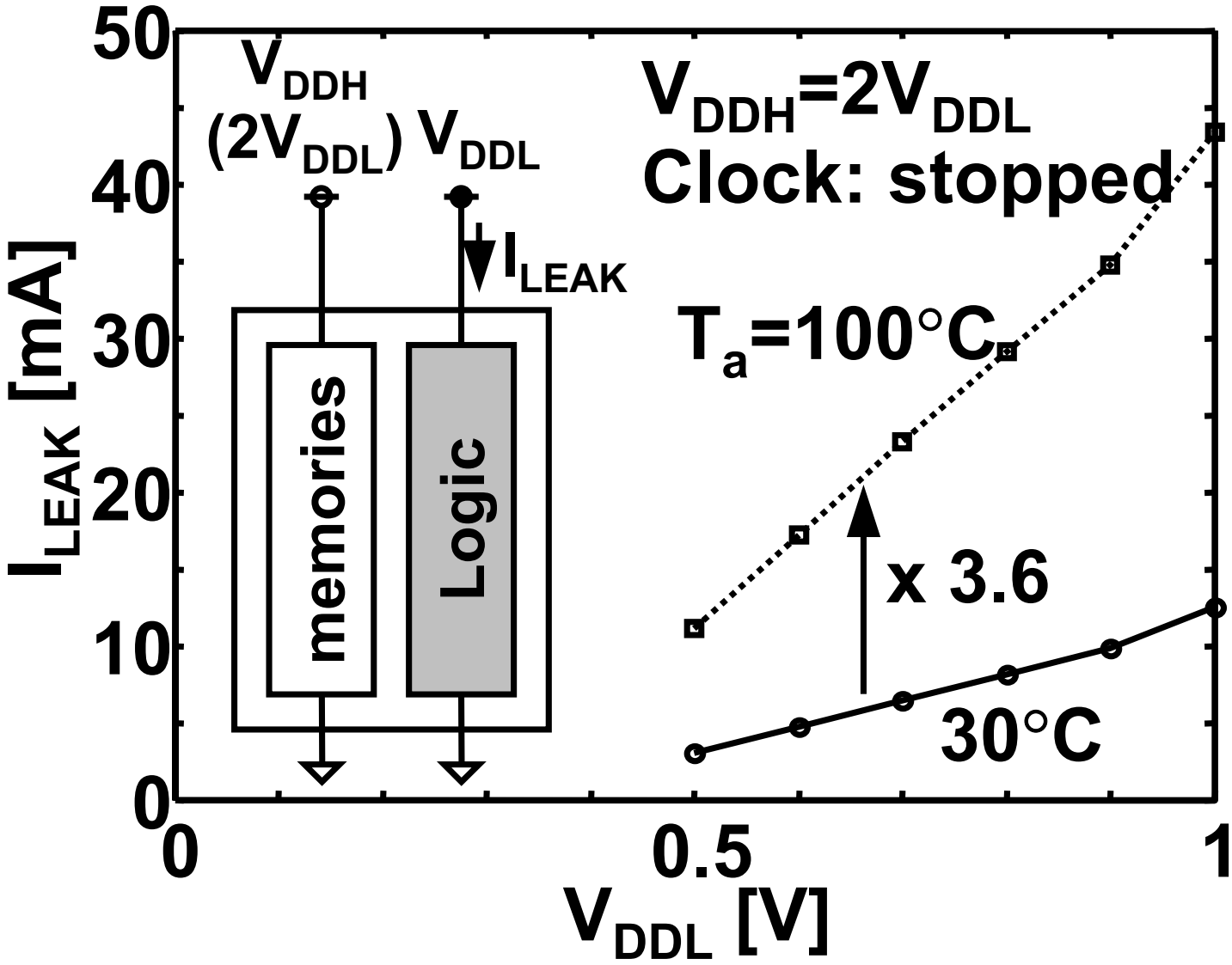
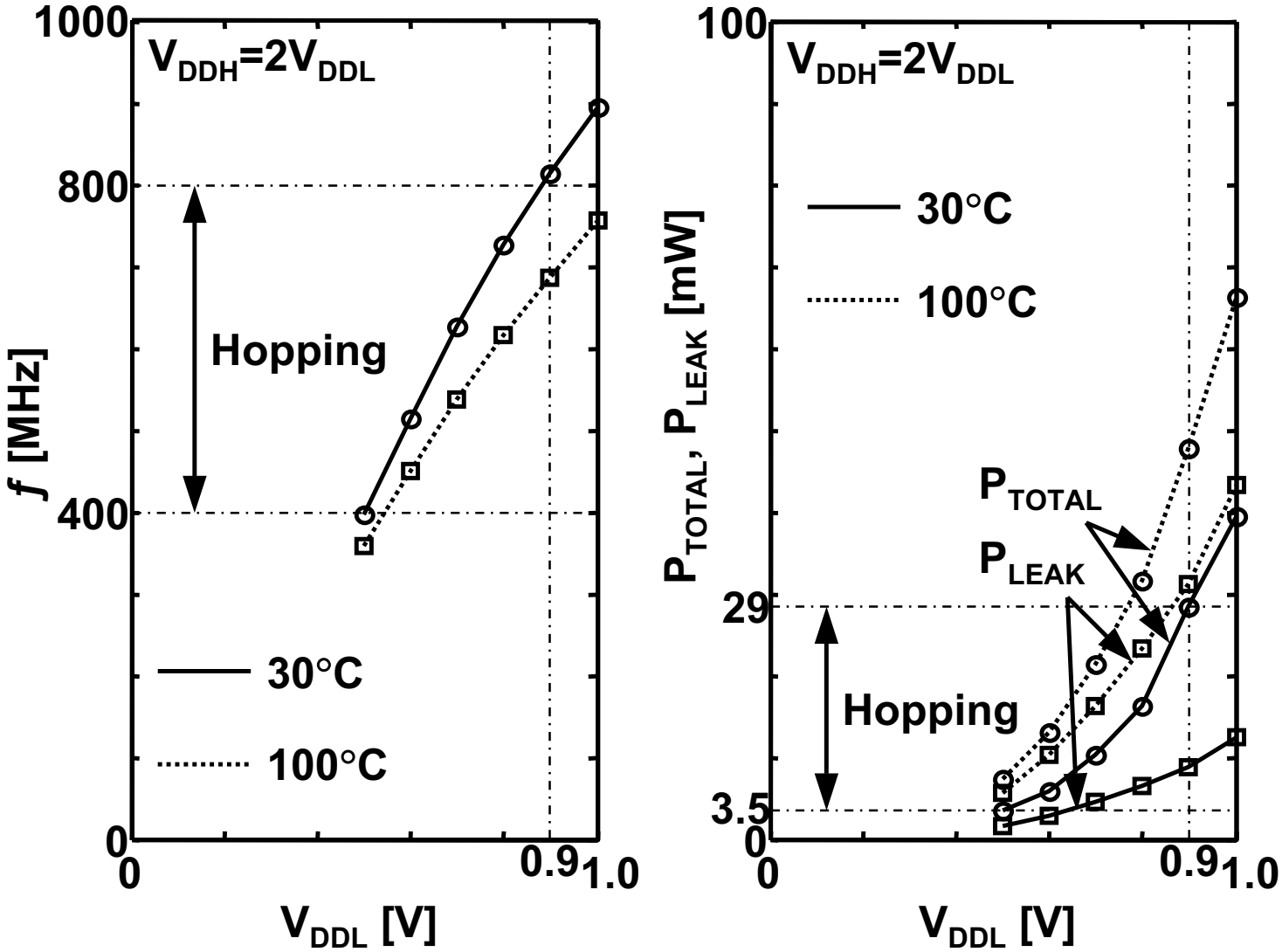


Figure 6.3.5: Measured leakage dependence on V_{DDL}.



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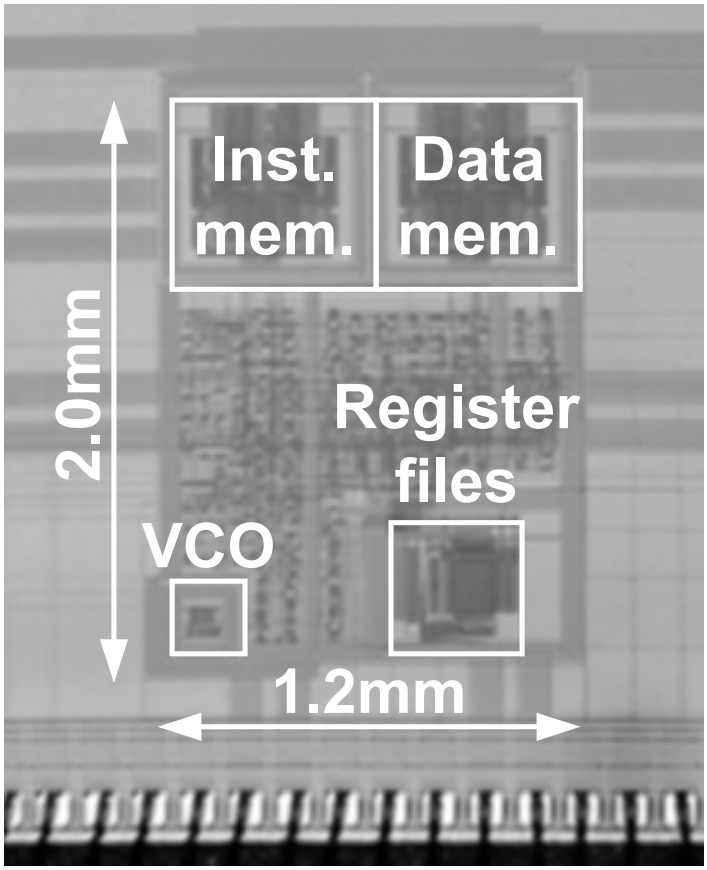

- 0.25-µm, 3-metal FD-SOI
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  (V_{THL}=0.0V, V_{THH}=0.3V)

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