#6.3

A 0.5-V, 400-MHz, V_{DD}-Hopping Processor with Zero-V_{TH} FD-SOI Technology

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Outline

- Introduction & motivation
- V_{DD}-hopping
- Circuit design
- Experimental results
- Summary

Introduction

- **Low-power processor**
  - **PDA, cell phone**
- **In 2013, V_{DD}=0.5V.**
- **Fully-depleted silicon-on-insulator (FD-SOI)**
  - **Steep s-factor (≈0.06V/dec)**
  - **Small junction capacitance**

Motivation

- Target: 0.5V, 400MHz as processor system
  - 0.5V, 100MHz FD-SOI adder was reported*.
- 0.5V V_{DD} & zero V_{TH} in logic part
  - V_{TH} must be <20% of V_{DD} for high speed.
- Higher V_{DD} & V_{TH} for memories
  - To suppress cell leak
- 800MHz (x2 speed) is also possible.
  - V_{DD}-hopping

* T. Douseki, et al., Symp. VLSI Circ., pp. 6-9, 2002.

V_{DD}-hopping

- Introduction & motivation
- **V_{DD}-hopping**
- Circuit design
- Experimental results
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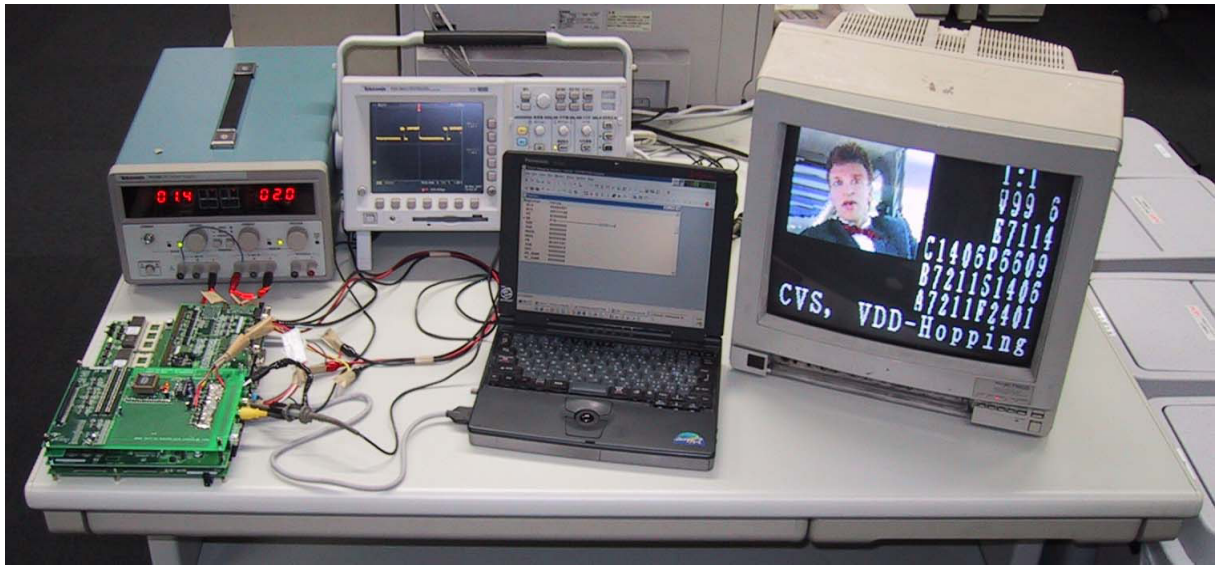
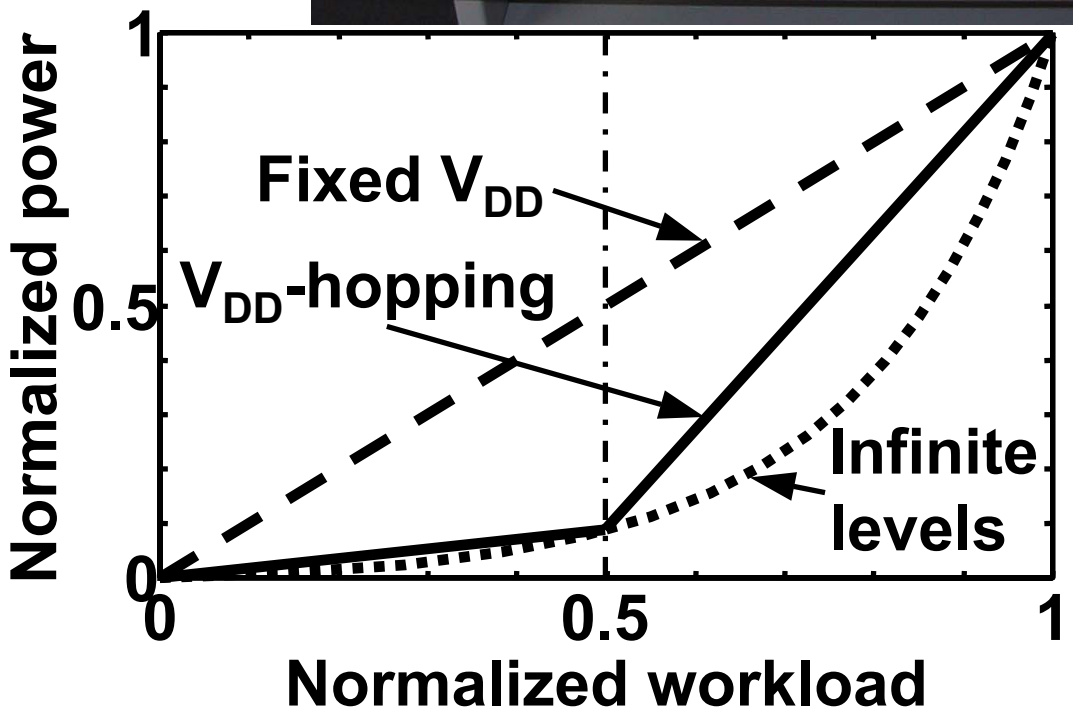
V_{DD}-hopping in MPEG4 system





- f for low V_{DD} & $2f$ for high V_{DD}
- Suitable for multimedia application
- 75% power save in MPEG4 encoding

V_{DD}-hopping in leaky environment

- V_{DD}-hopping*
  - –Dynamic power management
  - –f for low V_{DD} & $2f$ for high V_{DD}
- V_{TH}-hopping**
  - –f for high V_{TH} & $2f$ for low V_{TH} with body bias
  - –Cannot be applied to FD-SOI.

- With help of DIBL, V_{DD}-hopping is effective even in leakage-dominant environment.

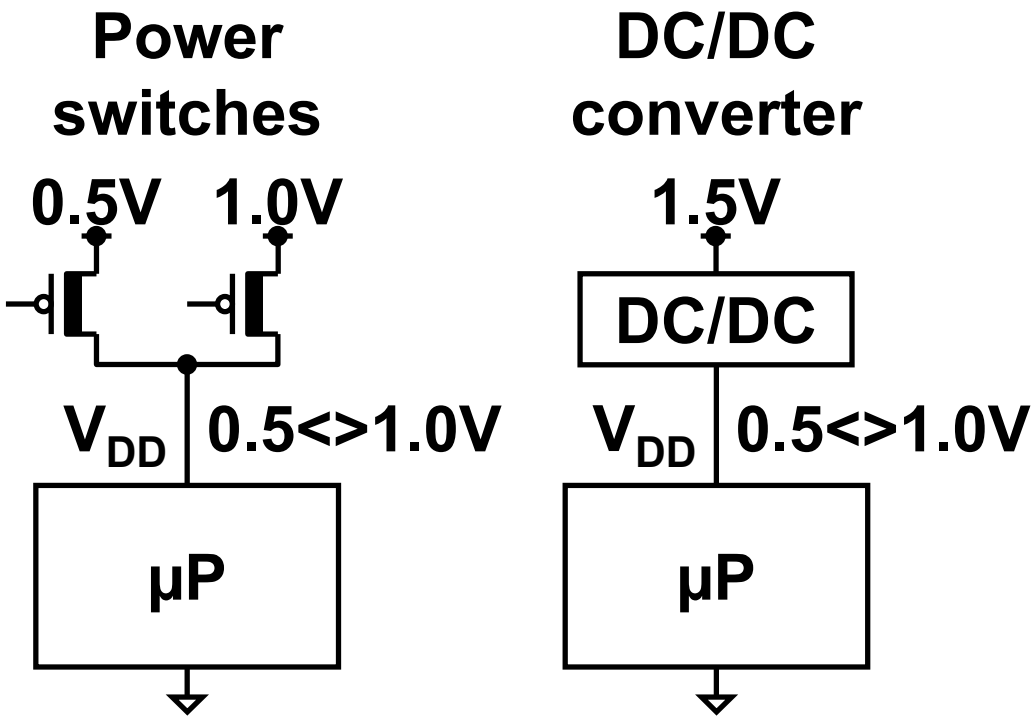
* H. Kawaguchi, et al., IEICE T. Elec., vol. E85-C, no. 2, pp. 263-271, 2002.

** K. Nose, et al., IEEE JSSC, vol. 37, no. 3, pp. 413-419, 2002.

V_{DD}-hopping mechanism

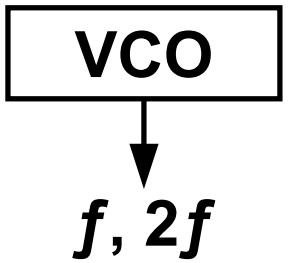
- At least, 2 kinds of V_{DD}s & fs must be provided.

V_{DD} (power supply)



- V_{DD} is externally changed.
- In terms of transient time, on-chip device is better.

f (frequency)



- VCO can output f & $2f$.
- frequency selector is implemented.

Circuit design

- Introduction & motivation
- V_{DD}-hopping
- **Circuit design**
- Experimental results
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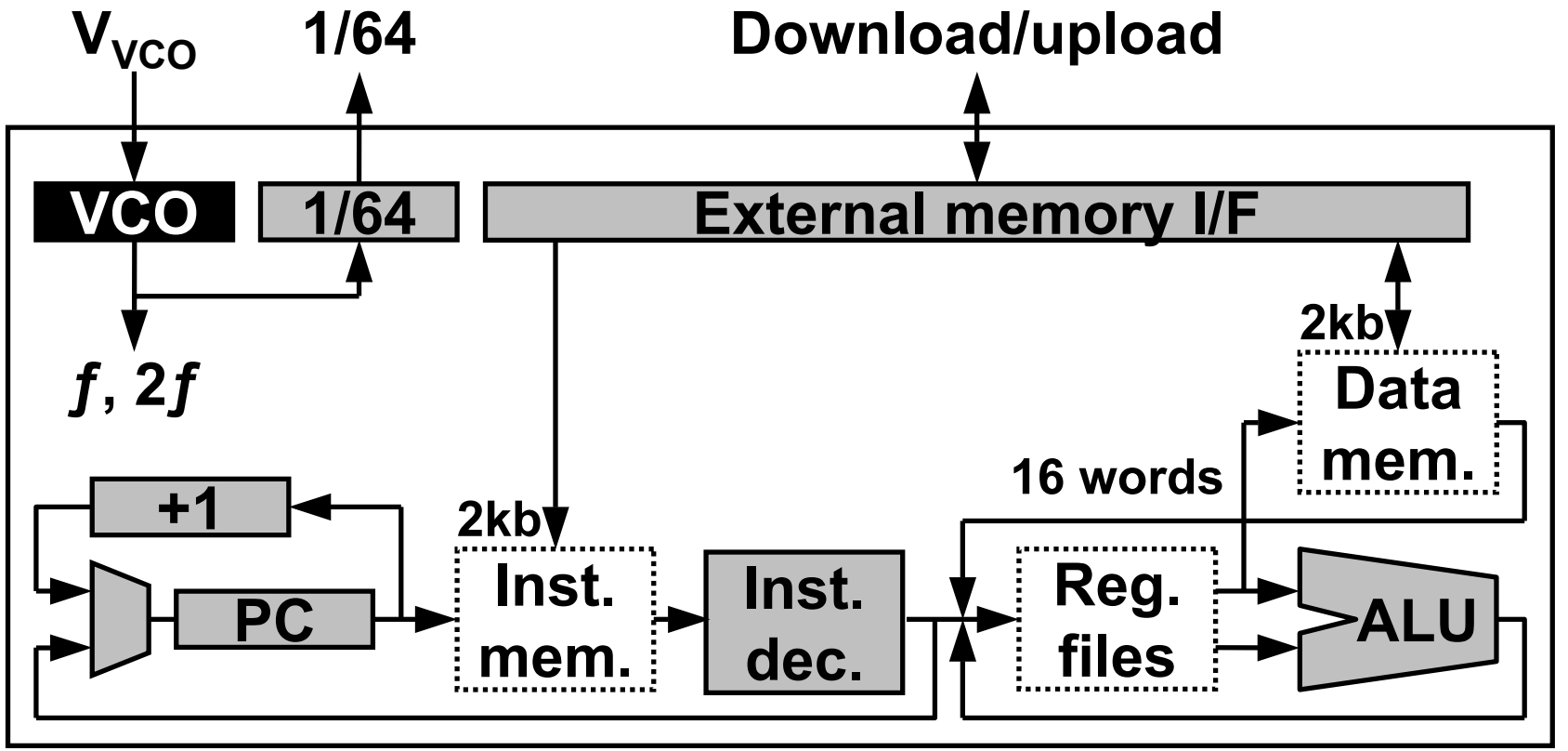
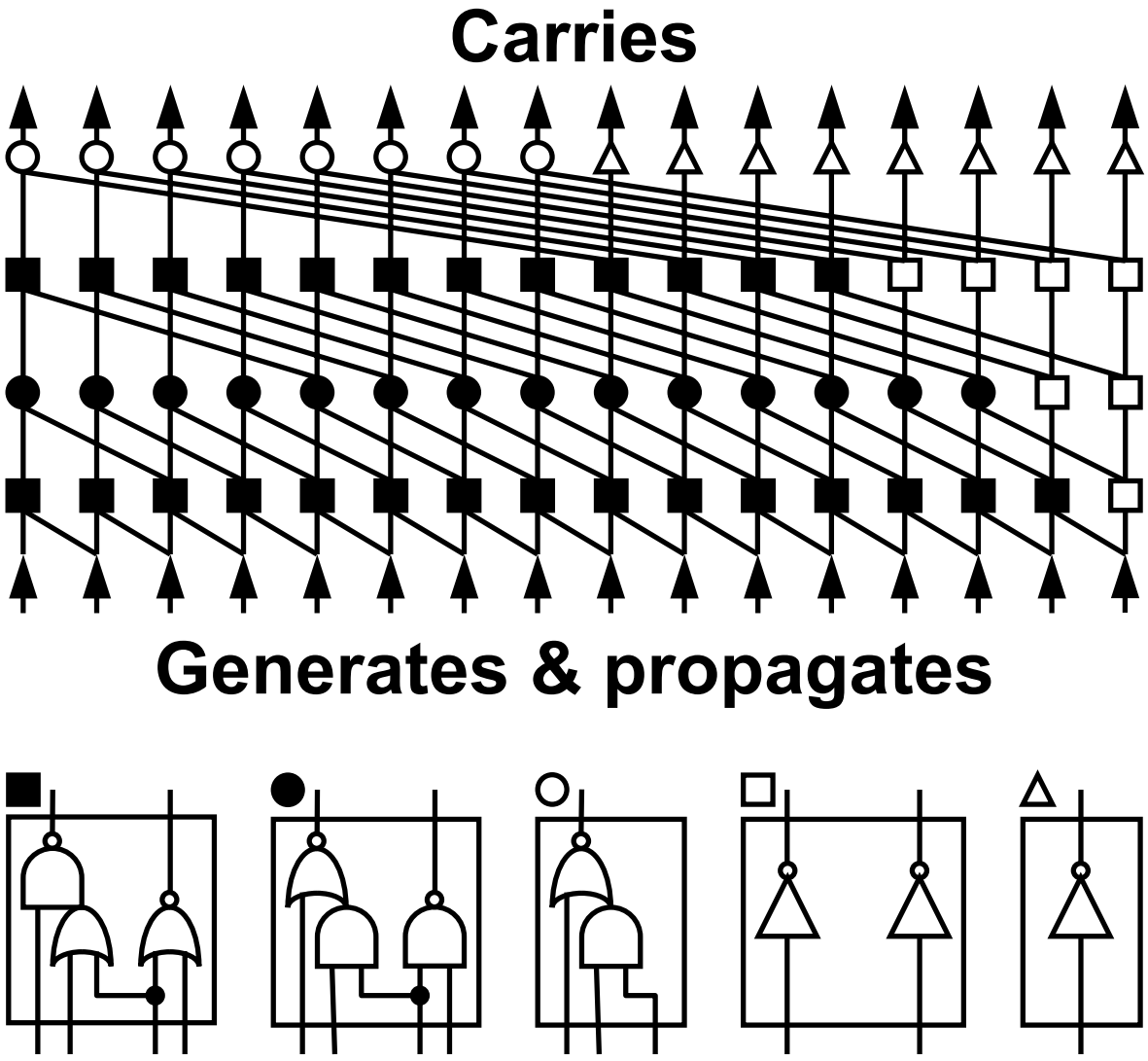
Block diagram

- Dual V_{DD} & V_{TH} scheme
  - –Low V_{DD} & V_{TH} for logic, high V_{DD} & V_{TH} for memories
- $V_{DDH}=2V_{DDL}$.

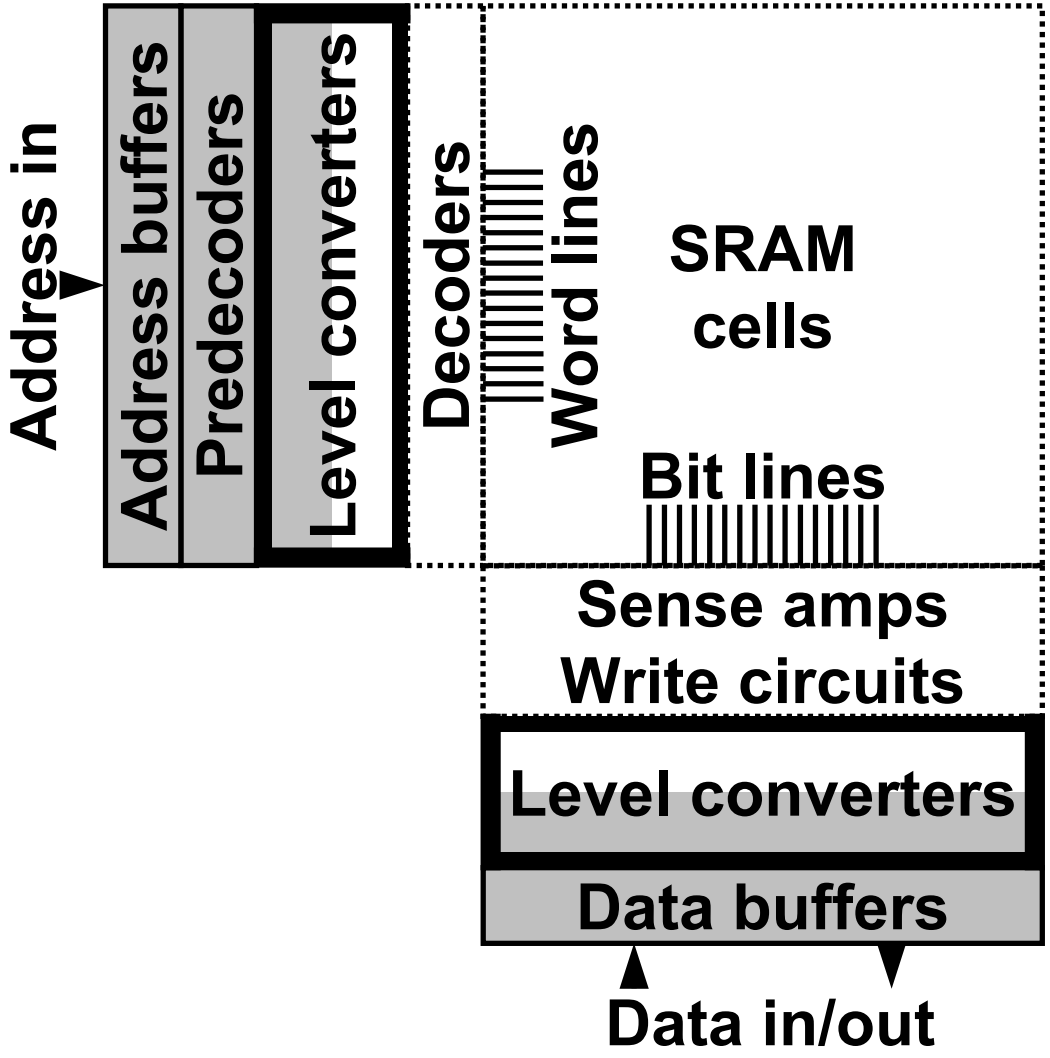


16bit Kogge-Stone adder in ALU



- Critical path in logic part
- 6-gate path
- 1.5ns w/o F/Fs at 0.5V V_{DDL}
- 2.1ns with F/Fs
- ALU also has shifter & bit operator.

SRAM block diagram



- High V_{DD} & V_{TH} cells
  - To suppress cell leak
- High V_{DD} WL & BL
- Low V_{DD} buffers & predecoder

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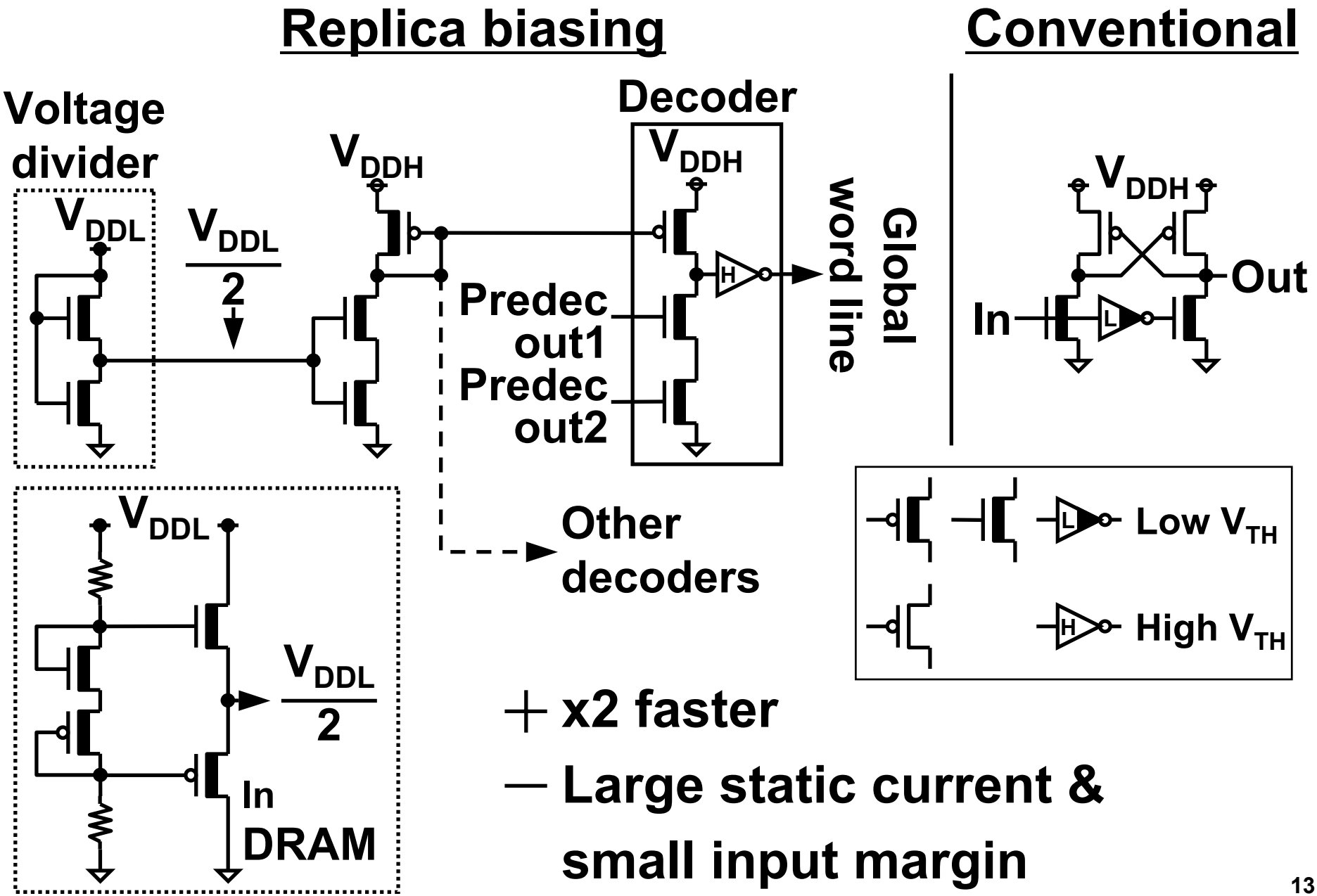
- Level-up converters are needed.

Low V_{DD} & V_{TH} (V_{DDL} & V_{THL})

High V_{DD} & V_{TH} (V_{DDH} & V_{THH})

Replica-biasing level-up converter



+ x2 faster

— Large static current & small input margin

Experimental results

- Introduction & motivation
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- **Experimental results**
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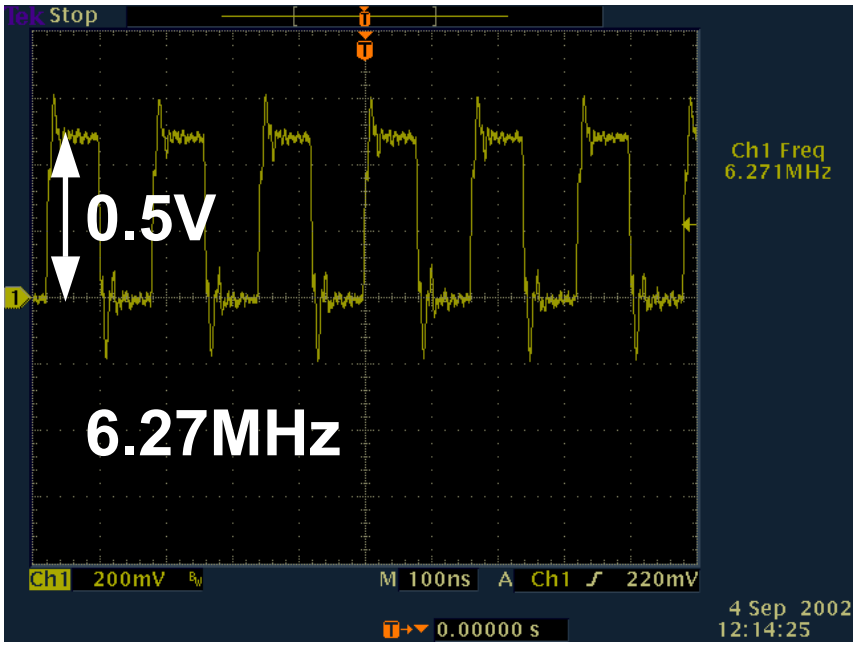
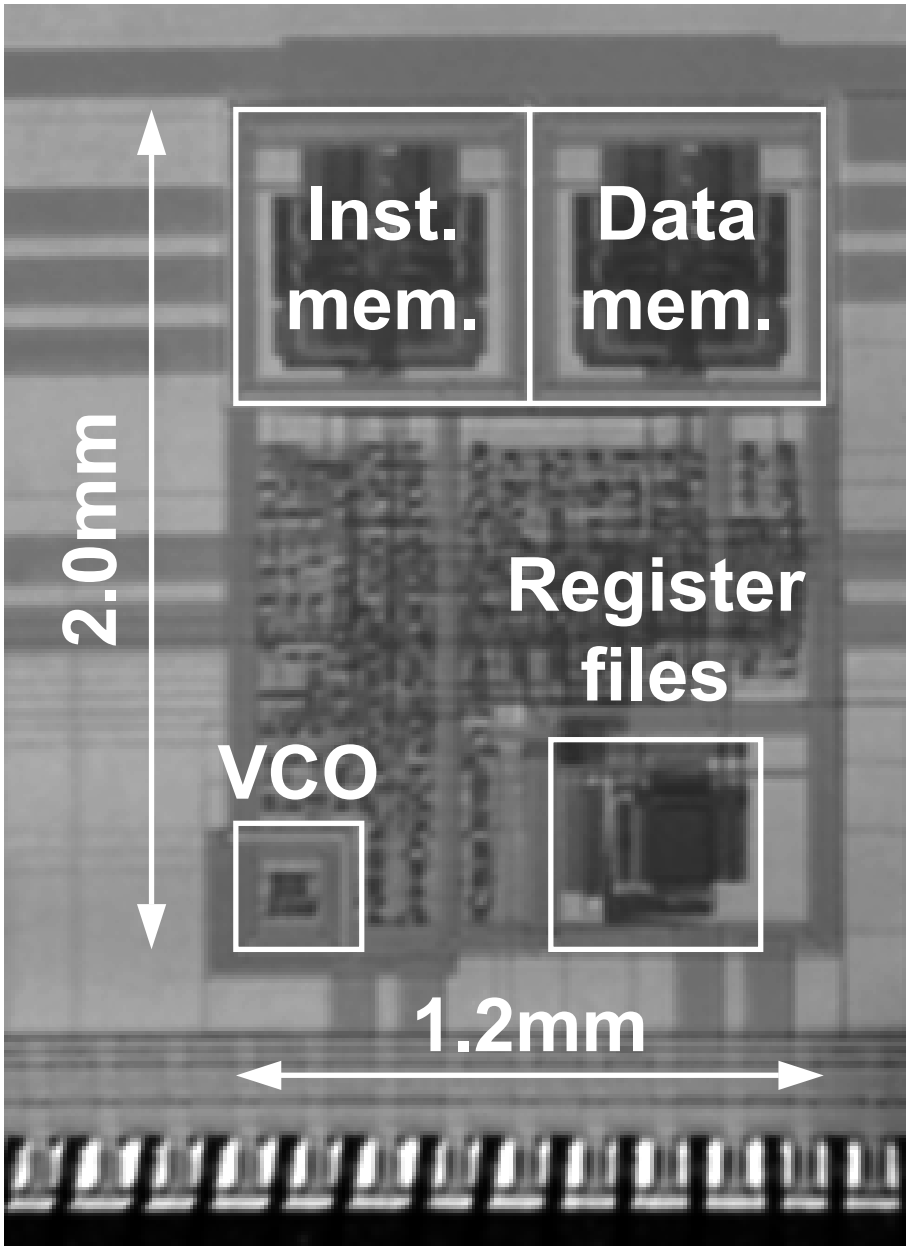
Measurement setup

- LSI tester
- Slow testing
  - –External memory I/F



- VCO output
  - –1/64 of internal operation *f*
- 0.5V, 400MHz operation

Chip micrograph



- 0.25µm, 3-metal FD-SOI
- Dual-V_{TH} (V_{THL}=0.0V & V_{THH}=0.3V)
- 2000 gates in logic part
- Memories account for 85% of transistor count.

Compact cell library

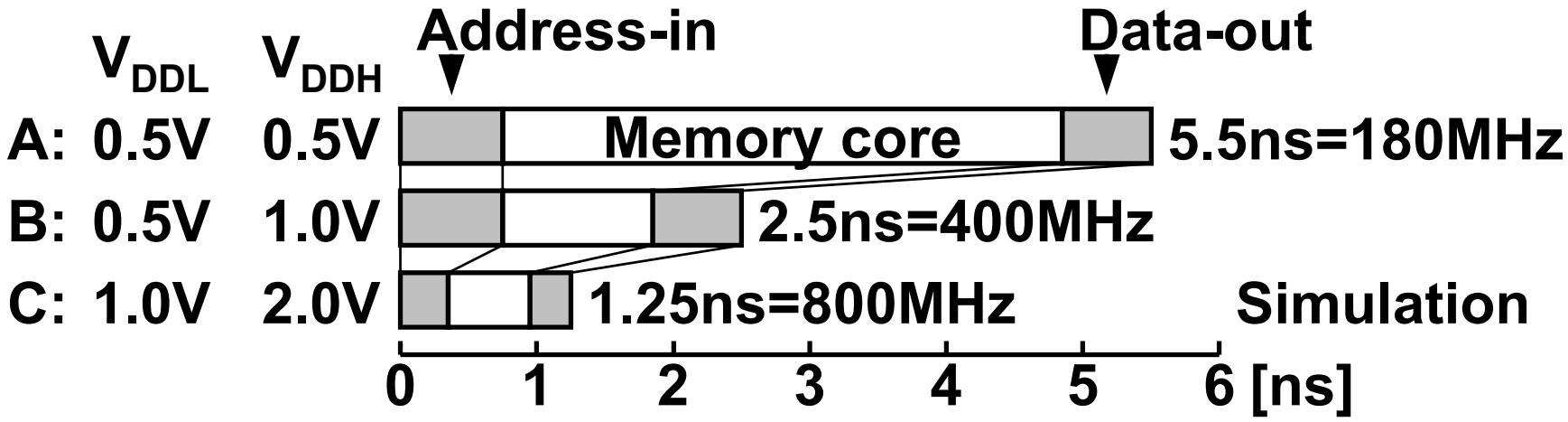
- Small number of logic gates doesn't degrade performance much*.

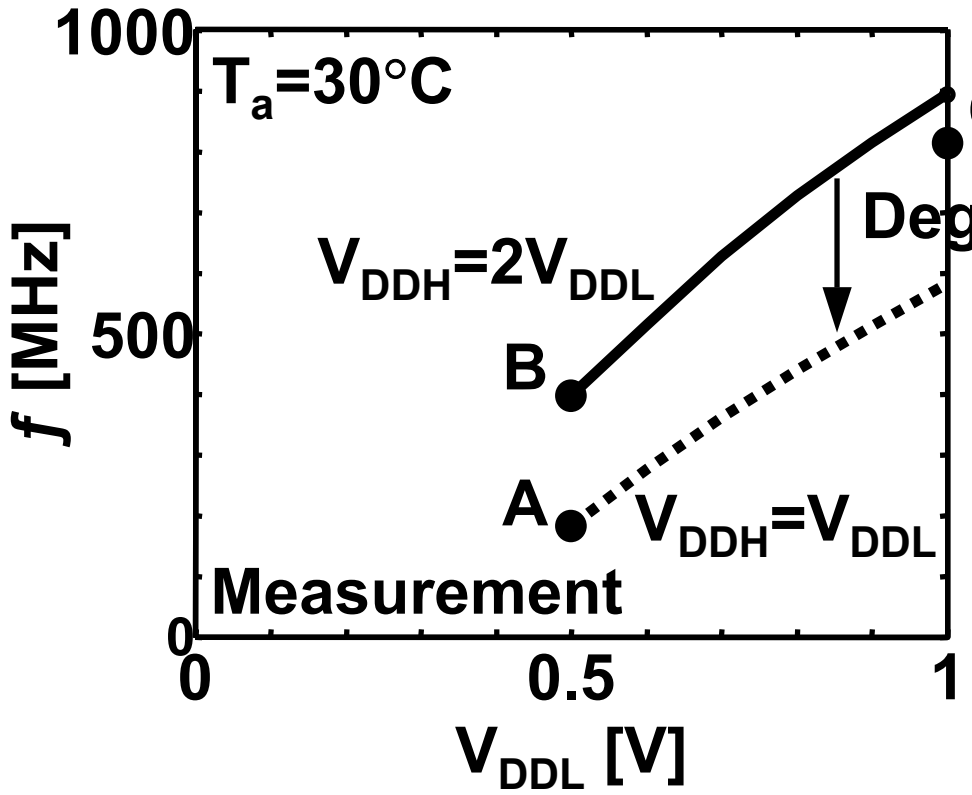
- Only 20 kinds of logic gates
  - –Detailed design tuning is possible.
  - –INVx3, NANDx3, NORx3, AOIx2, OAIx2, EXOR, EXNOR, MUXx2, DFFx2, CLKBUF

- On 2NOR, I_{ON_P}/I_{OFF_N}=33 when V_{DDL}=0.5V.
  - –Sizing is critically important.

* N. D. Minh, et al., ASPDAC, pp. 475-480, 2000.

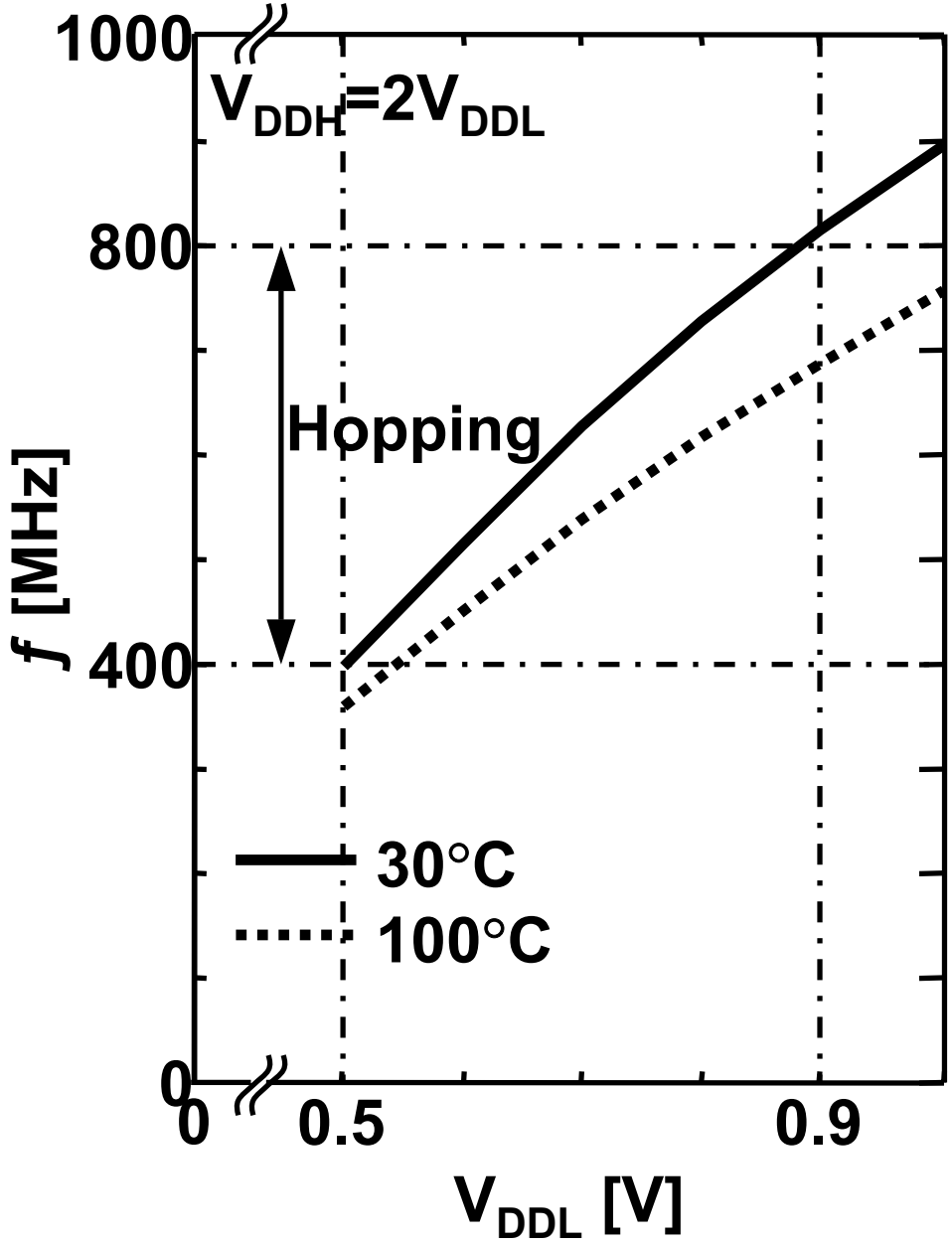
SRAM delay breakdowns - critical path





- V_{DDH} should be 2V_{DDL}.
  - –For high speed
- V_{DDH} should not be 2.0V.
  - –Level-up converter fails when V_{DDL}=0.5V.

Operation frequency - measurement



- 0.5V-400MHz & 0.9V-800MHz
- In sub-1V with moderate V_{TH}, delay has negative temperature coefficient*.

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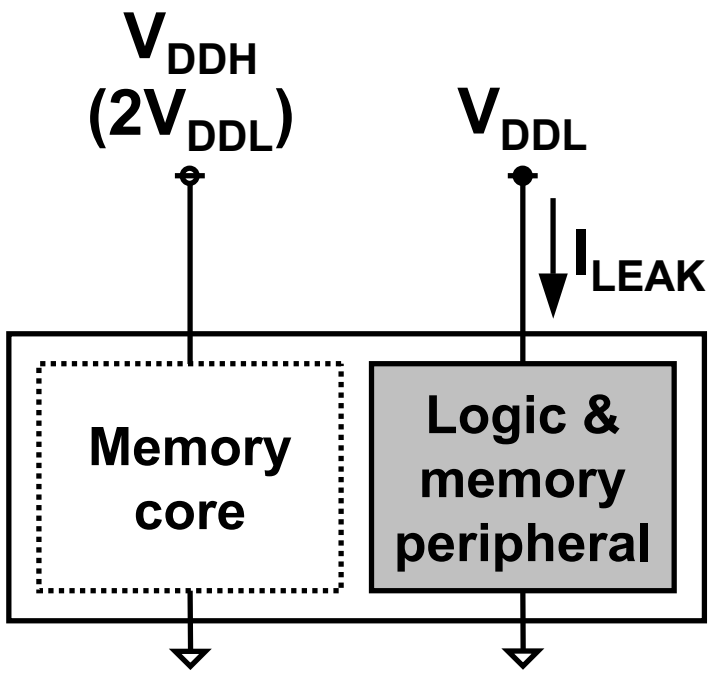
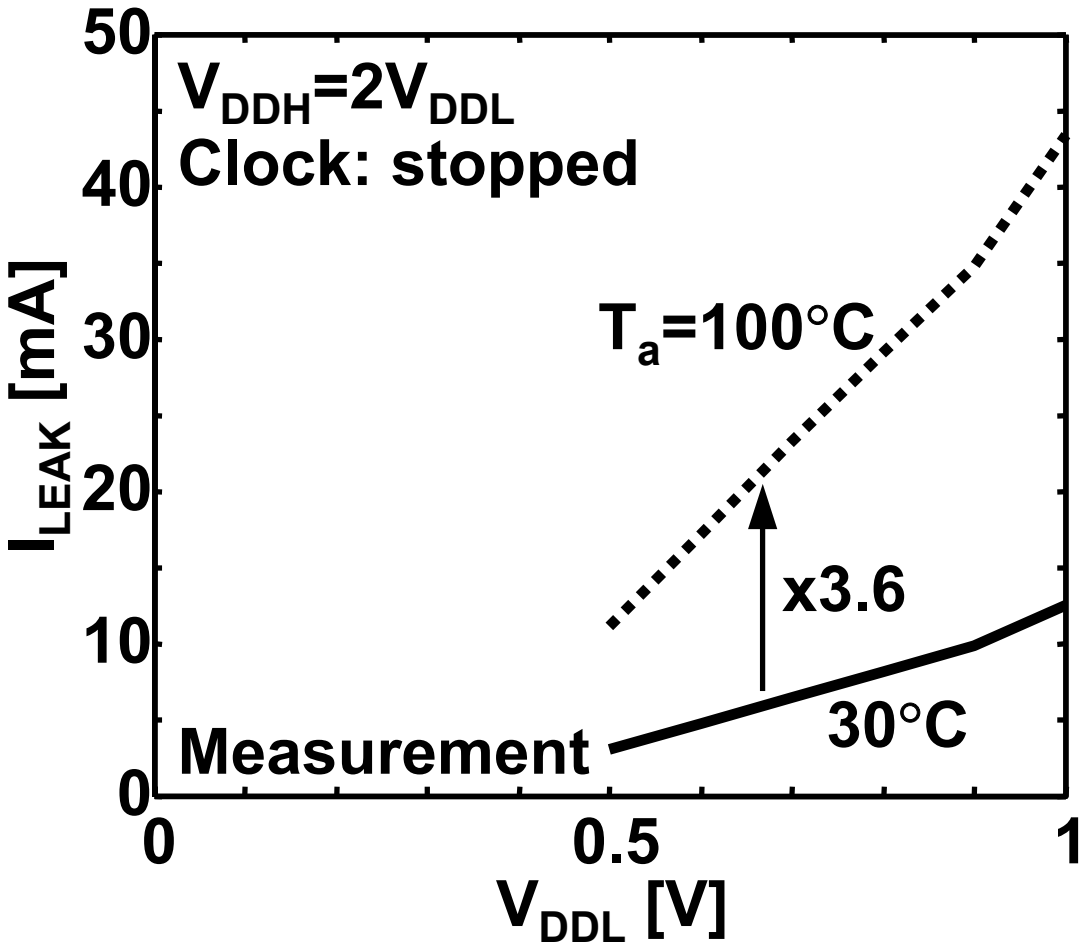
- However, with 0 V_{TH}, positive temperature dependence is observed.

* K. Kanda, et al., IEEE JSSC, vol. 36, no. 10, pp. 1559-1564, 2001.

Leakage dependence on V_{DDL}





- Leakage is strong function of V_{DDL}.

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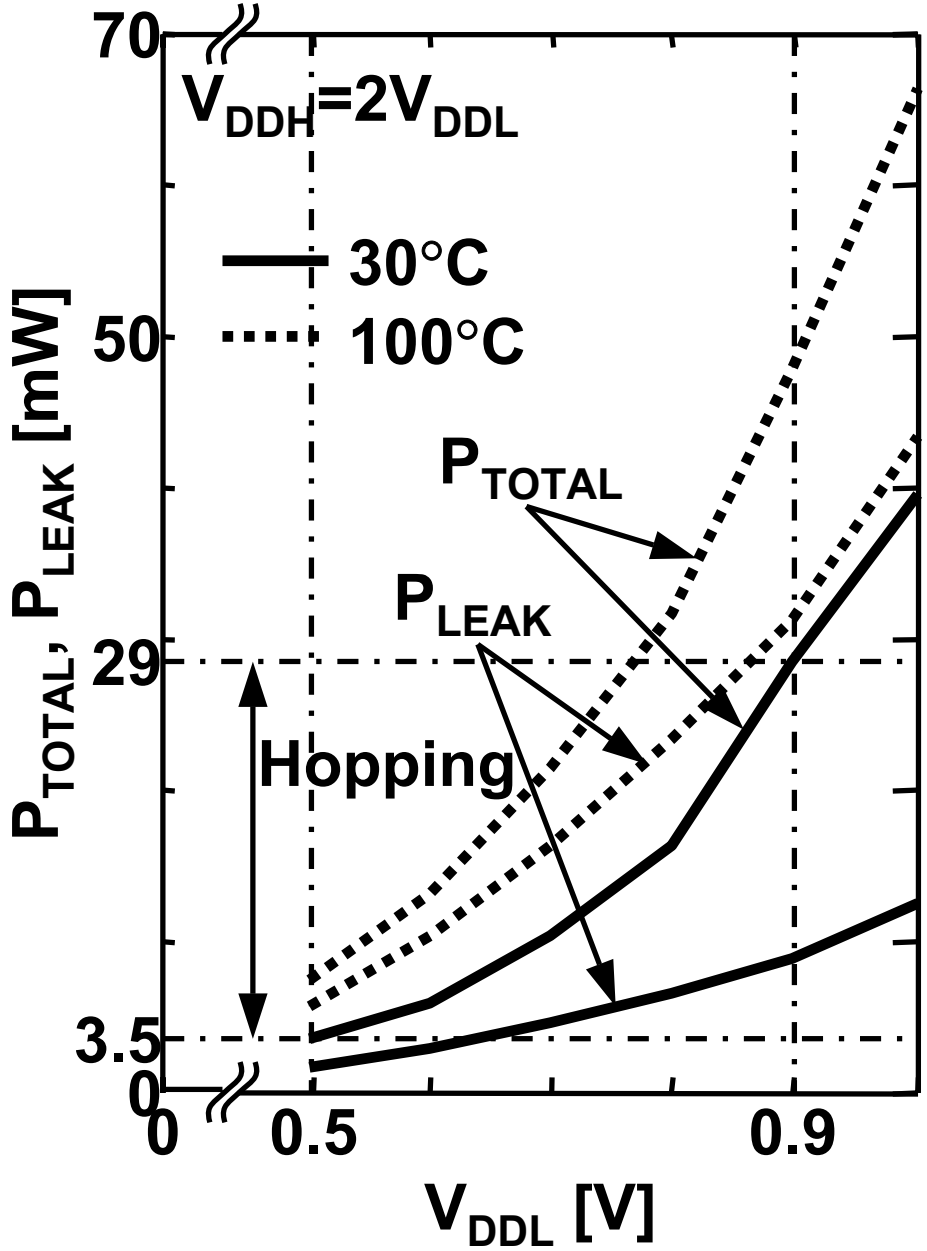
- Drain induced barrier lowering (DIBL) effect

Power - measurement



- P_{TOTAL} & P_{LEAK}
  - –Similar dependence
- Possible to scale power by changing only V_{DDL}
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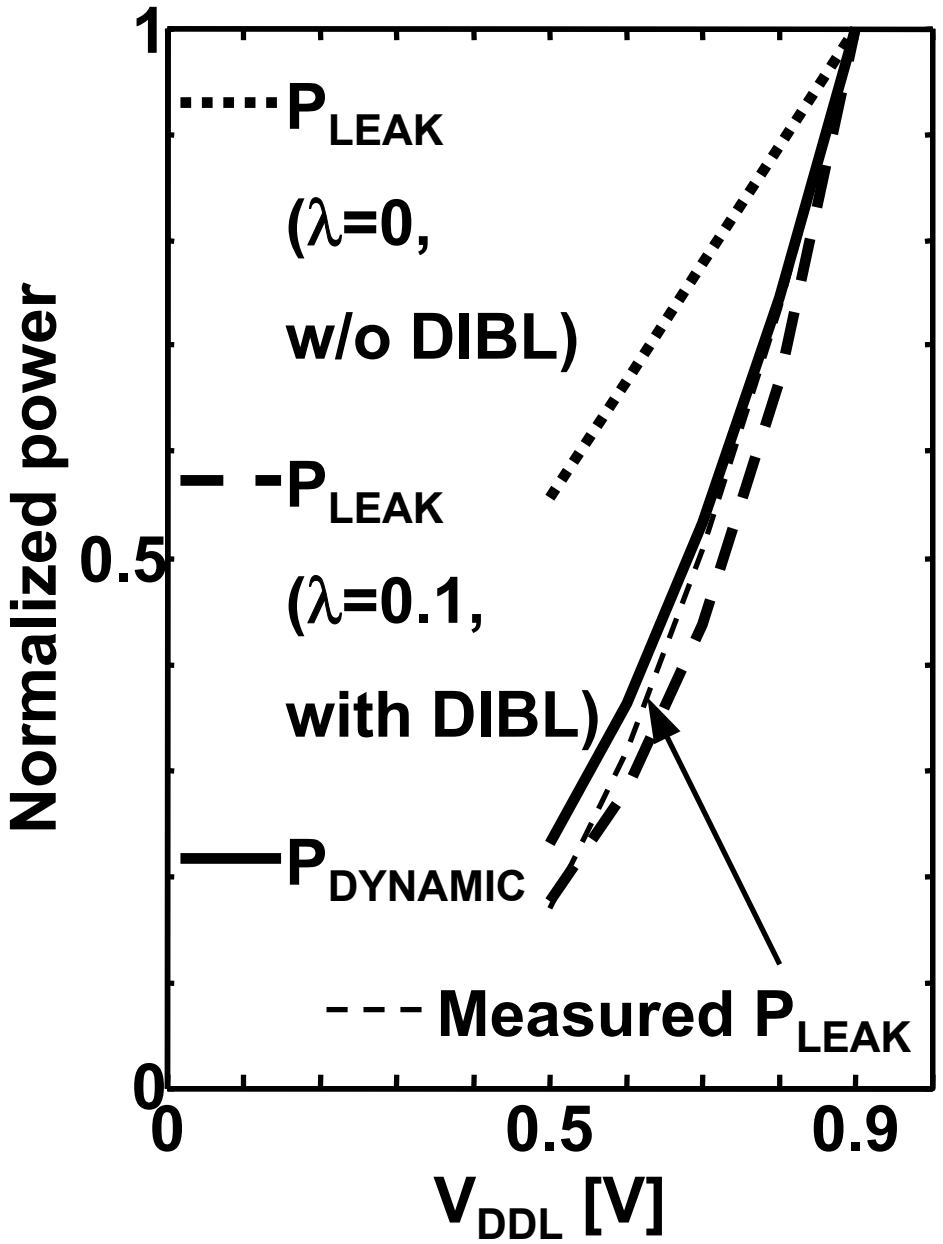
- V_{DD}-hopping is effective even in sub-1V FD-SOI.

Power scaling in V_{DD}-hopping - analysis



$$P_{LEAK} \propto V_{DDL} \cdot I_0 \cdot 10^{-\frac{V_{TH}-\lambda \cdot V_{DDL}}{s}}$$

$$\propto V_{DDL} \cdot 10^{\frac{\lambda \cdot V_{DDL}}{s}}$$

$$P_{DYNAMIC} \propto f \cdot V_{DDL}^2$$

$$\propto \frac{(V_{DDL} - V_{THL})^{\alpha}}{V_{DDL}} \cdot V_{DDL}^2$$

$$\propto V_{DDL}^{2.5}$$

V_{THL}=0

λ=0 or 0.1 (DIBL coefficient)

s=0.08 (s-factor)

α=1.5

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Summary

- 0.5V, 400MHz, 3.5mW, FD-SOI processor with compact cell library

- Design methodology in 0.5V generation
  - Zero V_{TH}
  - Dual V_{DD} & V_{TH}, low for logic & high for memory
  - Replica-biasing level converter
  - With help of DIBL, V_{DD}-hopping is effective even in leakage-dominant environment.