#6.3

A 0.5-V, 400-MHz, $V_{DD}$-Hopping Processor with Zero-$V_{TH}$ FD-SOI Technology

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Outline

• Introduction & motivation

• $V_{DD}$-hopping

• Circuit design

• Experimental results

• Summary
Introduction

• Low-power processor
  – PDA, cell phone

• In 2013, $V_{DD} = 0.5V$.

• Fully-depleted silicon-on-insulator (FD-SOI)
  – Steep s-factor ($\approx 0.06V/\text{dec}$)
  – Small junction capacitance
Motivation

• Target: 0.5V, 400MHz as processor system
  – 0.5V, 100MHz FD-SOI adder was reported*.

• 0.5V $V_{DD}$ & zero $V_{TH}$ in logic part
  – $V_{TH}$ must be $<20\%$ of $V_{DD}$ for high speed.

• Higher $V_{DD}$ & $V_{TH}$ for memories
  – To suppress cell leak

• 800MHz (x2 speed) is also possible.
  – $V_{DD}$-hopping

V_{DD}-hopping

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$V_{DD}$-hopping in MPEG4 system

- $f$ for low $V_{DD}$ & $2f$ for high $V_{DD}$
- Suitable for multimedia application
- 75% power save in MPEG4 encoding
V_{DD}-hopping in leaky environment

• V_{DD}-hopping*
  – Dynamic power management
  – \( f \) for low V_{DD} & \( 2f \) for high V_{DD}

• V_{TH}-hopping**
  – \( f \) for high V_{TH} & \( 2f \) for low V_{TH} with body bias
  – Cannot be applied to FD-SOI.

↓

• With help of DIBL, V_{DD}-hopping is effective even in leakage-dominant environment.

\textbf{V}_{\text{DD}}\text{-hopping mechanism}

- At least, 2 kinds of \( V_{\text{DD}} \)s & \( f \)s must be provided.

\begin{itemize}
  \item \( V_{\text{DD}} \) (power supply)
  \item DC/DC converter
  \item \( V_{\text{DD}} \) 0.5<>1.0V
  \item DC/DC converter
  \item \( V_{\text{DD}} \) 0.5<>1.0V
  \item \( f \) (frequency)
  \item VCO
  \item \( f, 2f \)
\end{itemize}

- \( V_{\text{DD}} \) is externally changed.
- In terms of transient time, on-chip device is better.
- VCO can output \( f \) & \( 2f \).
- frequency selector is implemented.
Circuit design

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Block diagram

- Dual $V_{DD}$ & $V_{TH}$ scheme
  - Low $V_{DD}$ & $V_{TH}$ for logic, high $V_{DD}$ & $V_{TH}$ for memories
- $V_{DDH}=2V_{DDL}$.
16bit Kogge-Stone adder in ALU

- Critical path in logic part
- 6-gate path
- 1.5ns w/o F/Fs at 0.5V $V_{DDL}$
- 2.1ns with F/Fs
- ALU also has shifter & bit operator.

Carries

Generates & propagates
SRAM block diagram

- High $V_{DD}$ & $V_{TH}$ cells
  - To suppress cell leak
- High $V_{DD}$ WL & BL
- Low $V_{DD}$ buffers & predecoder
- Level-up converters are needed.

- Low $V_{DD}$ & $V_{TH}$ ($V_{DDL}$ & $V_{THL}$)
- High $V_{DD}$ & $V_{TH}$ ($V_{DDH}$ & $V_{THH}$)
Replica-biasing level-up converter

Replica biasing

Conventional

Voltage divider

Decoder

Global word line

Other decoders

+ x2 faster
- Large static current & small input margin

Experimental results

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Measurement setup

- LSI tester
- Slow testing
  - External memory I/F

- VCO output
  - 1/64 of internal operation $f$
- 0.5V, 400MHz operation
• 0.25µm, 3-metal FD-SOI

• Dual-$V_{TH}$
  ($V_{THL}=0.0V$ & $V_{THH}=0.3V$)

• 2000 gates in logic part

• Memories account for 85% of transistor count.
Compact cell library

• Small number of logic gates doesn't degrade performance much*. 
  
• Only 20 kinds of logic gates
  – Detailed design tuning is possible.
  – INVx3, NANDx3, NORx3, AOIx2, OAIx2, EXOR, EXNOR, MUXx2, DFFx2, CLKBUF

• On 2NOR, \( \frac{I_{ON_P}}{I_{OFF_N}} = 33 \) when \( V_{DDL} = 0.5V \).
  – Sizing is critically important.

SRAM delay breakdowns - critical path

<table>
<thead>
<tr>
<th>$V_{DDL}$ [V]</th>
<th>$V_{DDH}$ [V]</th>
<th>Address-in</th>
<th>Data-out</th>
</tr>
</thead>
<tbody>
<tr>
<td>A: 0.5</td>
<td>0.5</td>
<td>Memory core</td>
<td>5.5ns=180MHz</td>
</tr>
<tr>
<td>B: 0.5</td>
<td>1.0</td>
<td></td>
<td>2.5ns=400MHz</td>
</tr>
<tr>
<td>C: 1.0</td>
<td>2.0</td>
<td></td>
<td>1.25ns=800MHz</td>
</tr>
</tbody>
</table>

- $V_{DDH}$ should be $2V_{DDL}$.
  - For high speed
- $V_{DDH}$ should not be 2.0V.
  - Level-up converter fails when $V_{DDL}=0.5V$.

$V_{DDH}=2V_{DDL}$

$V_{DDH}=V_{DDL}$

Simulation

Measurement

$T_a=30^\circ$C
Operation frequency - measurement

- 0.5V-400MHz & 0.9V-800MHz

- In sub-1V with moderate $V_{TH}$, delay has negative temperature coefficient*.

- However, with 0 $V_{TH}$, positive temperature dependence is observed.

Leakage dependence on $V_{DDL}$

- Leakage is strong function of $V_{DDL}$.
- Drain induced barrier lowering (DIBL) effect

![Graph showing leakage current ($I_{LEAK}$) as a function of $V_{DDL}$](image)

$V_{DDH} = 2V_{DDL}$

Clock: stopped

$T_a = 100^\circ C$

Measurement

$V_{DDH} = 2V_{DDL}$

$Ta=100^\circ C$

x3.6

30$^\circ C$

0 0.5 1

0 10 20 30 40 50

$I_{LEAK}$ [mA]

$V_{DDL}$ [V]
Power - measurement

- $P_{\text{TOTAL}}$ & $P_{\text{LEAK}}$
  - Similar dependence

- Possible to scale power by changing only $V_{\text{DDL}}$

- $V_{\text{DD}}$-hopping is effective even in sub-1V FD-SOI.

$V_{\text{DDL}}$ [V]

$P_{\text{TOTAL}}$, $P_{\text{LEAK}}$ [mW]

Hopping

$V_{\text{DDH}} = 2V_{\text{DDL}}$

- 30°C
- 100°C

Power scaling in $V_{DD}$-hopping - analysis

\[ P_{\text{LEAK}} \propto V_{DDL} \cdot I_0 \cdot 10 \]
\[ \frac{V_{TH} - \lambda \cdot V_{DDL}}{s} \]
\[ P_{\text{DYNAMIC}} \propto f \cdot V_{DDL}^2 \]
\[ \propto \frac{(V_{DDL} - V_{THL})^\alpha}{V_{DDL}} \cdot V_{DDL}^2 \]
\[ \propto V_{DDL}^{2.5} \]

$V_{THL} = 0$
$\lambda = 0$ or $0.1$ (DIBL coefficient)
$s = 0.08$ (s-factor)
$\alpha = 1.5$
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• 0.5V, 400MHz, 3.5mW, FD-SOI processor with compact cell library

• Design methodology in 0.5V generation
  – Zero $V_{TH}$
  – Dual $V_{DD}$ & $V_{TH}$, low for logic & high for memory
  – Replica-biasing level converter
  – With help of DIBL, $V_{DD}$-hopping is effective even in leakage-dominant environment.