10.7 1.27Gb/s/pin 3mW/pin Wireless Superconnect (WSC) Interface Scheme

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High-speed and high-density I/O's are becoming more and more important to fill an increasing gap between the communication bandwidth inside a VLSI and the bandwidth among chips. The ITRS roadmap predicts that VLSI pin count will exceed 7000 in the future. Thus low-power is also essential for future I/O's. Currently available I/O schemes still have issues to overcome to be a realistic solution for the future. High-speed serial links are fast but analog circuits to drive large off-chip load consume 100mW and occupy about 0.05mm^2. Micro bump technology [1] offers high-density I/O's, but the existence of the physical contacts requires a highly capacitive ESD structure that increases delay, power and area and hinders the scaling of the pads further.

Wireless I/O schemes without physical contacts are an attractive alternative for future interfaces. This has been tried in printed circuit board environments in [2] but the power per pin is still larger than 10mW. This paper describes an I/O scheme, Wireless Superconnect (WSC), which enables two chips to directly communicate by capacitive coupling. It provides high-density, low-power and high-speed I/O communication.

Figure 10.7.1 shows a sketch of the WSC scheme. The topmost metal layer is used to form mini-pads. Each mini-pad is about 20μm per side and separation between mini-pads is 20μm. When both chips are placed face-to-face and the pad distance is about 1μm to 2μm including the top protection layer, each pair of pads forms a capacitor of the order of 10fF. This value is sufficient for the receiver described later to pick up the small signal generated on the capacitor node. The small capacitance associated with the contact-less pad is achieved by the elimination of an ESD protection structure, which usually adds pico-farads of capacitance to an I/O. Measurement indicates no ESD problem exists since the surface of the pad is covered by oxide. The situation is the same as a normal internal node which has interconnect using the top metal layer. As for providing power physical connection using embedded bumps are preferable [2] but for low-power applications, the power may be supplied through inductive coupling.

Figure 10.7.2 shows the circuit implementation of the WSC whose transmitter can be a simple CMOS driver. On the other hand, the receiver needs to amplify the small signal. A CMOS inverter whose input and output are tied is used to transmit a clock signal but this type of amplifier consumes a great deal of power due to the short-circuit current. A sense-amplifying flip-flop activated by the recovered clock is used for other signals to reduce power dissipation. The transmitter and receiver use $V_{DD}/2$ precharge whose activation timing is controlled by signals, ϕ_{PCS} and ϕ_{PCR}. The transmitter translates a NRZ signal into a return-to-$V_{DD}/2$ signal. The receiver based on sense-amplifying F/F reproduces the original signal. $V_{DD}/2$ voltage level is distributed from a $V_{DD}/2$ generator used in DRAMs shared among pads. These circuits can be laid out under the pad and small circuit area is achieved because neither a large output driver nor an ESD protection circuit is necessary.

SPICE simulation results are shown in Fig. 10.7.3. Prior to sending data, both terminals of the coupling capacitor and sense amplifier inputs, N1, N2 and N3, are precharged to $V_{DD}/2$. When sending data, $V_{DD}/2$ precharge is terminated by two control signals, ϕ_{PCS} and ϕ_{PCR}. Soon after ϕ_{PCS} goes to low, sender's transmission gate is opened, and D_{IN} is propagated to N1. When sufficient signal amplitude develops on N2, ϕ_{AMP} is activated. The voltage difference between N2 and N3 is then amplified into a digital signal level. Since gate overlap capacitance induces coupling noise from control signals to a data signal, precharging transistors are designed as small as possible. A dummy capacitor is placed on node N3 and at the output node of $V_{DD}/2$ generators to stabilize the voltage.

Figure 10.7.4 shows the test circuit and the measured waveforms. In the measurement, pad alignment of about 3μm is achieved using a marking on the edge of a scriber line. When I/O is activated, clock signal having frequency of f_1 is transmitted from the bottom chip to the upper chip. There, three data signals having frequencies of $f_1/2$, $f_1/4$, and $f_1/8$ are generated by a frequency divider. Then these signals are transmitted back to the bottom chip and are measured as shown in Fig. 10.7.4. During this period, I/O and the shift register operate at the frequency of f_1. Then, ϕ_{STR} is deactivated, and the stored data is scanned out by a slower clock frequency of f_2. The clock signal is fed to a frequency divider, and the frequency f_1 divided by 64 is monitored from outside of the chip. In order to realize robust clock transmission, the coupling capacitor for the clock is designed about 20 times larger than that for data signals.

Figure 10.7.5 shows the measurement and SPICE simulation results of speed dependence on V_{DD}. In the figure, the maximum transmission rate and the power consumption at that rate are shown. 900μA of current is drawn from 3.3V power supply at the operating rate of 1.27Gb/s corresponding to 3mW of power per pin. Of the 900μA, 360μA is for the transmitter and 540μA is for the receiver. The performance of the WSC scheme with scaled MOSFET's is also investigated by SPICE simulations and results are shown in Fig. 10.7.6. The result indicates that future 7000 I/O's can operate at 8.0GHz with only 1.63W when WSC is used. Thus, the WSC scheme is scalable and is promising in future VLSI's.

Figure 10.7.7 shows the microphotograph of the test chip fabricated in 0.35μm CMOS technology.

Acknowledgements
The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

Reference
[1] A. Matsuzawa, "System Module with Chip on Chip Technology for Realizing True System LSI's," in 8th Gakushin 165 committee meeting, pp. 8-14, Nov. 2000.
[2] S. Mick, J Wilson, and P. Franzon, "4Gbps High-Density AC Coupled Interconnection, " *2002 IEEE Custom Integrated Circuits Conference*, pp. 133-140.

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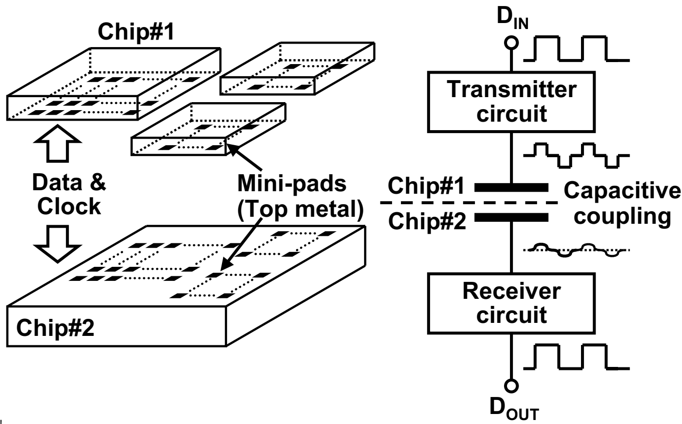

Figure 10.7.1: WSC overview.

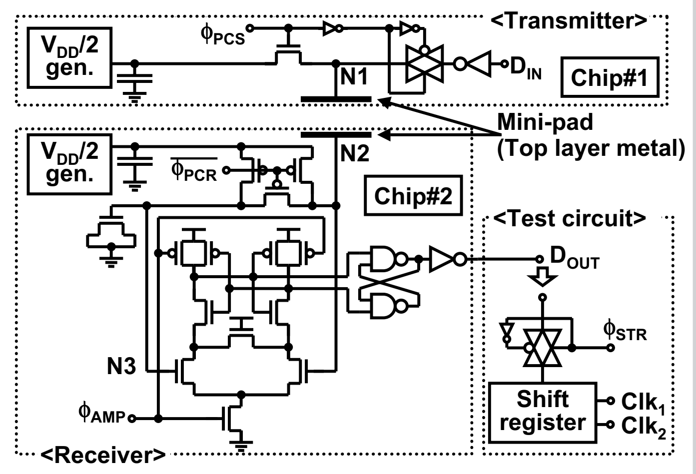

Figure 10.7.2: Circuit diagram of transmitter and receiver.

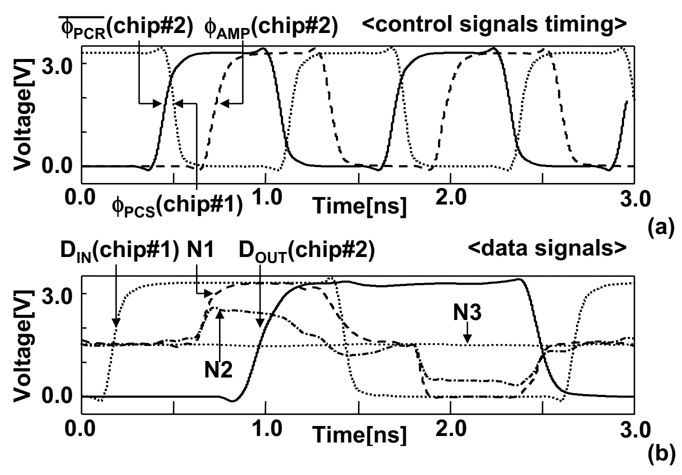

Figure 10.7.3: Operating waveform (SPICE simulation), (a) Control signals, and (b) Data signals.

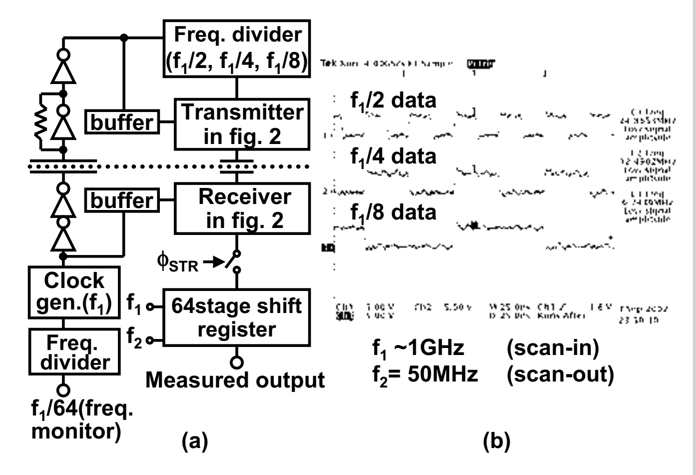

Figure 10.7.4: (a) Test environment, (b) Measured waveform.

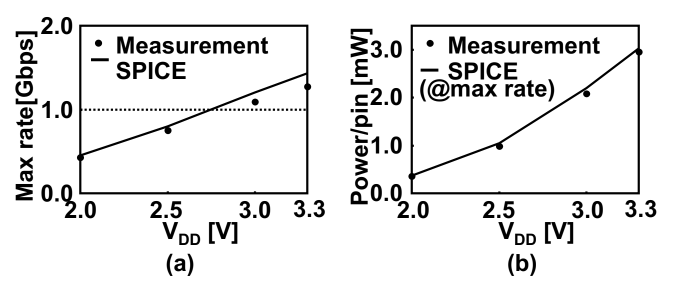

Figure 10.7.5: Measured and simulated WSC performance, (a) Supply voltage vs. speed, and (b) Supply voltage vs. power.

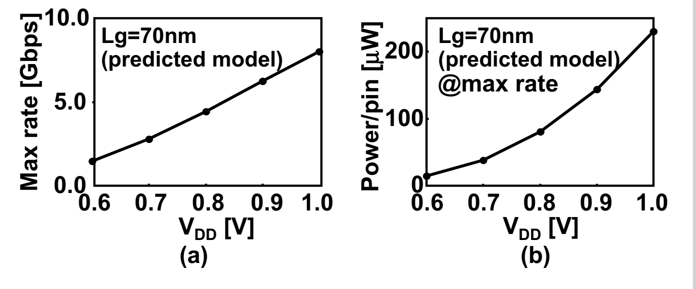

Figure 10.7.6: Simulated WSC performance in 70nm technology node, (a) Supply voltage vs. speed, and (b) Supply voltage vs. power.

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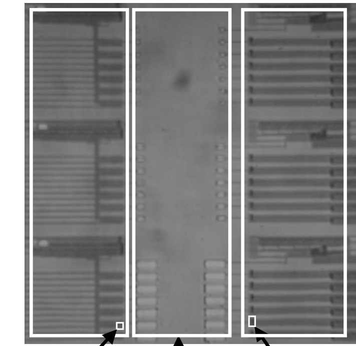

Figure 10.7.7: Test chip microphotograph.

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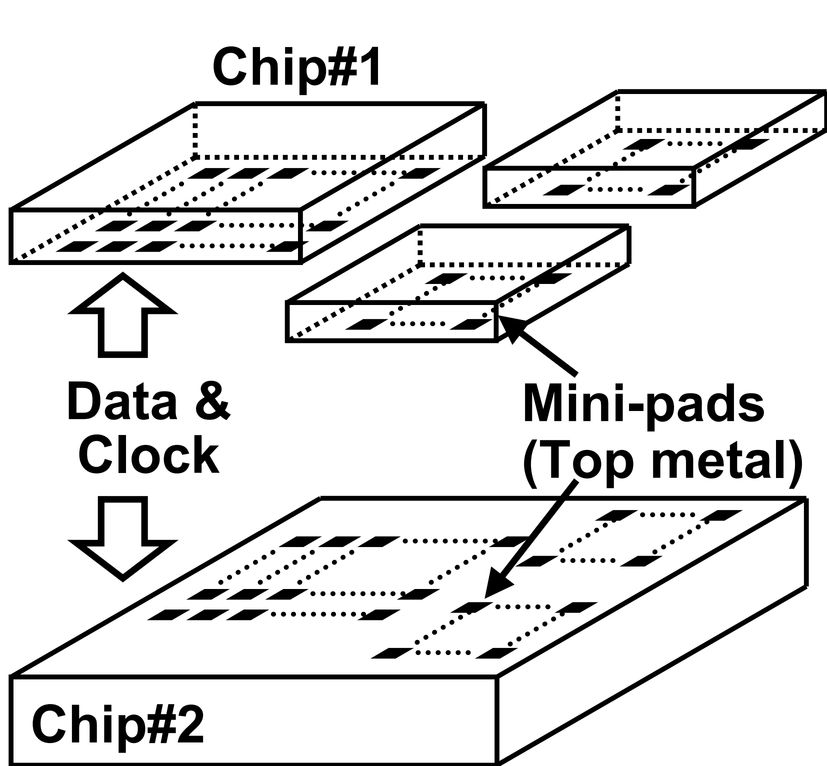

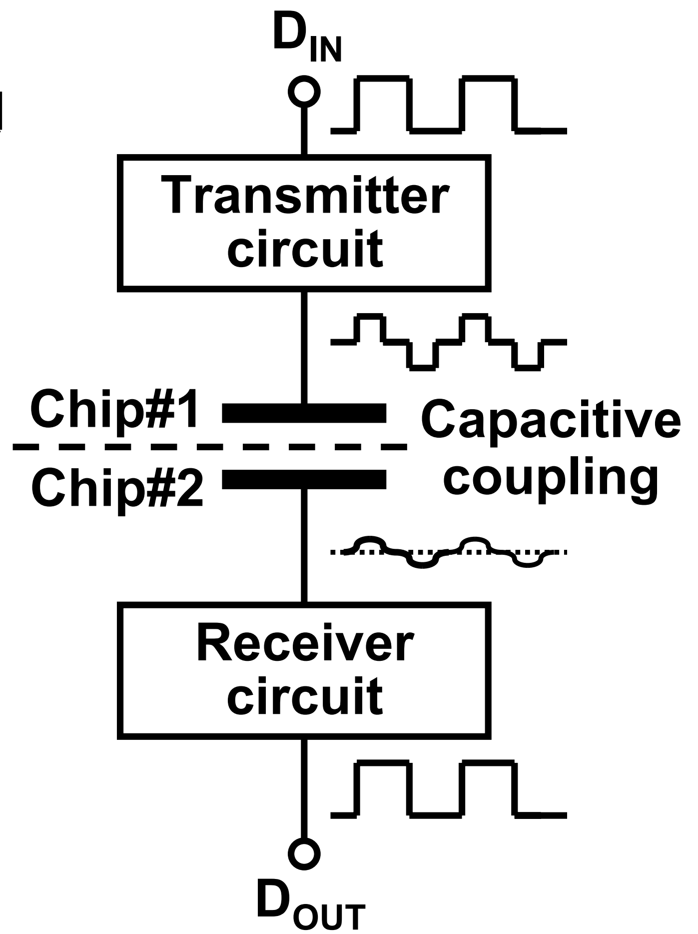

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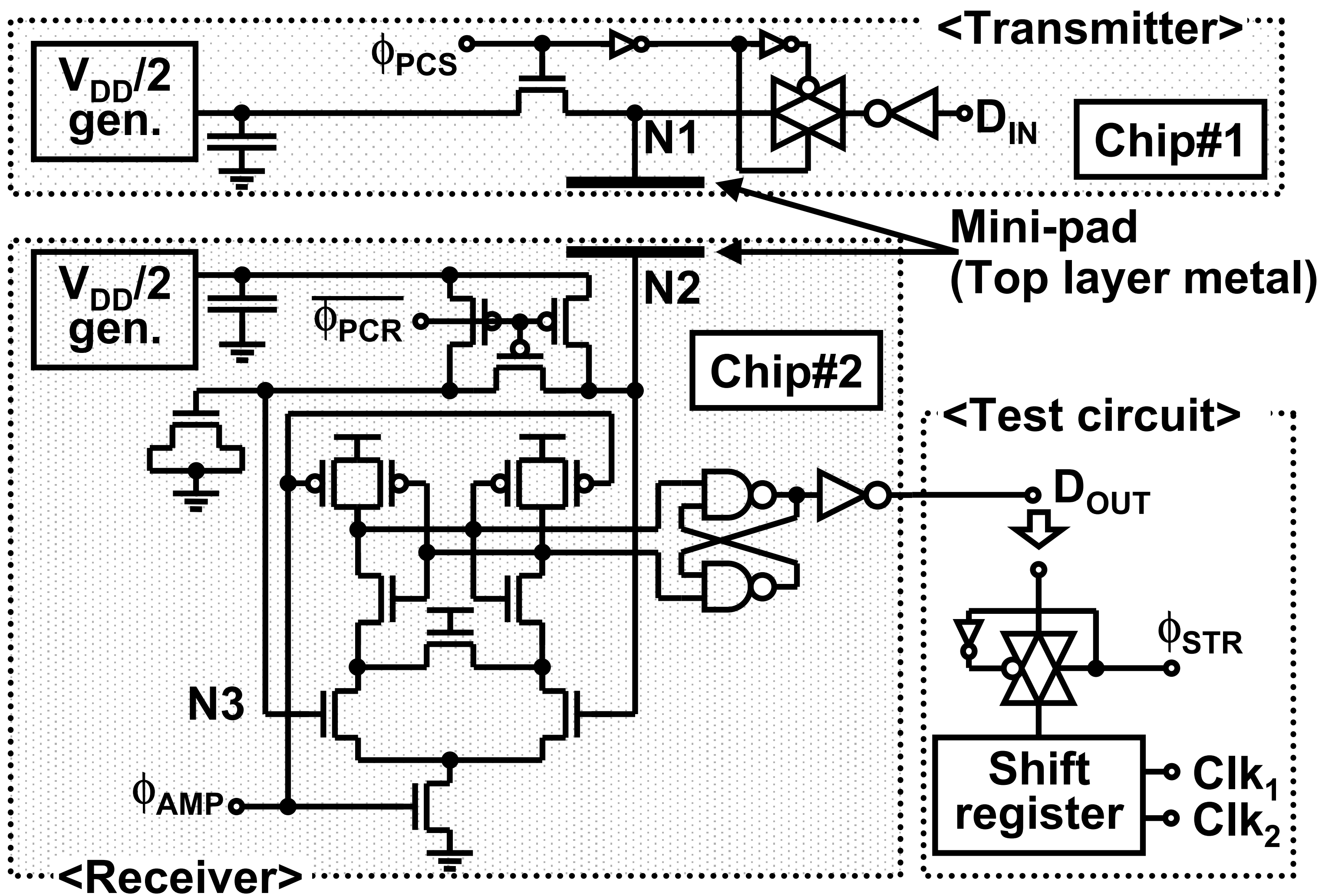

Figure 10.7.2: Circuit diagram of transmitter and receiver.

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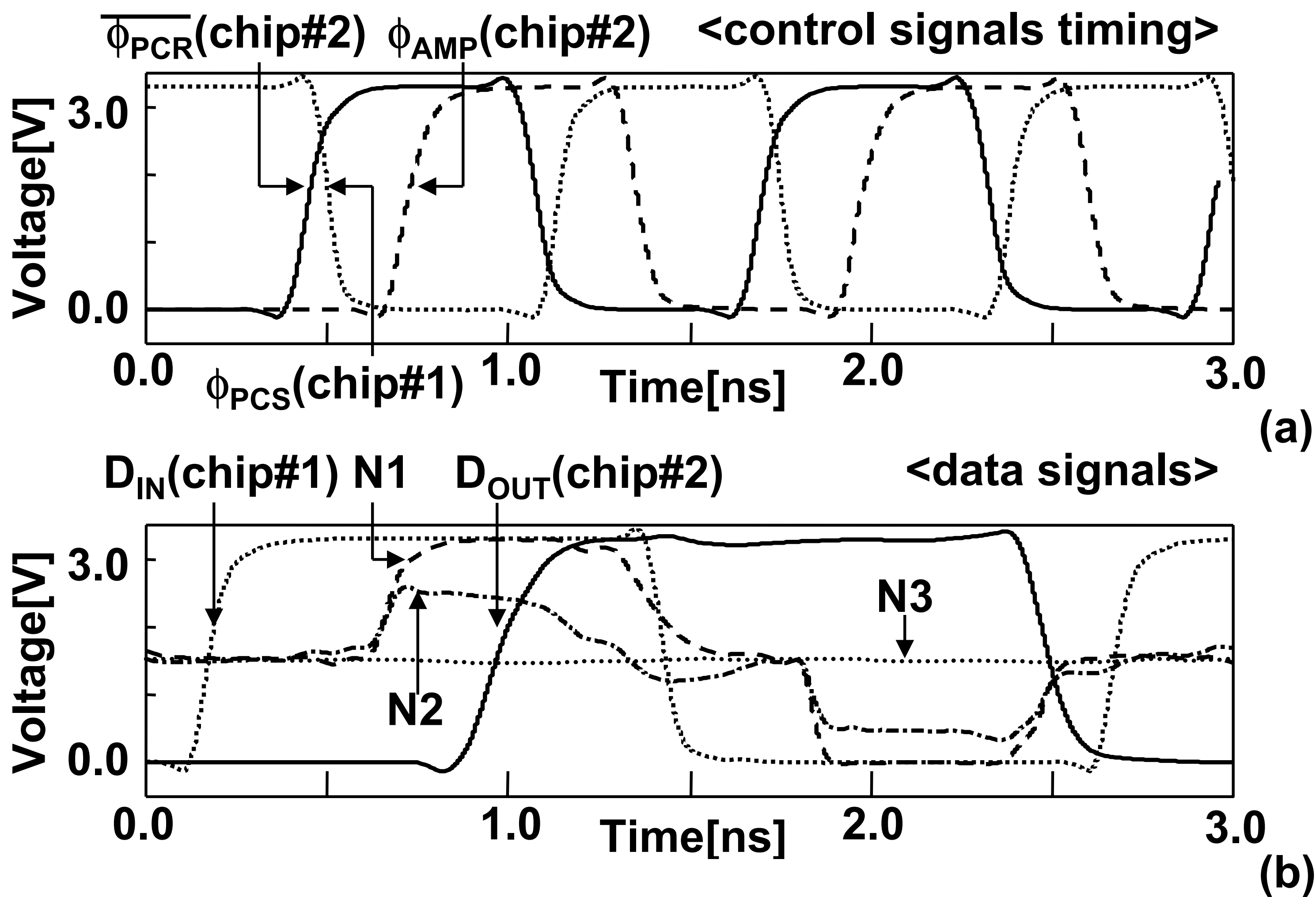

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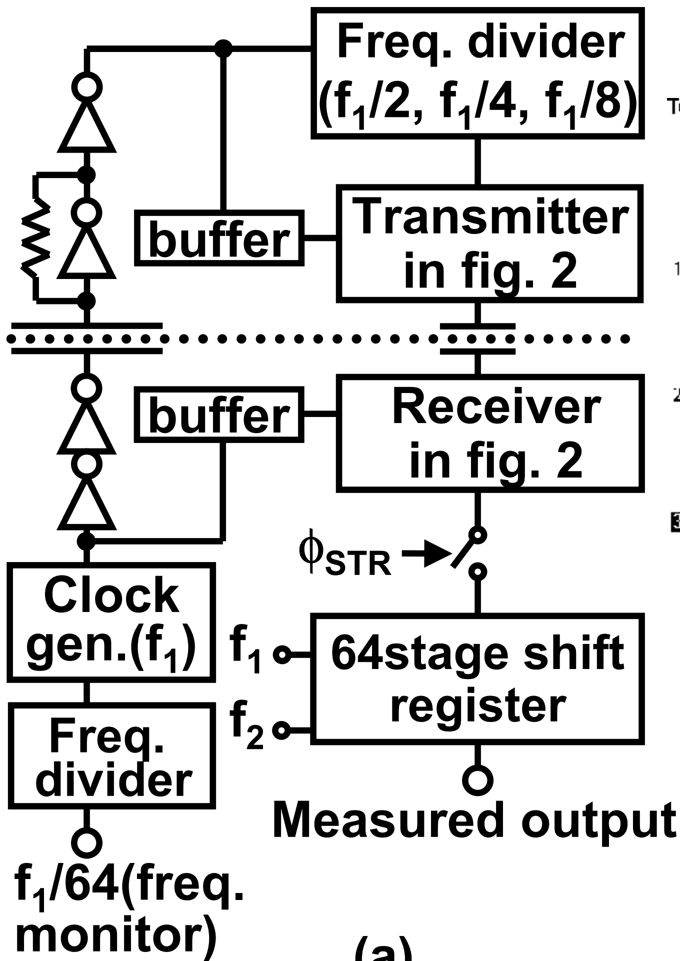


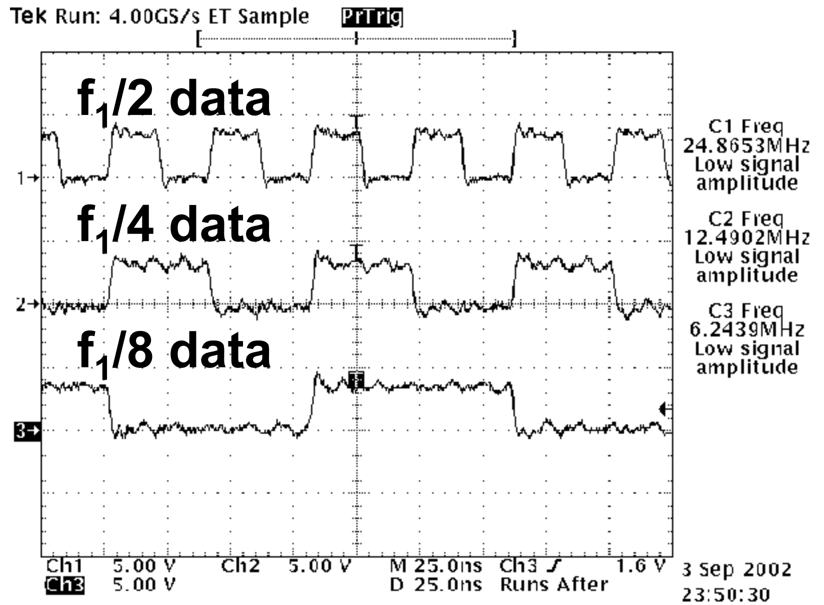
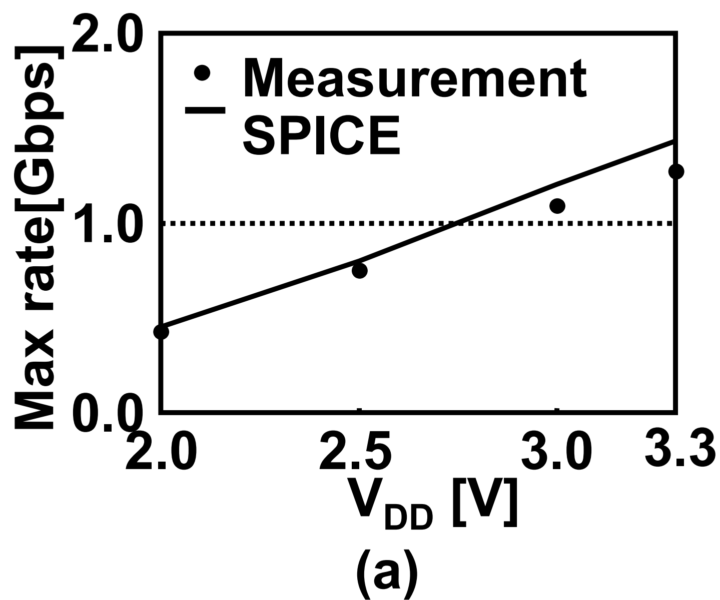


Figure 10.7.4: (a) Test environment, (b) Measured waveform.



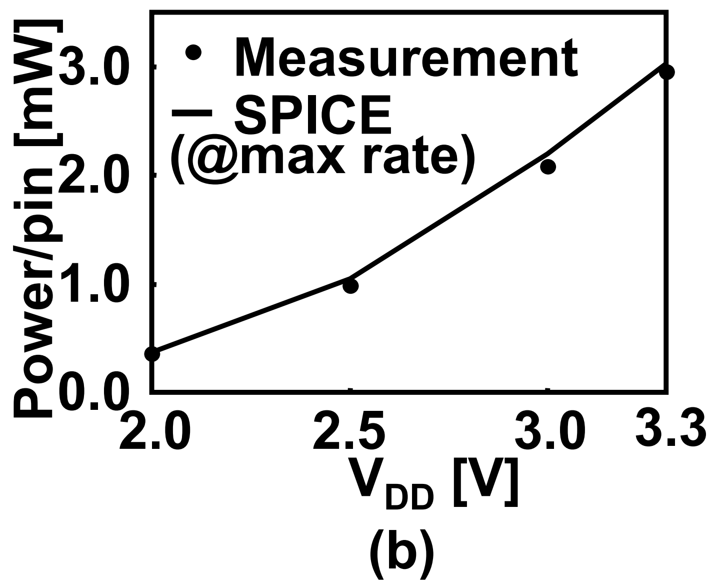


Figure 10.7.5: Measured and simulated WSC performance, (a) Supply voltage vs. speed, and (b) Supply voltage vs. power.

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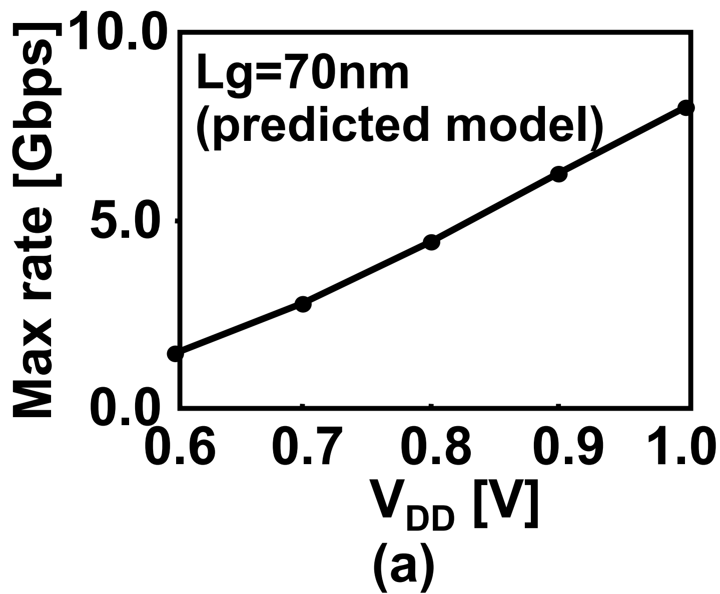

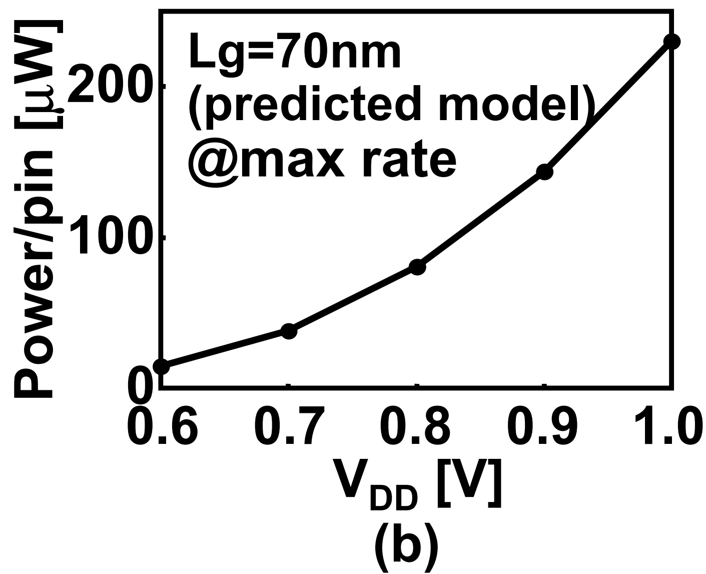

Figure 10.7.6: Simulated WSC performance in 70nm technology node, (a) Supply voltage vs. speed, and (b) Supply voltage vs. power.

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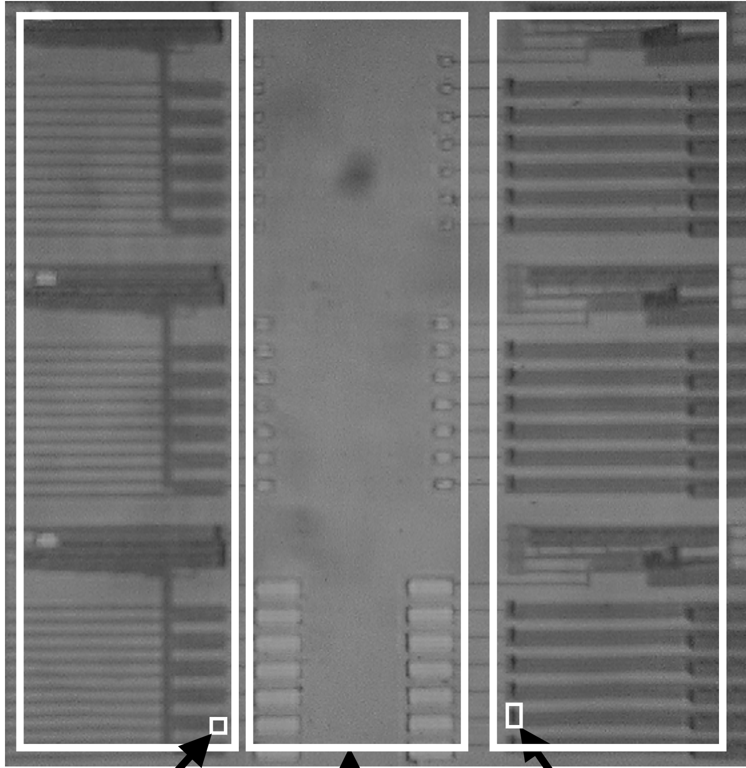

Figure 10.7.7: Test chip microphotograph.

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