1.27-Gbps/pin, 3mW/pin Wireless Superconnect (WSC) Interface Scheme

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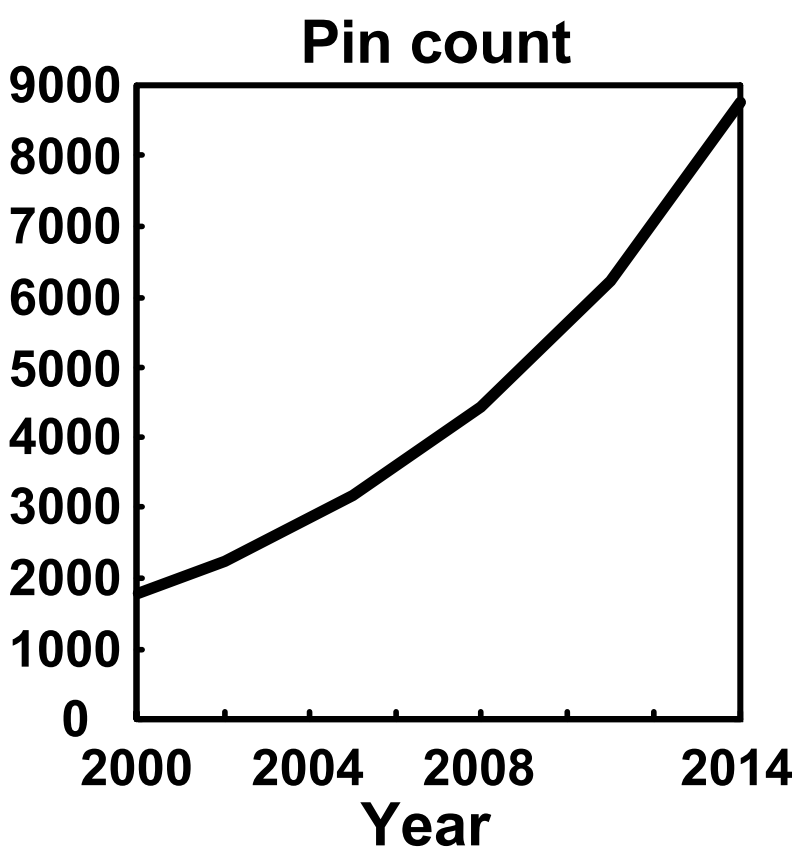
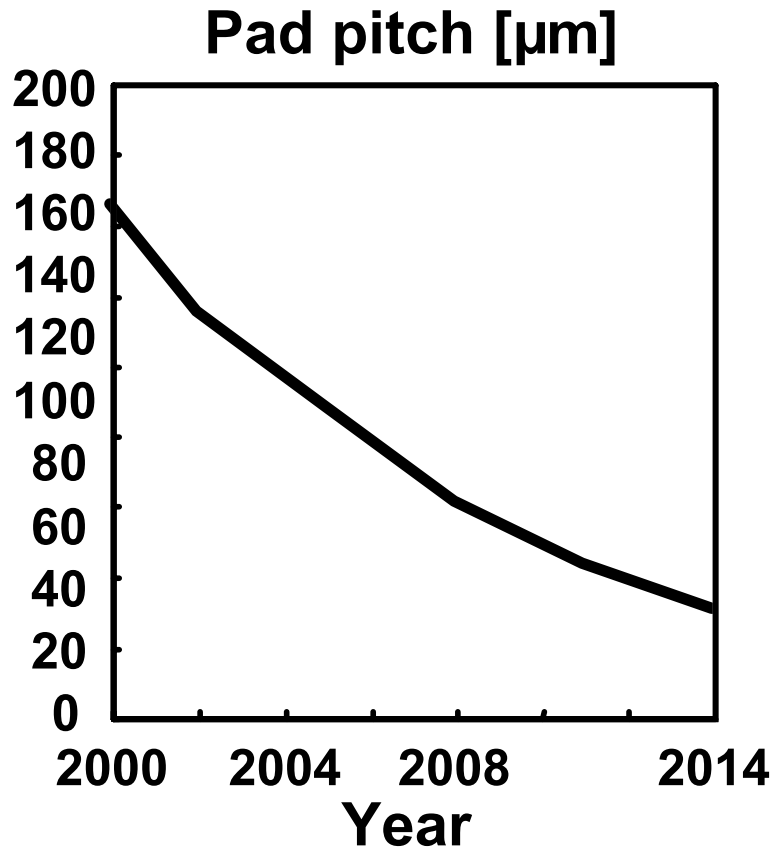
Outline

- Background
- WSC scheme overview
- Circuit design
- Measurement
- Simulation
- Conclusion

Trend in assembly predicted by ITRS

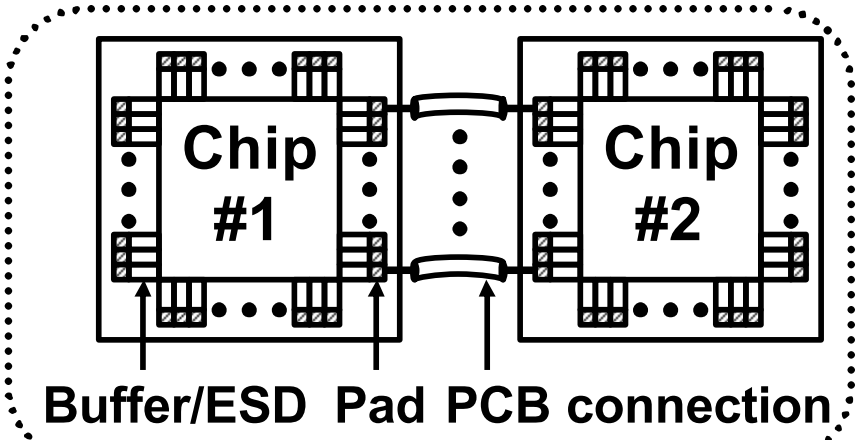




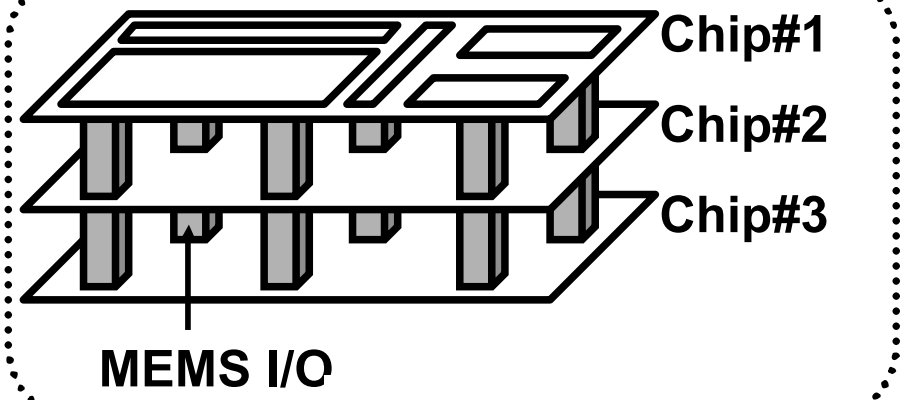
Target: Power/pin = 10.0mW (70W for 7000 pins)

Pad pitch = 20µm (7000 pads in 2.8mm^2)

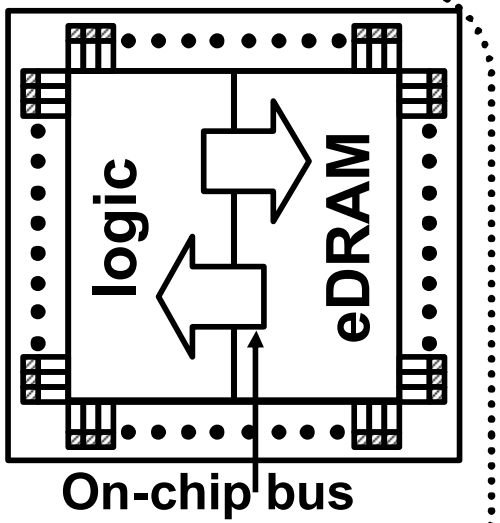
Various existing I/O schemes



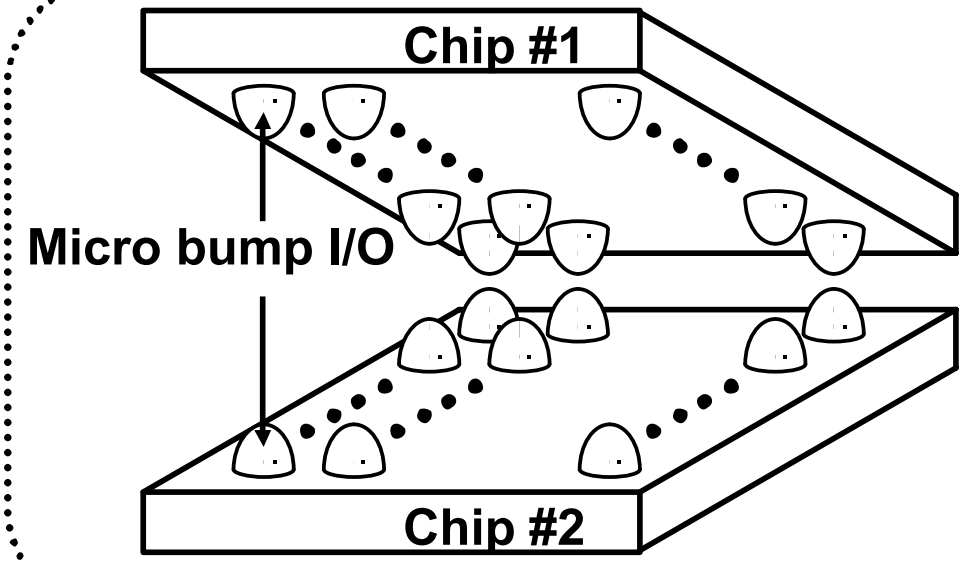
(A) High-speed link



(B) 3D MEMS

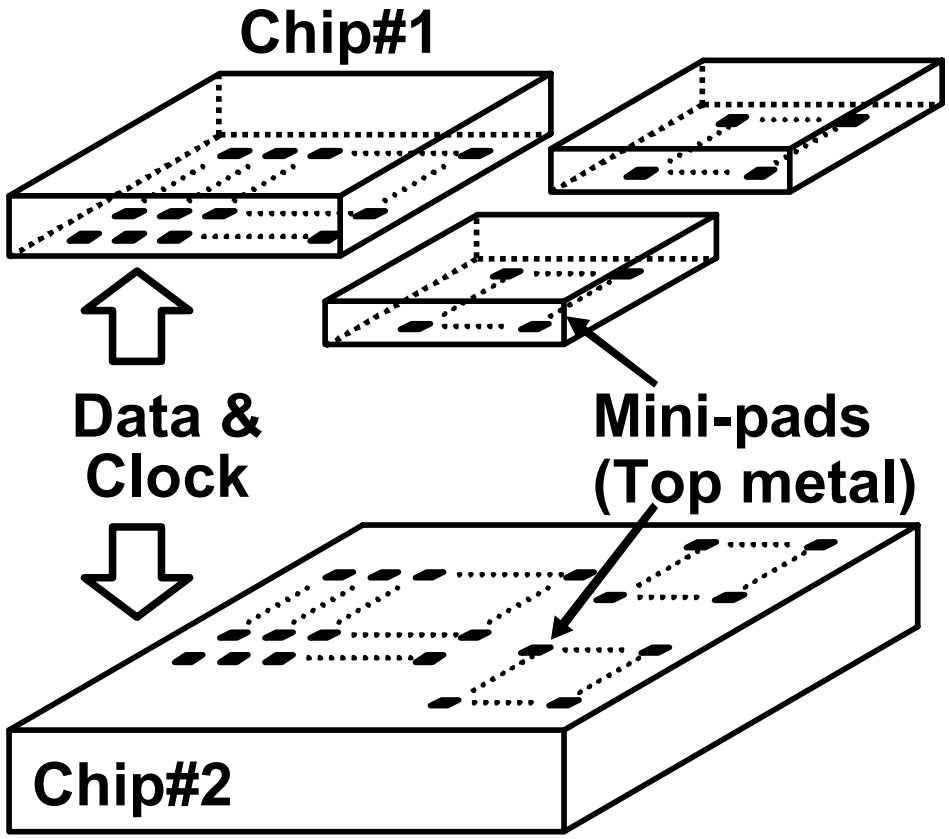


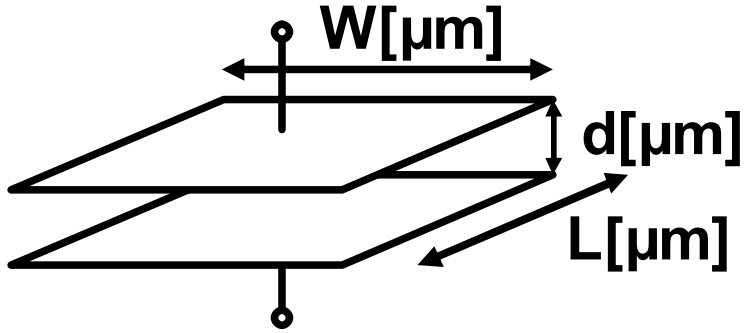
(C) System on a chip



(D) Micro bump

Wireless superconnect scheme overview





$$C = \frac{\varepsilon \cdot L \cdot W}{d}$$

$\varepsilon_{SiO2} = 35 \times 10^{-18}$ [F/μm]

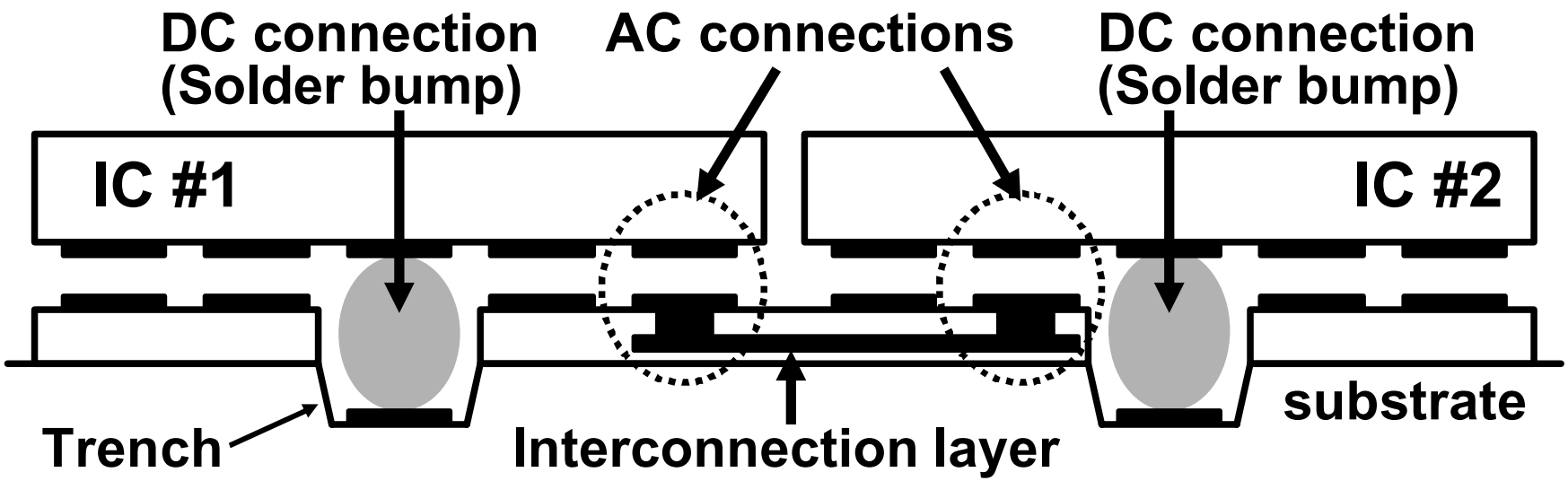
<ex.>

(L, W, d) (in μm)

(10, 10, 1) ➡ C=3.5fF

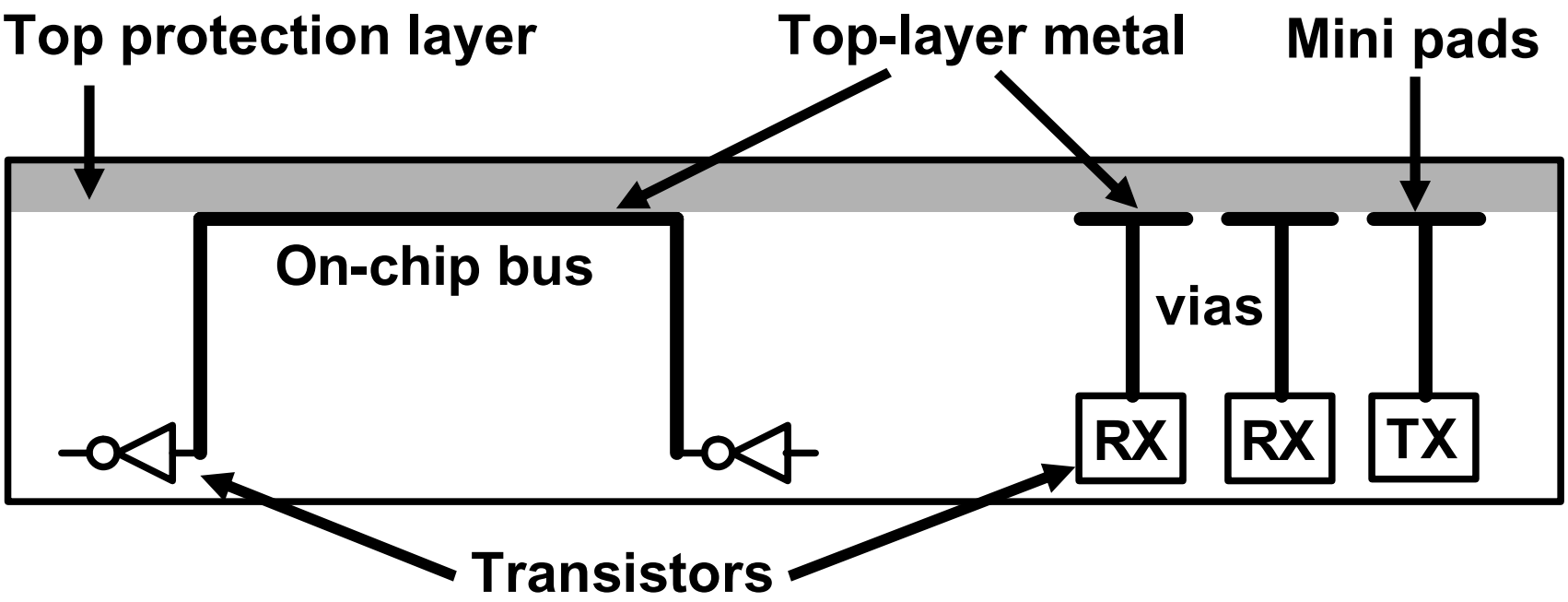
(20, 20, 1) ➡ C=14.0fF

Previous work



S. Mick et al. “4Gbps High-Density AC Coupled Interconnection,” Custom Integrated Circuits Conf., 2002, pp.133-140. (North Carolina State University)

ESD in WSC



ESD resiliency of pads

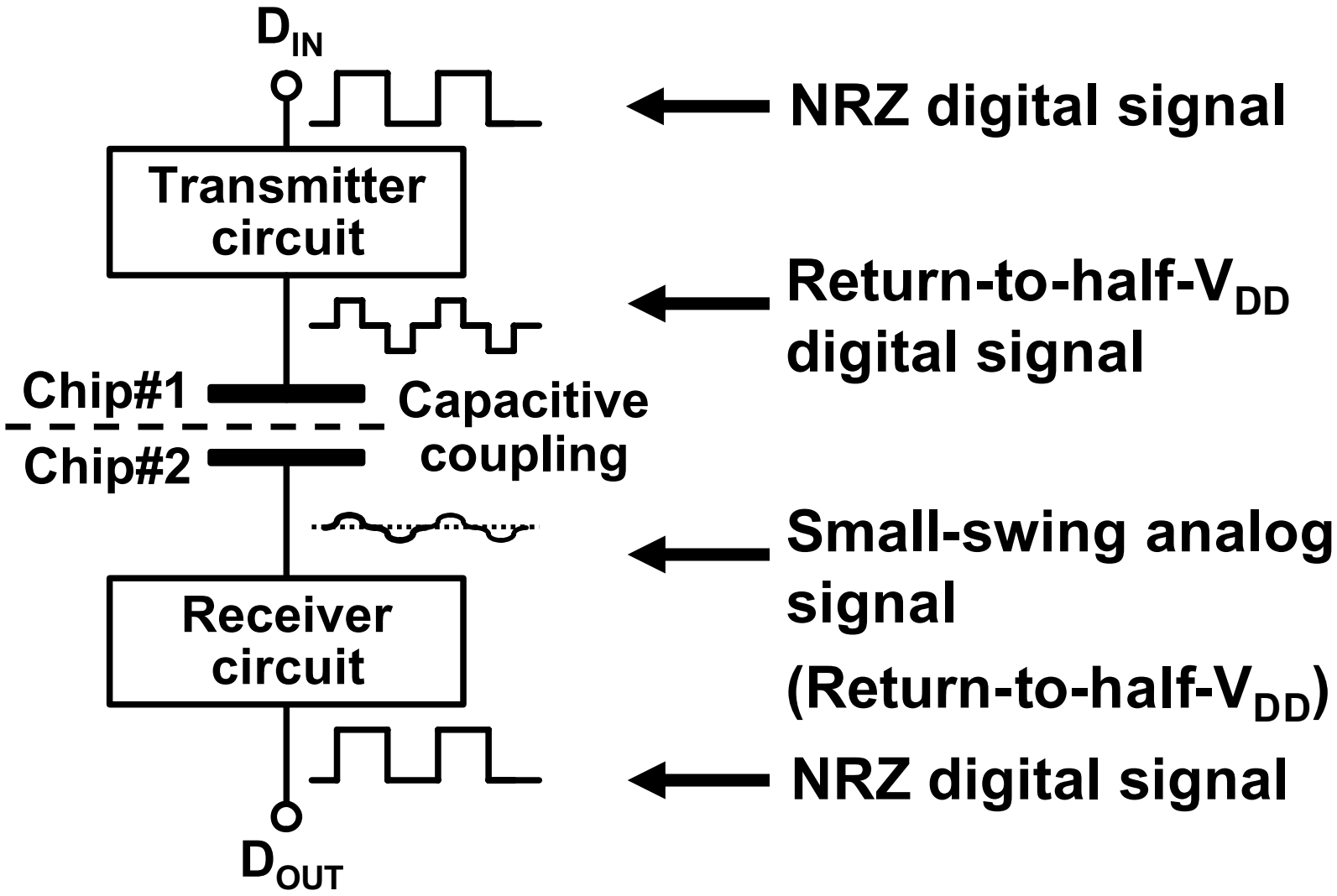
||

ESD resiliency of on-chip interconnections

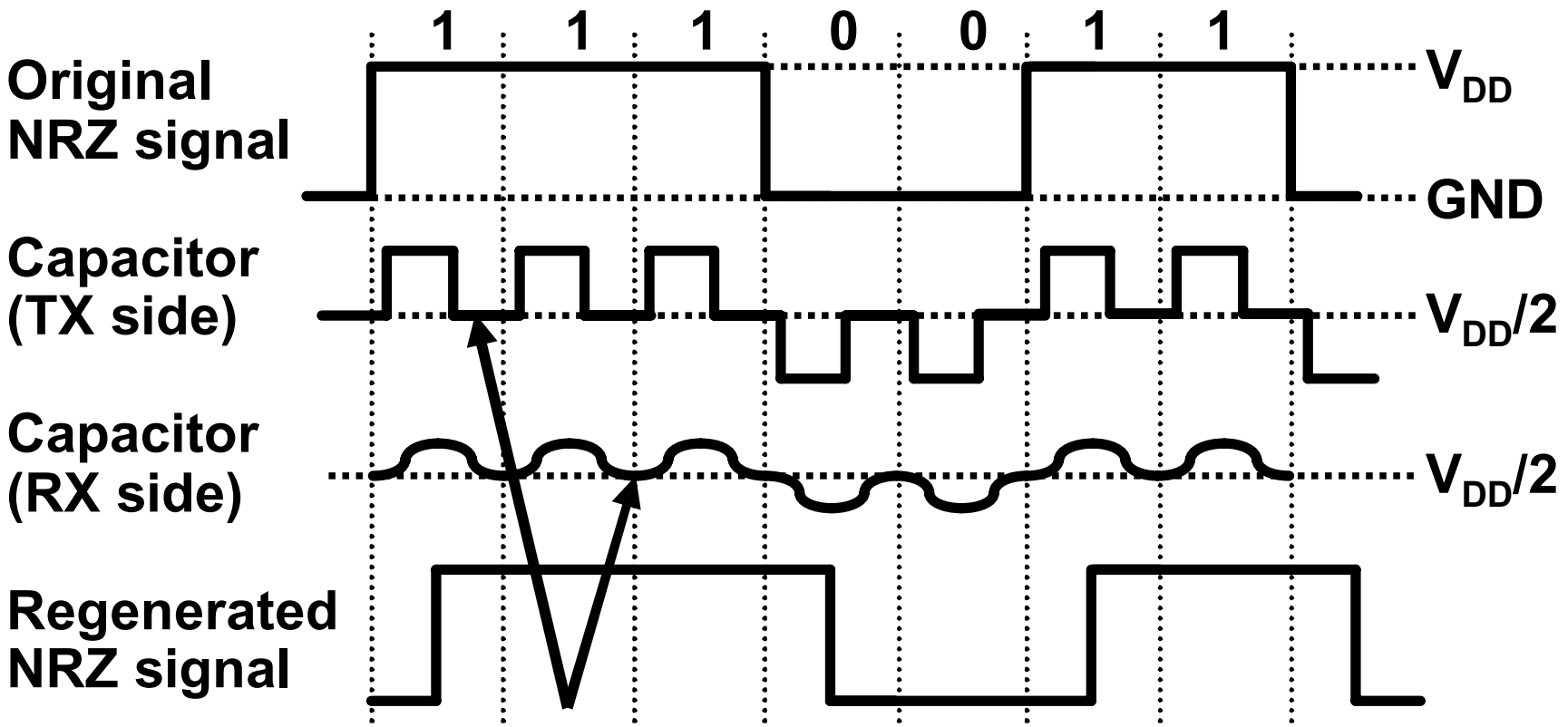
Comparison of interface schemes

	Serial link	3D MEMS	SOC	μ bump	WSC
Bandwidth	-	+	++	+	+
Cost	+	--	-	+	++
Area	--	++	-	+	+
ESD	-	-	-	-	+
Power	--	+	++	+	+
TAT	-	--	--	+	++

Signaling method in WSC



No DC-wandering problem

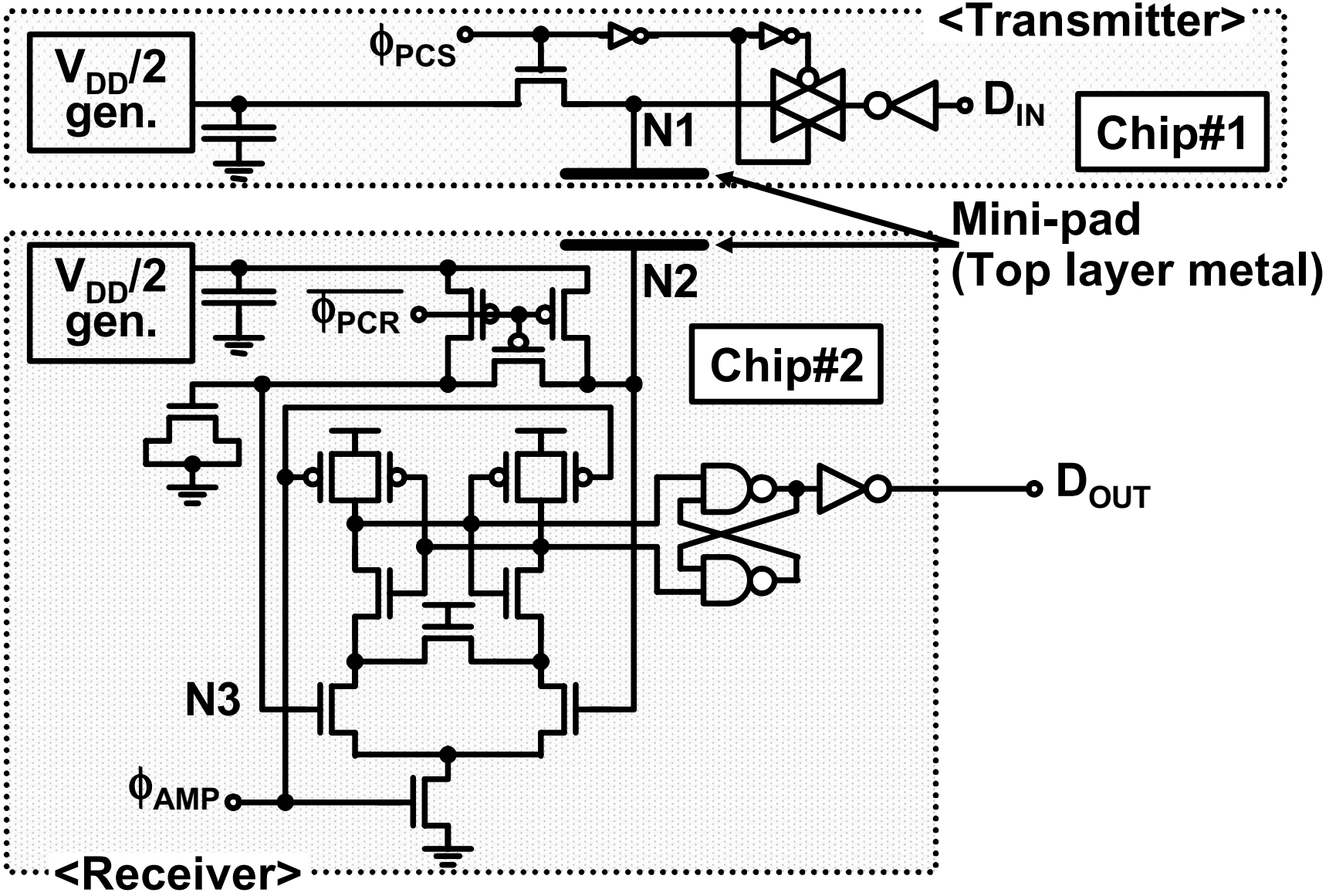


DC level is kept by $V_{DD}/2$ precharging.

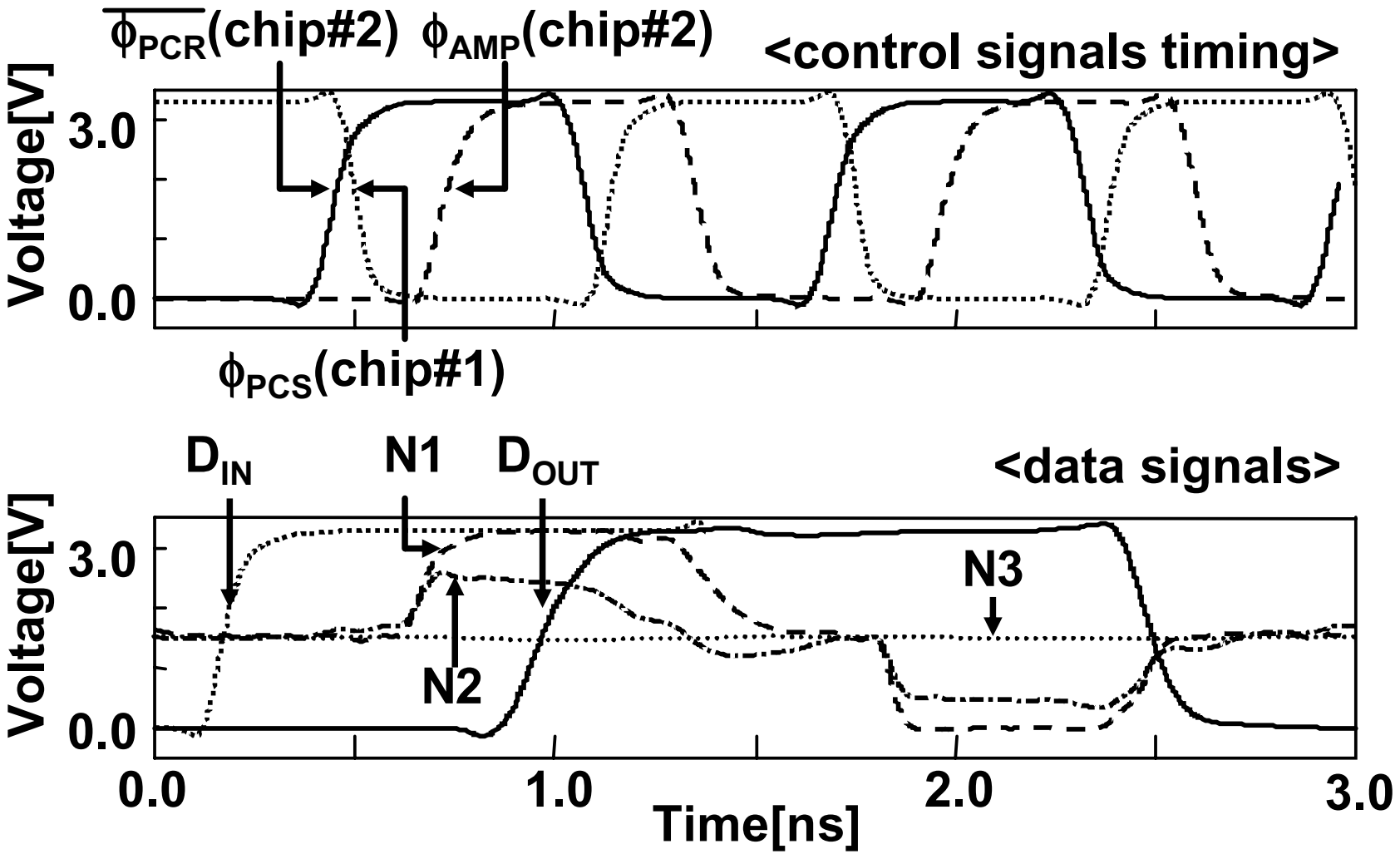
➡ Transition occurs in every cycle.

Precise timing for precharging and amplifier activation is needed.

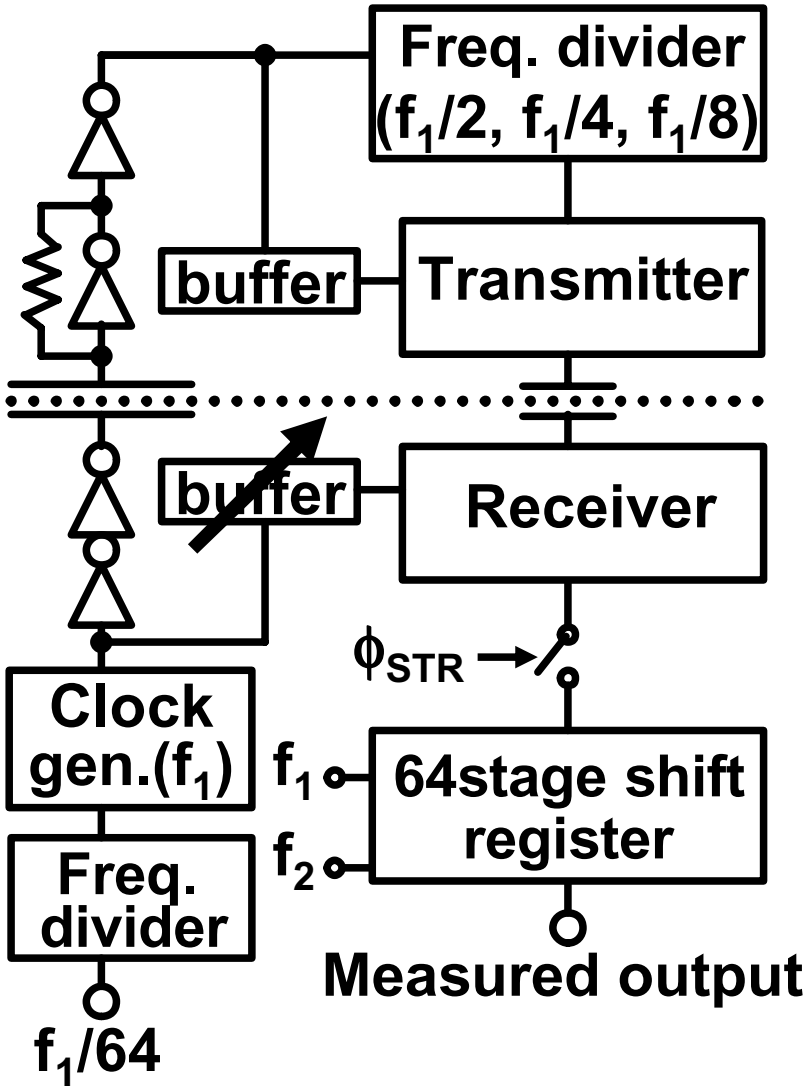
Circuit diagram of transmitter and receiver



Operating waveform

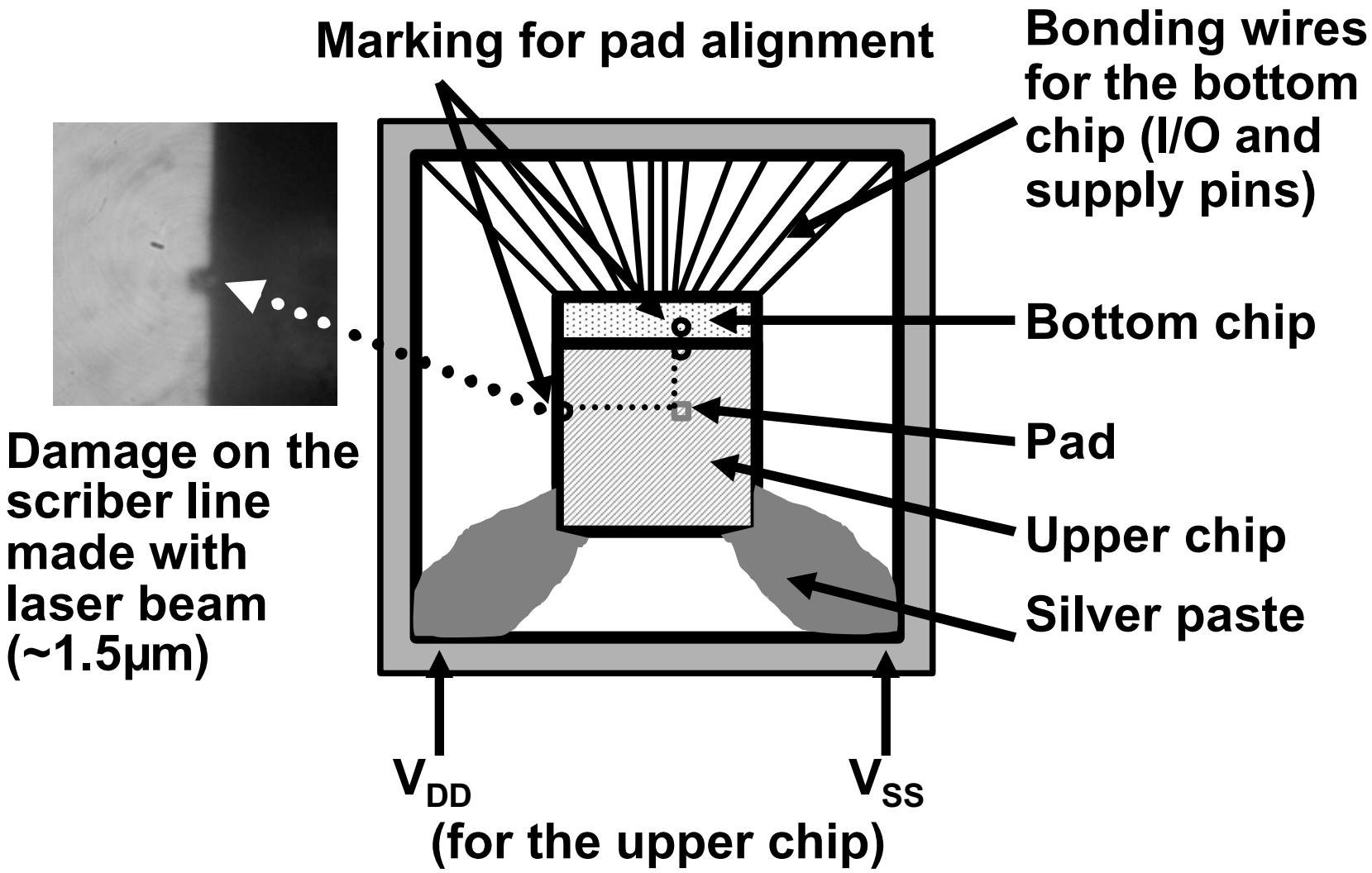


Test environment



- On-die clock generation for high frequency
- Receiver timing control with a variable delay buffer
- Monitoring clock frequency with a divider
- Storing data sequences in a shift register

Measurement setup

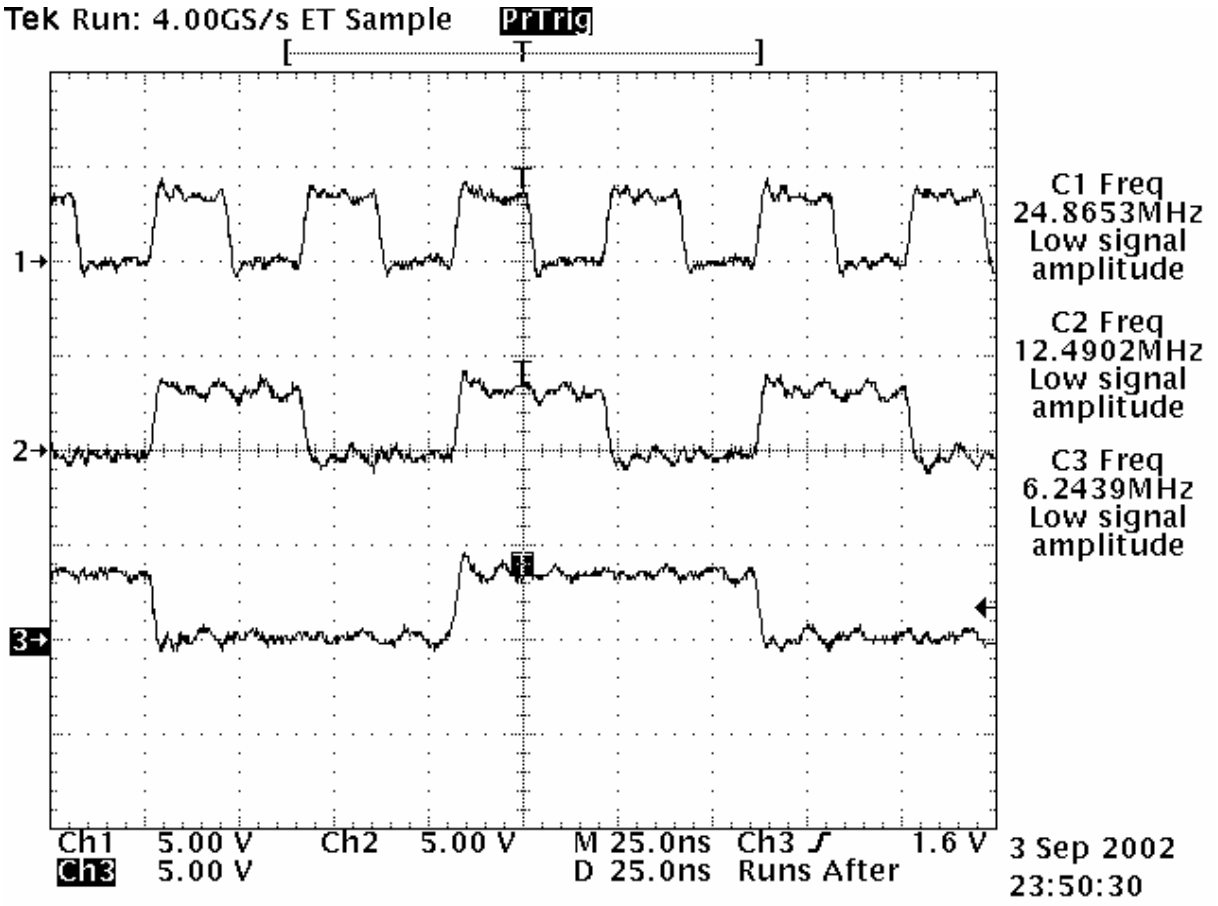


Measured waveform

$f_1/2$ data

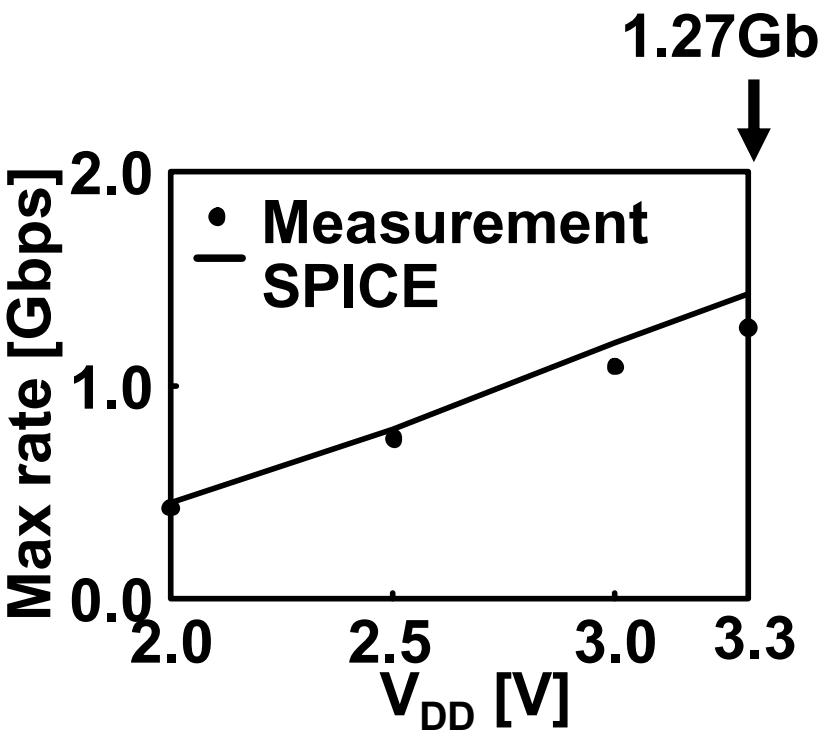
$f_1/4$ data

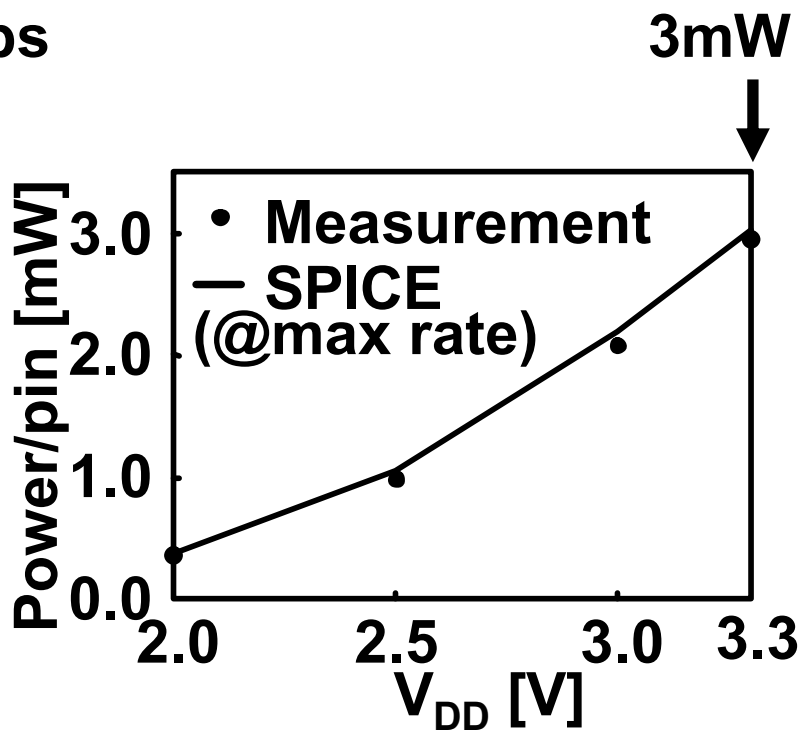
$f_1/8$ data



f_1~1GHz (scan-in), f_2= 50MHz (scan-out)

Measured and simulated WSC performance

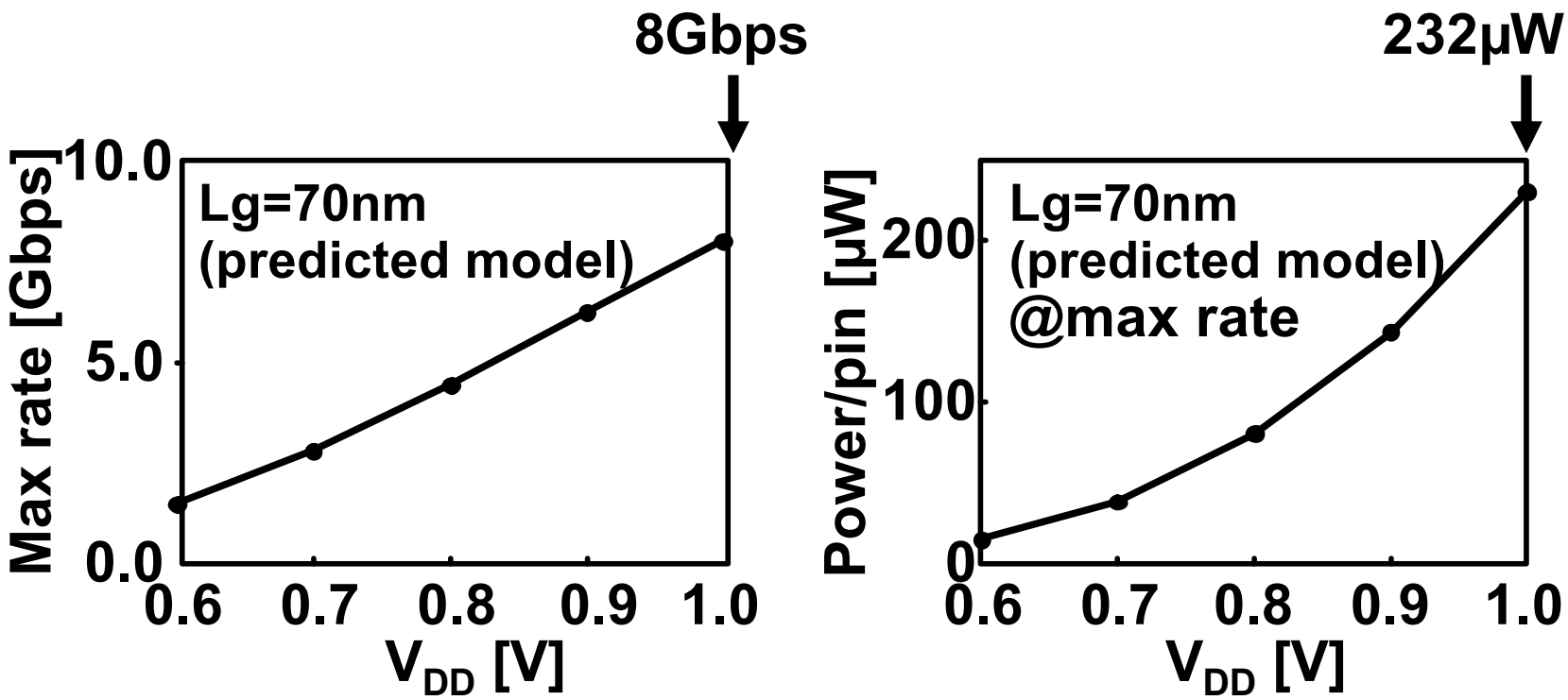




Transmitter : 360μA

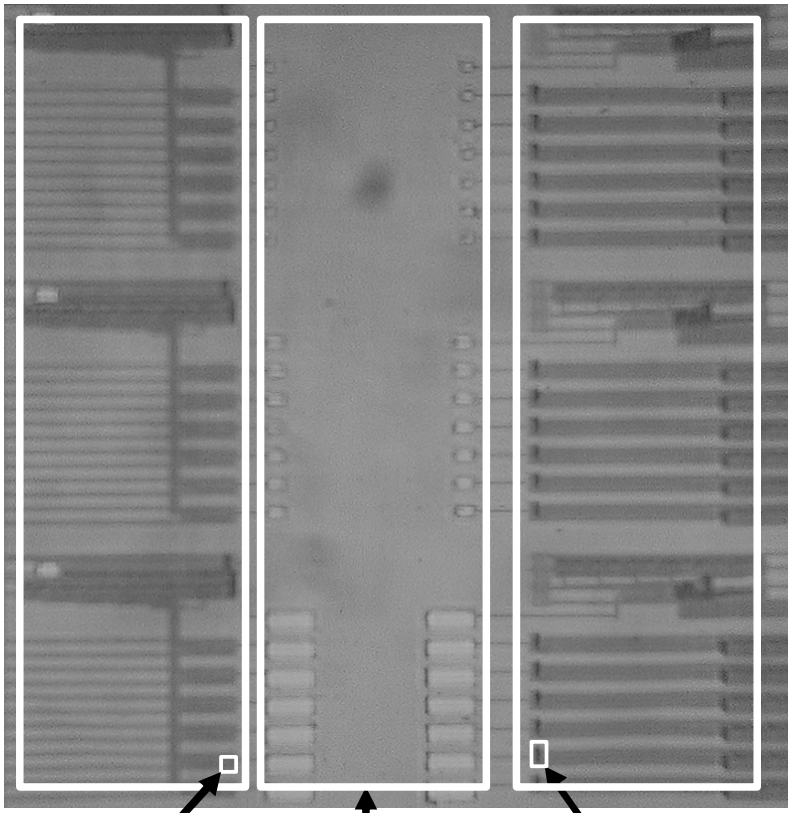
Receiver : 540μA

Simulated WSC performance in 70nm tech.



Future 7000 I/O pads can operate at 8GHz with only 1.63W.

Test chip microphotograph



Technology

0.35µm CMOS
Triple metal
3.3V supply

I/O design

Transmitter:20µmX20µm
Receiver: 12µmX12µm
Pad: 10µmX20µm

Conclusion

- WSC interface is proposed for high-density and low-power chip-to-chip communications.
- Low I/O capacitive load is achieved by small pad size and elimination of ESD structure.
- 1.27-Gbps with 3mW from 3.3V power supply was measured in 0.35μm CMOS technology.
- Simulation results in 70nm technology show possibility of 7000 I/O pads operating at 8-Gbps with 1.63W in 2.82mm^2.

Acknowledgements

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(VDEC = VLSI Design and Education Center)