Zigzag Super Cut-off CMOS (ZSCCMOS) Block Activation with Self-Adaptive Voltage Level Controller

An Alternative to Clock-Gating Scheme in Leakage Dominant Era

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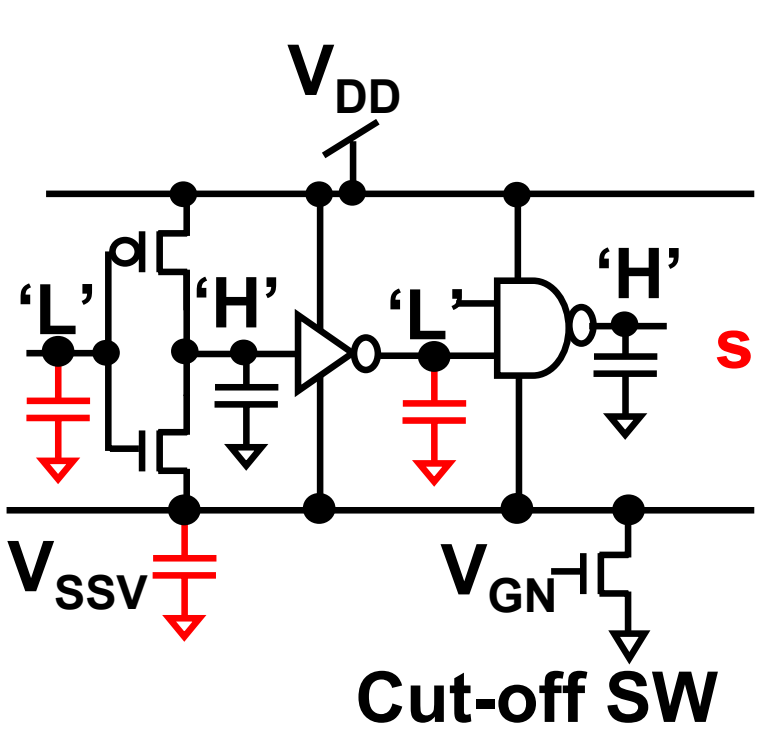
Outline

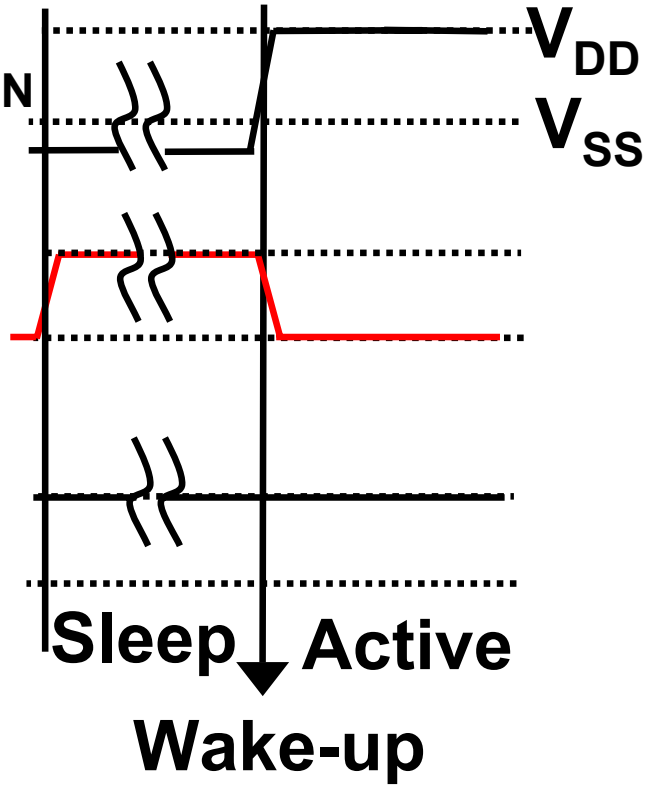
- Introduction
- Zigzag Super Cut-off CMOS (ZSCCMOS)
- ZSCCMOS Block Activation
- Control Circuitry with Adaptive Voltage Level Detector
- Measurement & Discussion
- Summary

Previous Leakage Suppression Scheme: Super Cut-off CMOS (SCCMOS)



'L' nodes & V_{SSV} (changed during sleep & restored to V_{SS} at wake-up)

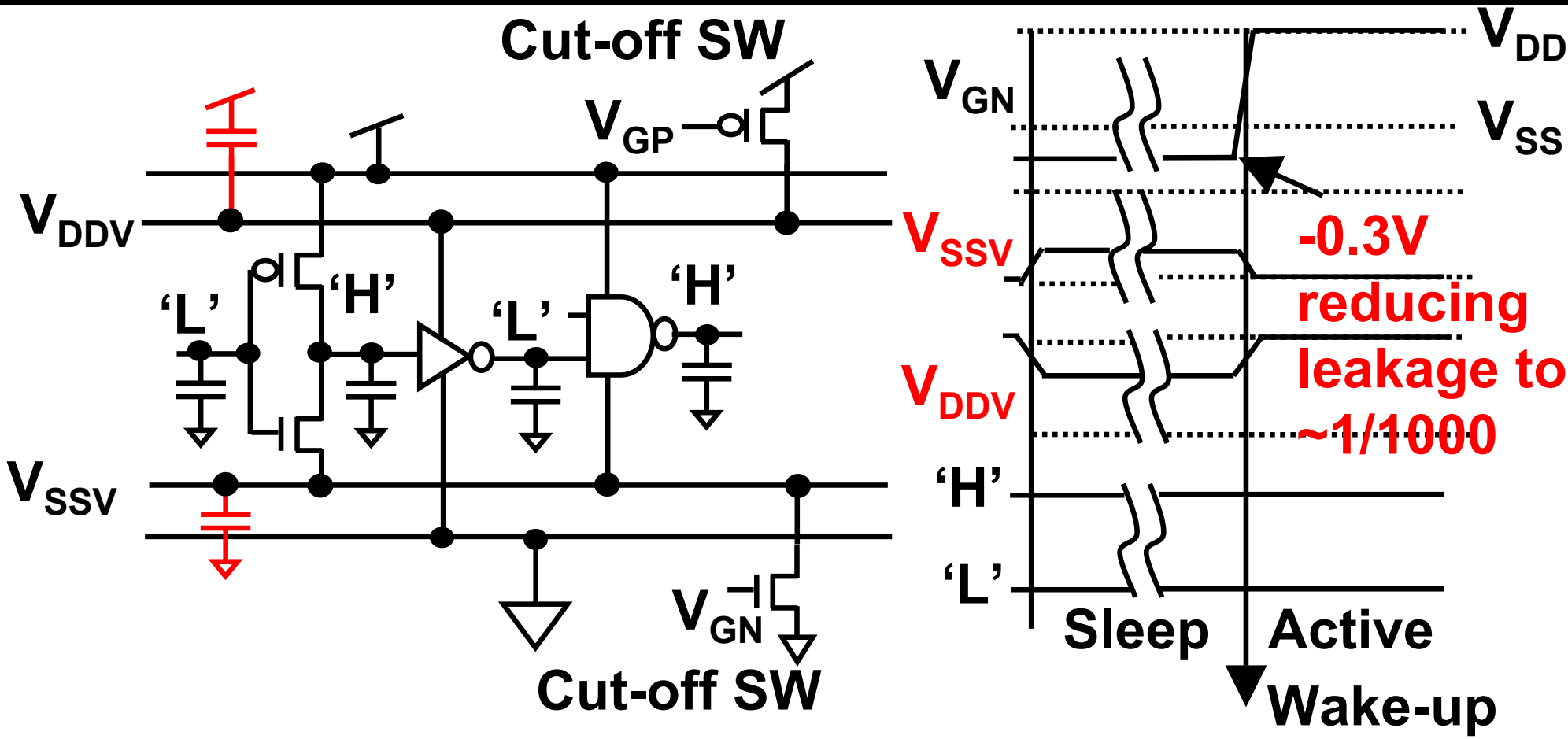
'H' nodes (not changed during sleep)



- Full swing of 'L' nodes and V_{SSV} nodes at wake-up

=> Long wake-up time and high rush current at wake-up

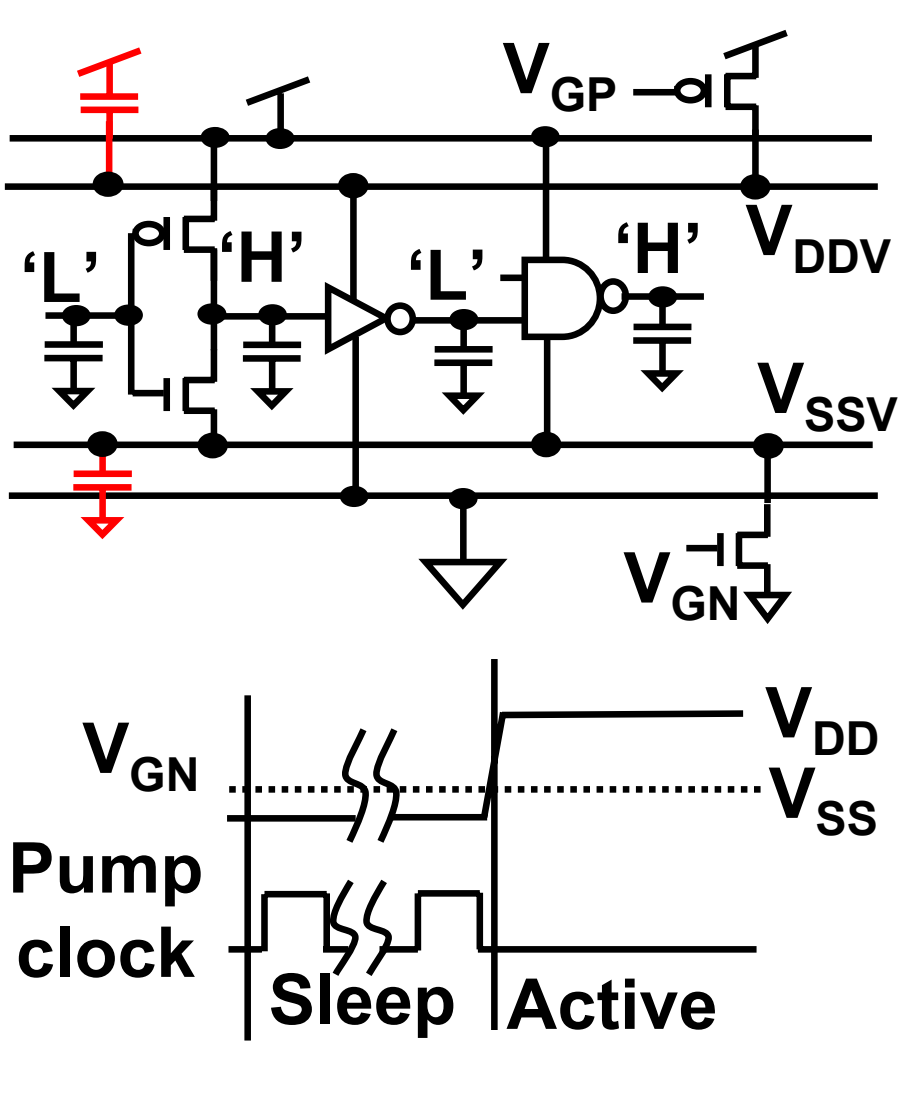
Zigzag Super Cut-off CMOS (ZSCCMOS)

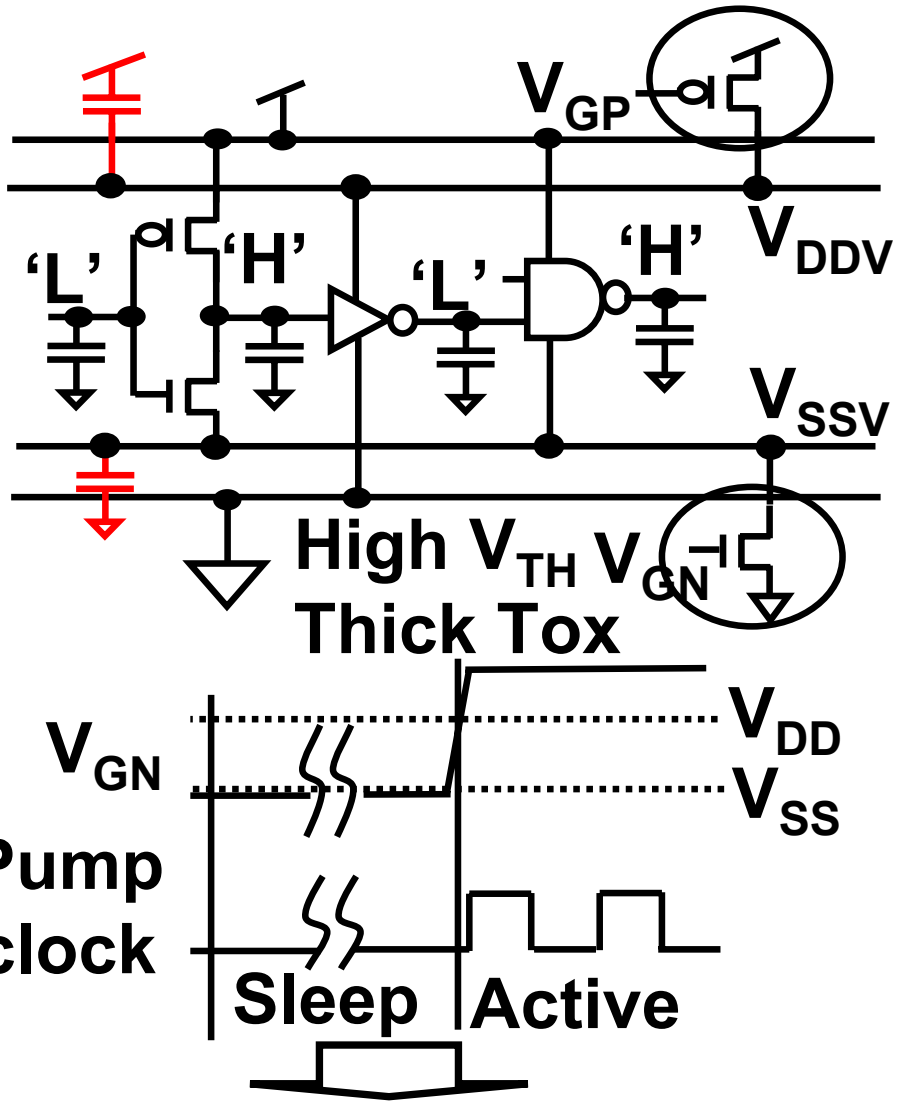


- Small voltage change of V_{SSV} and V_{DDV} due to reverse-source biasing effect
- No voltage change of 'H' and 'L' nodes at wake-up

=> Short wake-up time and low rush current at wake-up

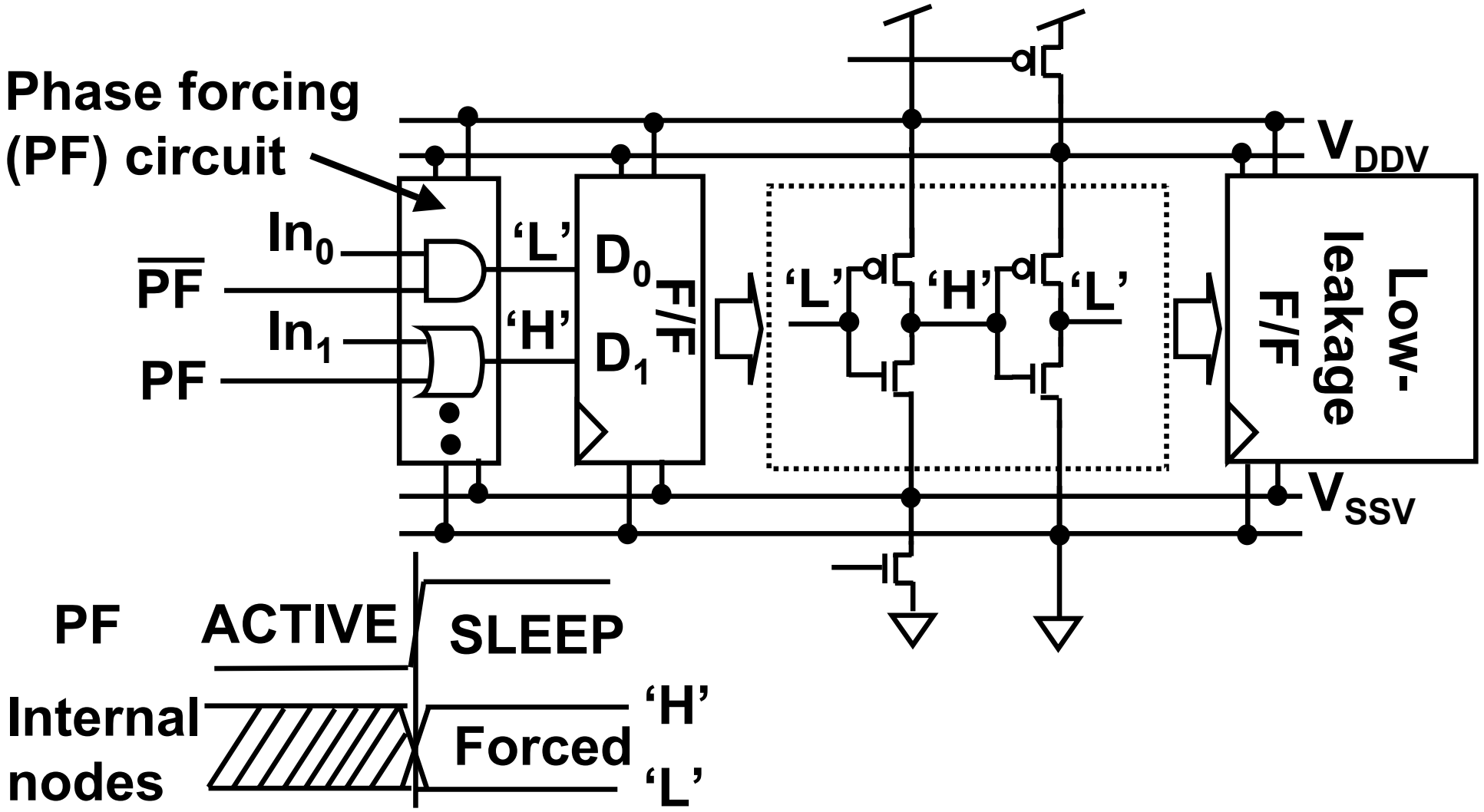
Derivative of ZSCCMOS (ZBGMOS)





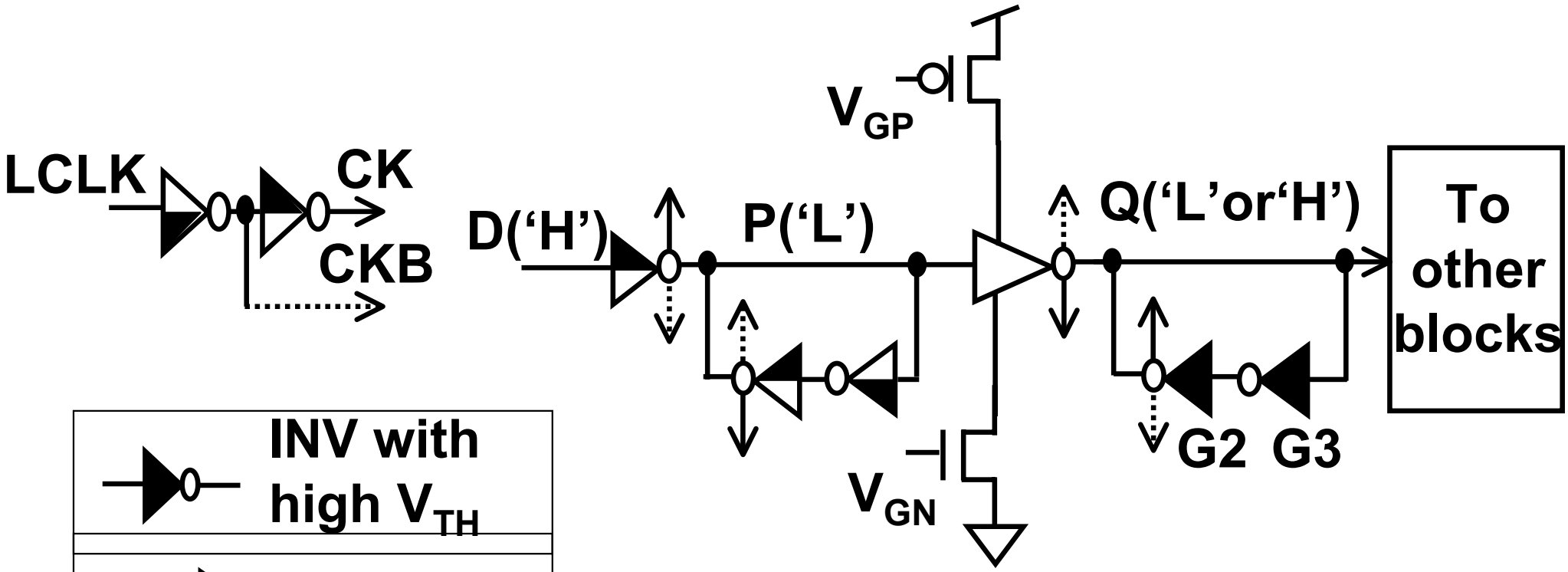
- **Not consuming pumping power during sleep**

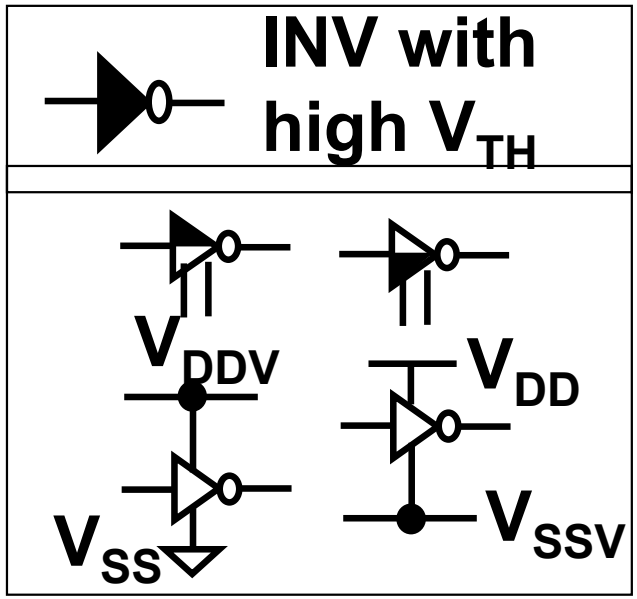
ZSCCMOS Block Activation Scheme with Phase Forcing



- Forcing every node to be 'L' or 'H' at sleep

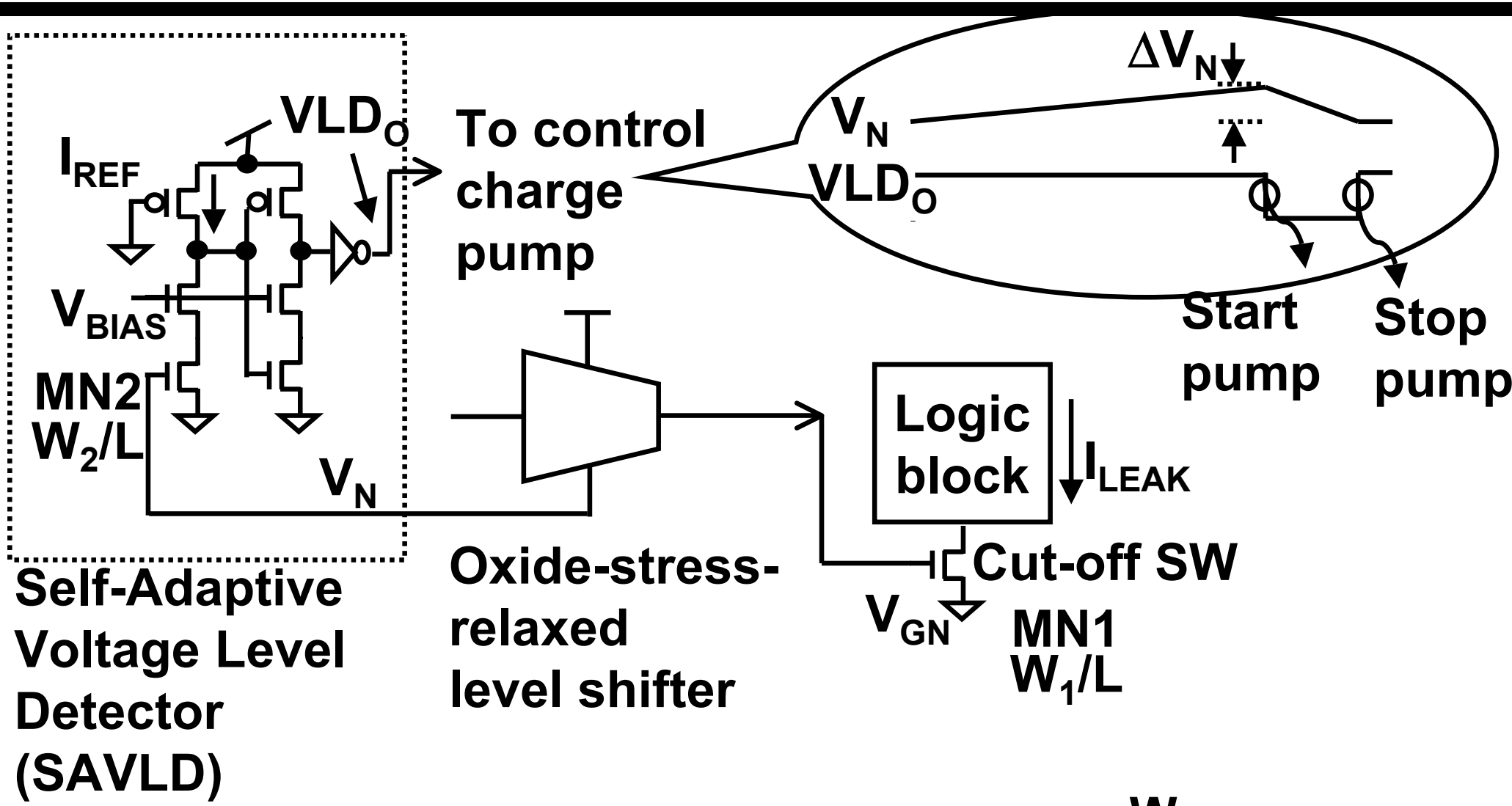
Low-Leakage Flip-Flop





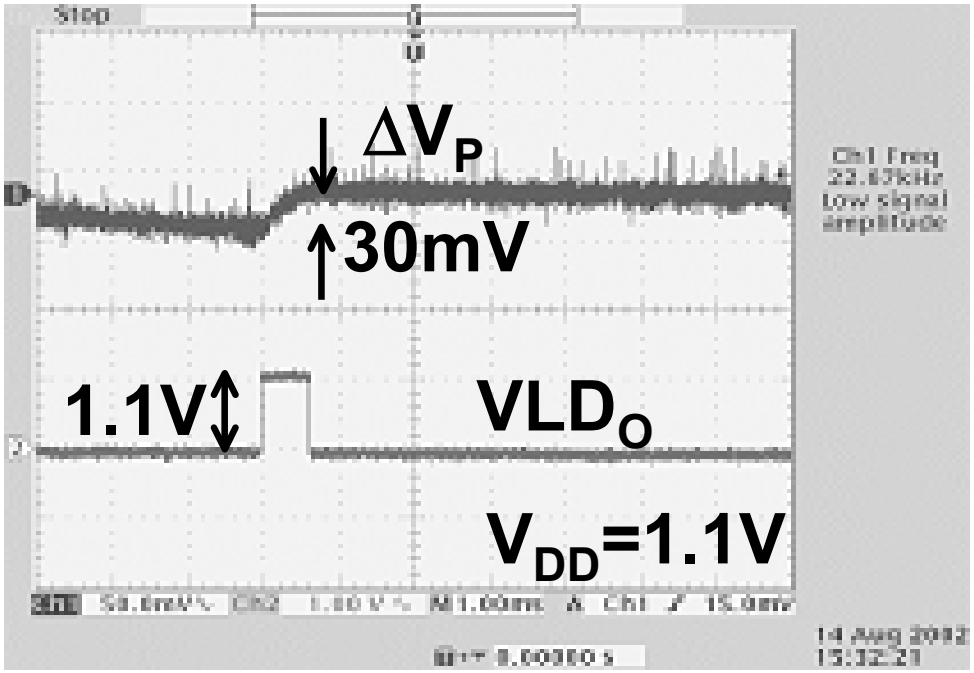
- Node Q not to be forced to 'H' or 'L' during sleep
- High-V_{TH} INV not on the critical path

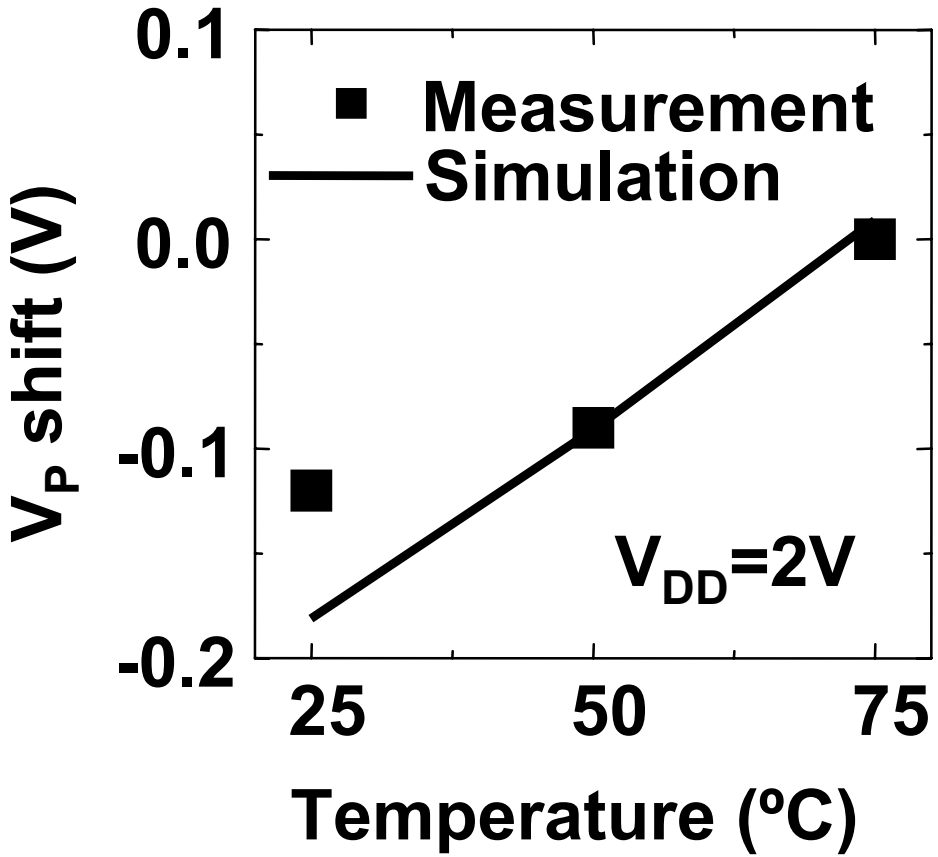
Control Circuit for NMOS Cut-off Switch



- Self-adaptively adjusting V_N as $I_{LEAK}\frac{W_2}{W_1} = I_{REF}$

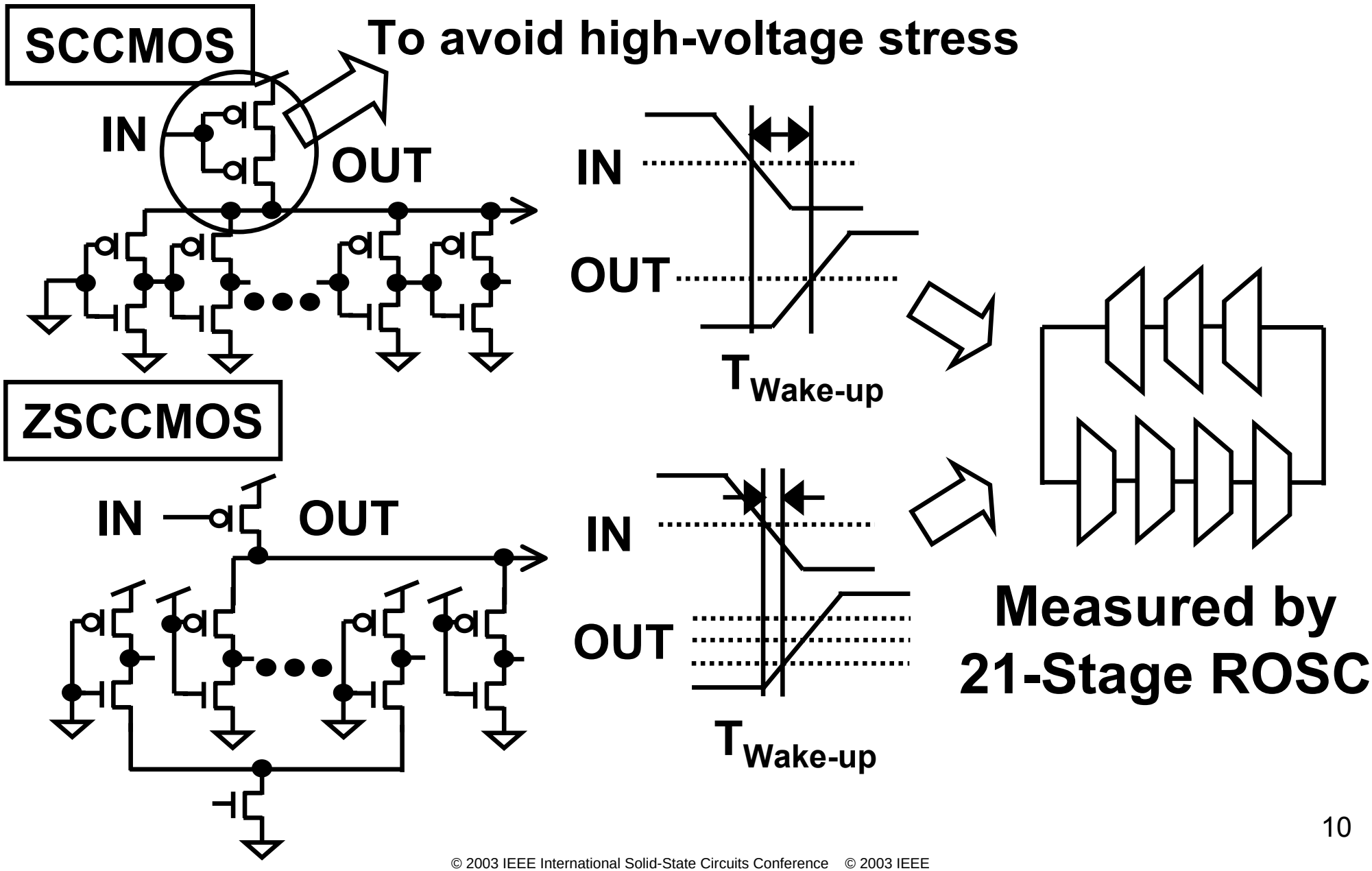
Measurement of Self-Adaptive V_P Level Detector



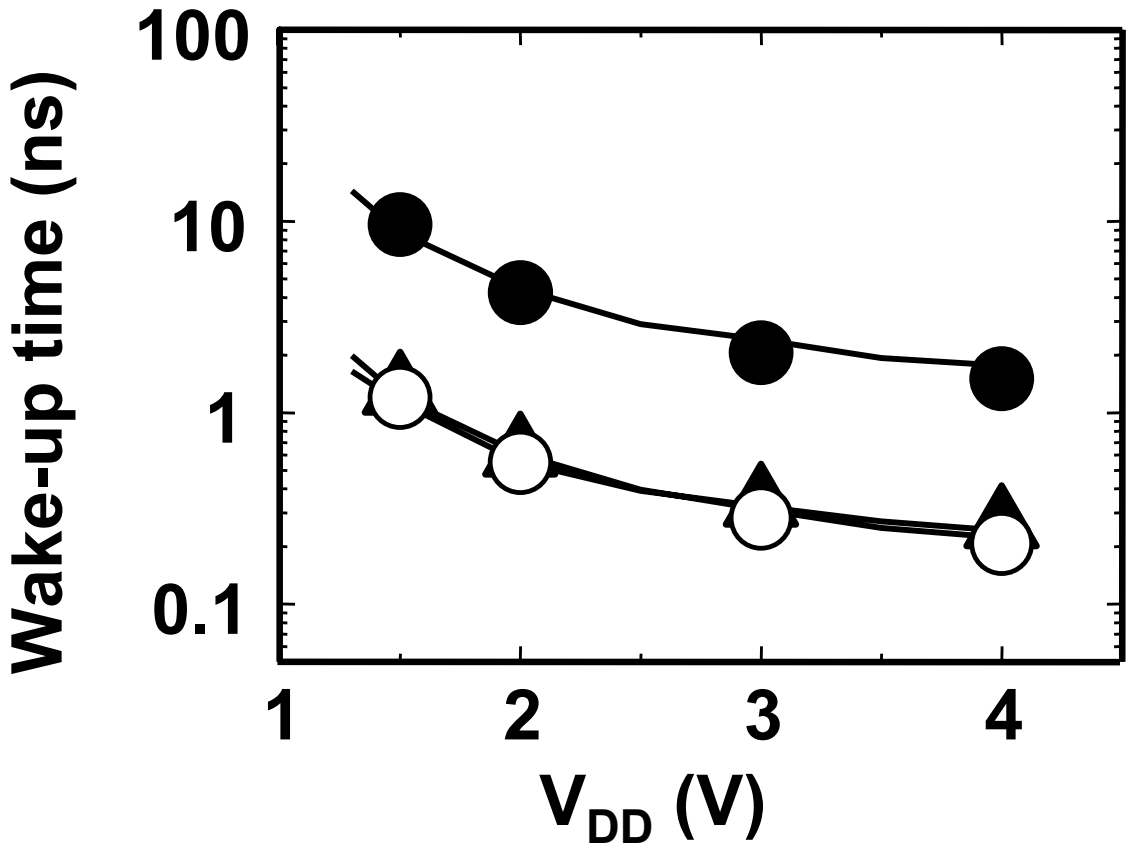


- Fabricated in 0.6-μm CMOS N-well process
- Self-adaptive V_P adjusting with varying temperature

Measurement Set-up



Comparison of Measured Wake-up Time



SCCMOS

ZSCCMOS

F.O.=3 INV

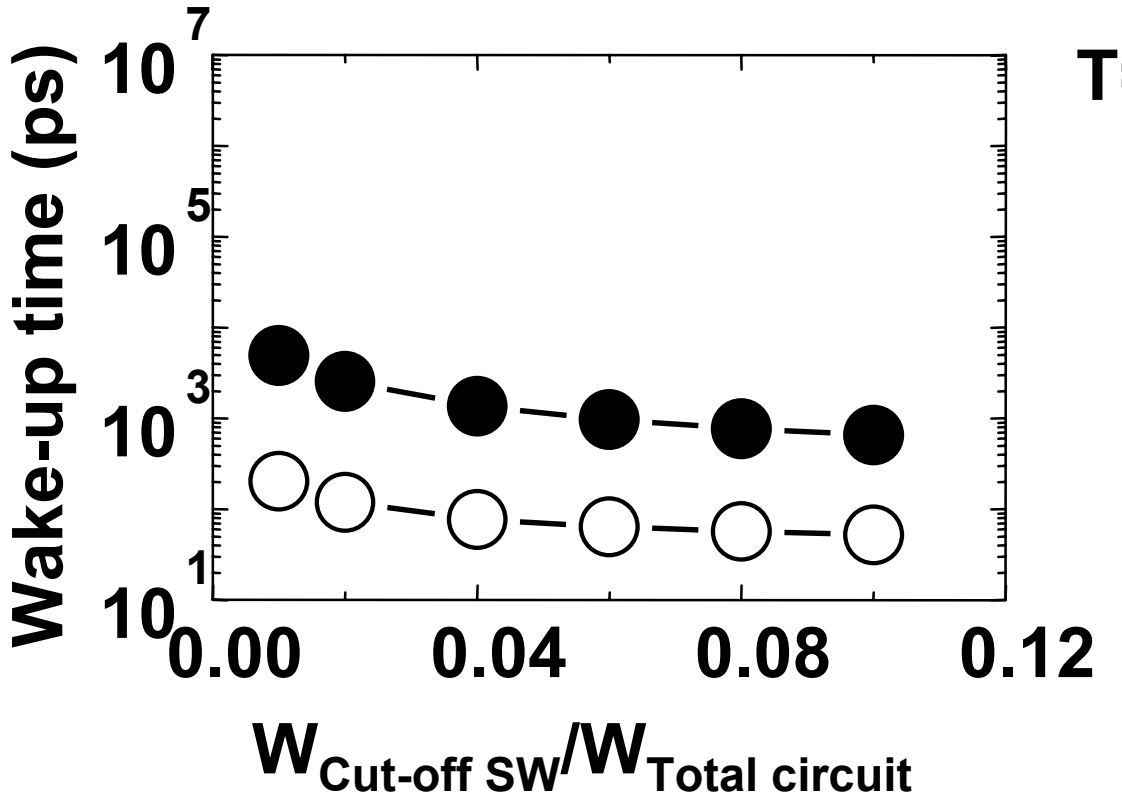
Simulation

$$\frac{W_{Cut-off\ SW}}{W_{Total\ circuit}} = 0.1$$

T=25ºC

- Fabricated in 0.6-µm technology
- 8 times shorter wake-up time of ZSCCMOS than SCCMOS

Comparison of Simulated Wake-up Time



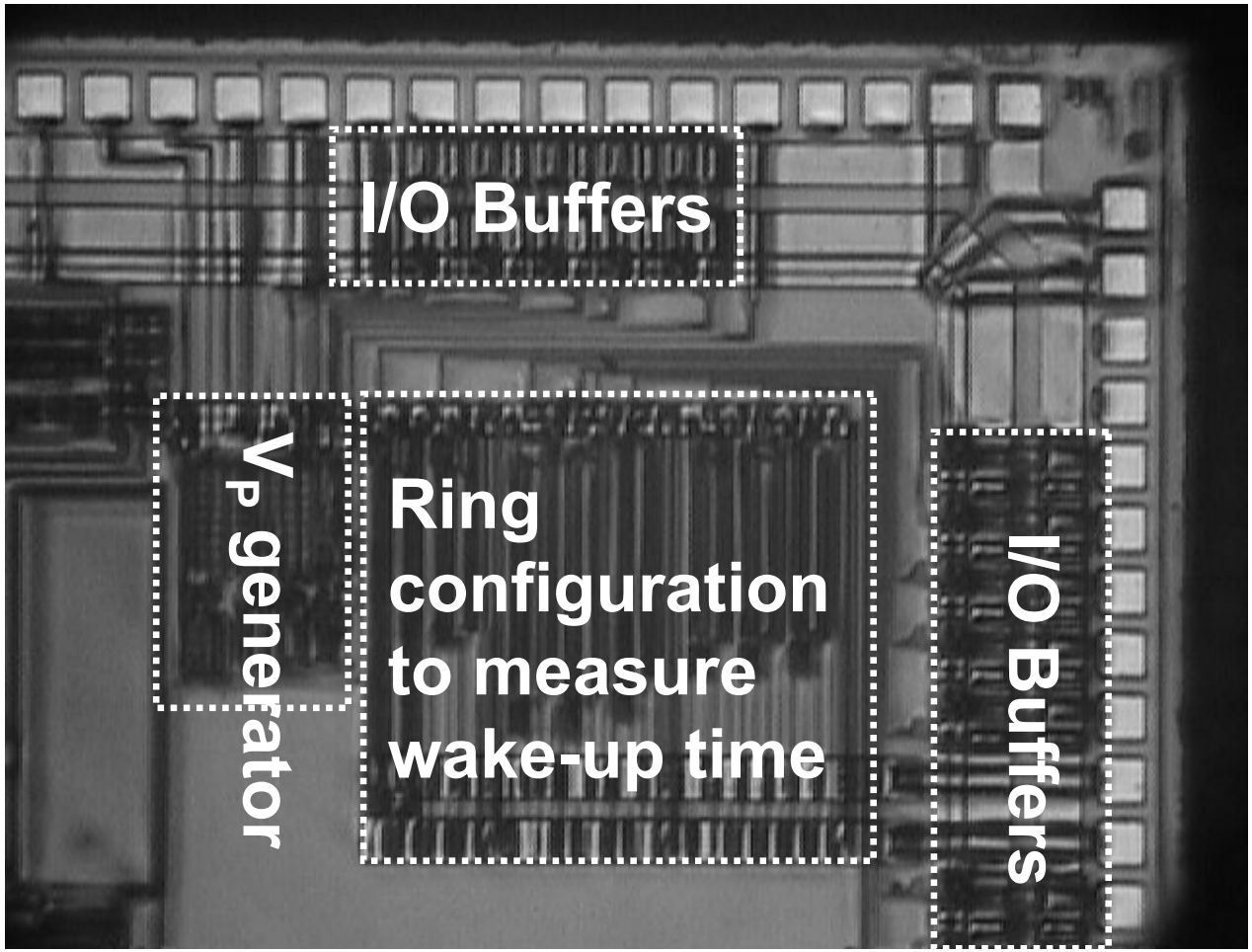
T=25°C V_{DD}=0.6V

● SCCMOS

○ ZSCCMOS

- Simulation by assuming 70-nm technology using Berkeley Predictive MOSFET Technology Model (BPTM)
- 12 times shorter wake-up time of ZSCCMOS than SCCMOS

Test Chip Micrograph



- **Fabricated in 0.6-μm CMOS technology**

Summary

- Zigzag scheme presented for leakage dominant era
- ZSCCMOS: ~200-ps wake-up time and smaller rush current than SCCMOS
- ZSCCMOS block activation scheme reduces leakage power to ~1/1000 when inactive.
- Gate voltage of cut-off SW self-adjusted so as to set I_{LEAK} constant over PVT variation