32.3 A Sheet-Type Scanner Based on a 3D Stacked Organic-Transistor Circuit with Double Word-Line and Double Bit-Line Structure

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An electronic artificial skin using organic field-effect transistors (OFETs) has been reported [1]. Recent advancement in the area is the integration of an OFET and organic photodiode (OPD) to realize a sheet-type scanner [2]. The thin sheet excludes heavy optical and mechanical parts and captures a black-and-white image on a paper. Although the basic function was demonstrated, a double wordline and bitline structure is introduced in the OFET sensor to reduce the line delay by a factor of five.

The device structure of the scanner and the acronyms for the various materials used are shown in Fig. 32.3.1. One OPD sheet and two OFET sheets are separately fabricated and glued together with silver paste. On the OPD sheet, a PEN base film is covered with ITO as a common anode. CuPc is p-type semiconductor and PTCDI is n-type one, forming the OPD [3, 4]. As a cathode, Au is deposited onto the OPD. The cathode is also a shield against direct incident light. Parylene passivates the OPDs through which a laser via passes. Additional top metals are connected to the OFET sheet1. The OFET sheets are fabricated as described in [1].

Light goes through the three sheets and then, reflected on the surface of the paper under scan. Black and white parts are discriminated by the difference of reflectance, which in turn modulates the amount of light to the OPD. The open area through which light passes is 45% of a total pixel area.

The circuit diagram of the proposed double WL/BL structure is shown in Fig. 32.3.2. For a 64×64 pixel array, WL and BL are both divided into eight blocks. A first WL (1WL) is connected directly to eight pixel selectors. A 1WL is selected by a 1WL selector, connected to a second WL (2WL). Similar notation is used for BLs. A 1BL is connected to an OFET amplifier that amplifies a 1BL voltage.

Although the hierarchical WL/BL structure is known for memories, the situation is different for sensor applications. In memories, the 1WL/1BL selectors are laid out by shifting memory cells to the sides. This is because memories are logical devices; for sensors, pixels can not be shifted because the pixel density changes and uniform sensing becomes impossible. Moreover, since the OFET is large, only one OFET is allowed per pixel or the open-area ratio becomes almost zero and light cannot enter the OPD. Thus, the 1WL/1BL selector OFETs are stacked on the pixel selector OFETs and a 3D stacked OFET sheet is essential.

Another technical challenge is that there are 1WL selectors, 1BL selectors, amplifiers and reset gates, all of which are placed in a single layer, the OFET sheet2. Regular array-like placement of the different kinds of OFETs is impossible but checkerboard-like pattern in Fig. 32.3.3 fulfills the requirements.

The serially-connected OFET decoder shown in Fig. 32.3.2 is introduced for lower power and higher speed operation than the parallel-connected one [1]. The configuration used does not draw active leakage because it is a dynamic circuit and does not require OFET sizing. The layout used is new so that cut-and-paste customization [1] is possible.

Figure 32.3.4 shows the delay optimization for the number of pixels per block, m, and the number of parallel OFETs used to make a 1WL selector, k. Values chosen are m=8, and k=1. For most cases, delay is optimized when m is about the square root of the total number of columns. When m is too large, 1WL delay becomes large, and when m is too small, 1WLS-bar delay becomes large. By introducing the double WL structure, the WL delay is reduced to 1/6 of the conventional single WL scheme. The double WL/BL design potentially reduces power as well since capacitance associated with the operation is reduced. This becomes especially important when random access is employed for intelligent image capturing.

The measured I-V characteristics of the pixel selector and OPD are shown in Fig. 32.3.5. V_{OPD} is restricted to 35V to avoid the Zener avalanche breakdown of the OPD. In silicon imagers, a charge transfer amplifying scheme is exploited to amplify a small charge induced by a silicon photodiode; however in OFET, realization is precluded since gate capacitance is huge. Instead, a current sensing technique is adopted. Before evaluating a photocurrent of an OPD, 1BL is precharged to V_{DD} with the boosted reset signal, $\overline{R}$. Then, one of the eight 1WLs is selected to "L". I_{WHITE} (I_{BLACK}) exists in the pixel selector and OPD when the paper is white (black). Then, $\overline{R}$ turns off, and 1BL voltage starts to decrease. The speed of the voltage decrease depends on I_{WHITE} and I_{BLACK}. The voltage decrease of 1BL is amplified by the amplifier, which starts to pull-up the 2BL voltage. The pull-up speed is a function of I_{WHITE} and I_{BLACK}, and thus we can know if the paper is either white or black.

The measured waveforms are shown in Fig. 32.3.6 together with a sketch of the stimulus signals in which $block_{11}$ is selected. Successful operation is observed and both the conventional single WL/BL and proposed double WL/BL devices are manufactured for comparison. The fall time of 1WL in the double WL/BL scheme is 3ms and 17ms in the conventional single WL scheme; i.e., the WL delay is more than a factor of five shorter in this design. When the sense voltage is 30V, in the double WL/BL scheme, the measured access time is 6ms and cycle time 7ms. Alternatively, using a single WL results in 35ms and 39ms, respectively. Measured power for this design is 900μW at a 7ms cycle and 350μW at a 39ms cycle. The conventional method only achieves 2.5mW at a 39ms cycle and is seven times that of the double WL/BL technique.

Figure 32.3.7 shows photographs of the scanner before assembly as well as a cross-section of the three stacked sheets. The pixel size is 1.27 × 1.27 mm² and total area is about 80 × 80 mm². In the future, one expects that the number of pixels per WL/BL to exceed 2048, and pixel size reduced by a factor of at least 16. The delay of the double WL/BL design using stacked OFET sheets should reduce the delay of an order or 10^3 seconds by a factor of several tens. The power consumption may also be decrease by the same factor. This design approach is applicable to other types of large-area OFET sensors including artificial skin and may solve fundamental issues in large-area sensor electronics.

Acknowledgements:
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References:
[1] T. Someya et al., "Cut-and-Paste Organic FET Customized ICs for Application to Artificial Skin," *ISSCC Dig. Tech. Papers*, pp. 288-289, Feb., 2004.
[2] T. Someya et al., "A Large-Area, Flexible, and Lightweight Sheet Image Scanner Integrated with Organic Field-Effect Transistors and Organic Photodiodes," *IEDM*, Session 15.1, Dec., 2004.
[3] Z. Bao et al., "Organic Field-Effect Transistors with High Mobility Based on Copper Phthalocyanine," 69, 3066, *Appl. Phys. Lett.*, 1996.
[4] J. Shinar, "Organic Light-Emitting Devices: A Survey," Springer, 2003.

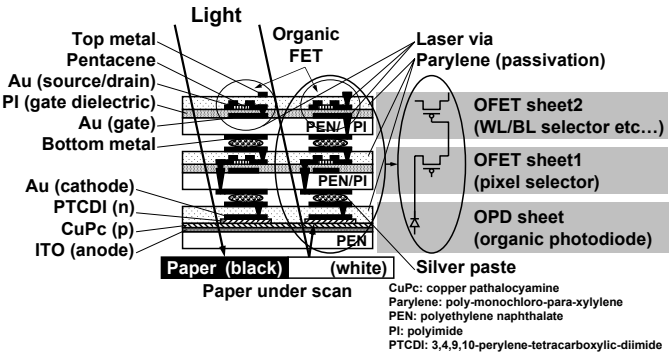

Figure 32.2.1: Device structure and corresponding circuit.

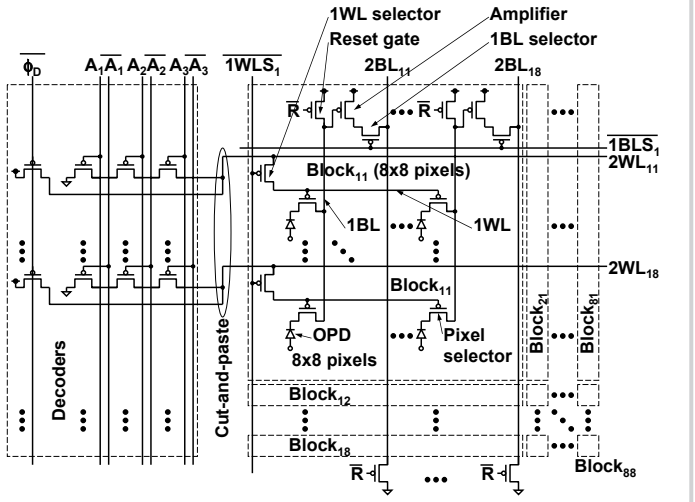

Figure 32.3.2: Circuit diagram.

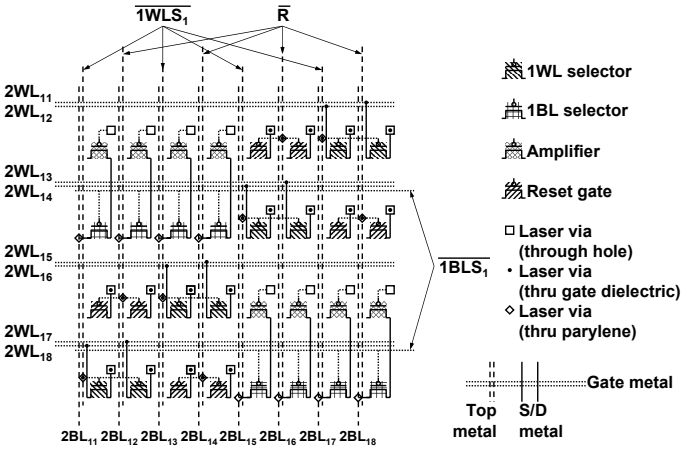

Figure 32.3.3: OFET sheet2 layout of 8 x 8 pixels in block.

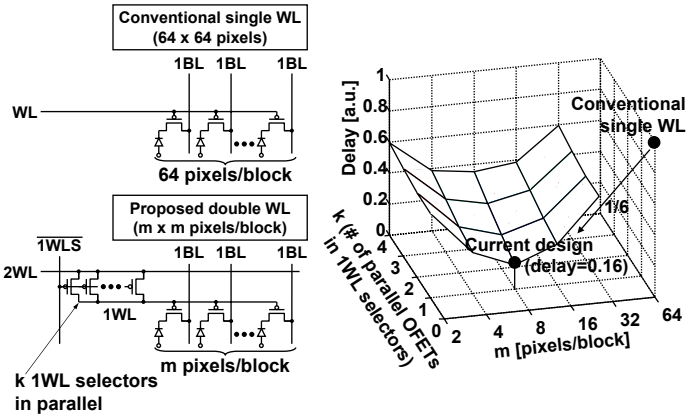

Figure 32.3.4: Simulated line delay in double WL structure.

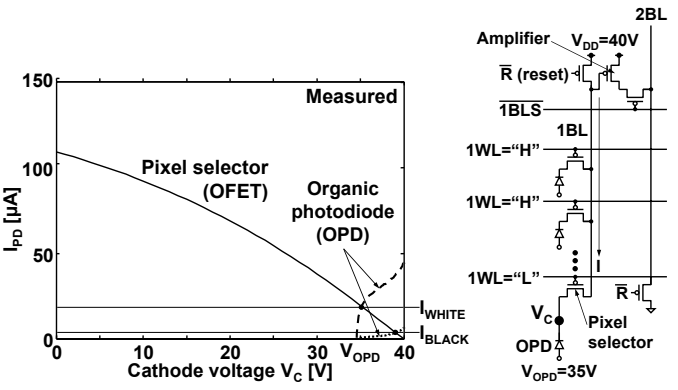

Figure 32.3.5: Measured I-V characteristics of pixel selector OFET and OPD, and operation points on 1BL.

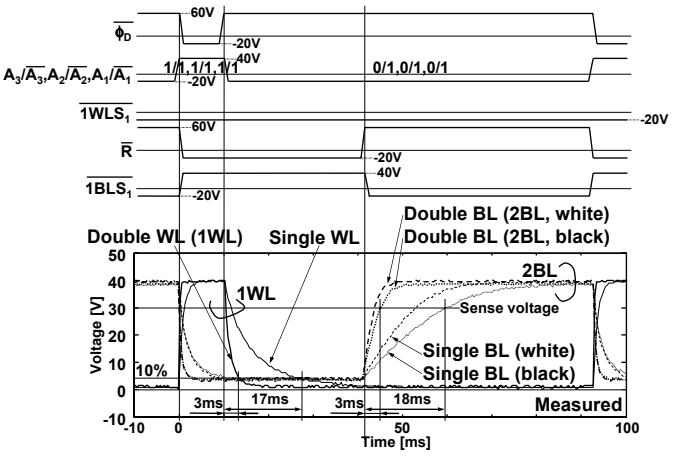

Figure 32.3.6: Measured operation waveforms.

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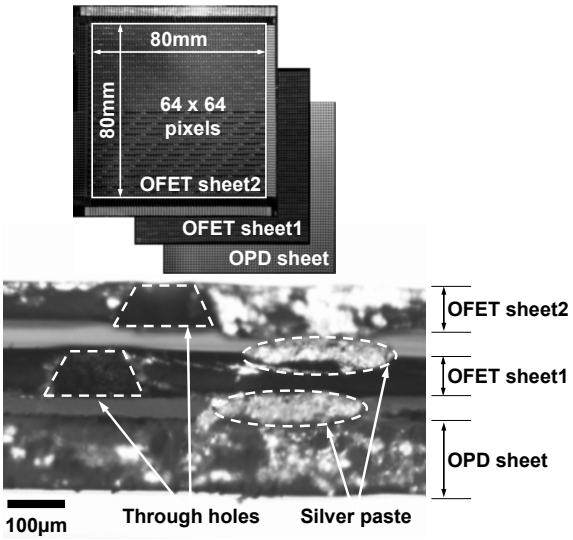

Figure 32.3.7: Photograph of fabricated scanner system and cross sectional view.

