An Organic FET SRAM for Braille Sheet Display with Back Gate to Increase Static Noise Margin

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Outline

- **Large Area Electronics Using Organic FETs**
- **Braille Sheet Display (BSD)**
- **Key Circuit Technologies for BSD**

  (1) 5-transistor SRAM Cells and Pipelining for Write-Operation

  (2) Control of SRAM Static Noise Margin with A Back Gate

  (3) Overdrive Techniques for Driver Transistors
- **Summary**

Organic FETs (OFETs)

	OFETs	Si MOSFETs
Design rule	50 μm	90 nm
Hardness	Flexible (a)	Solid
Drive current	25 nA / μm @ 40 V	1 mA / μm @ 1 V
Gate delay	0.3 ms	10 ps
Cost / area	Low (b)	High
Cost / transistor	High	Low
Lifetime	Days	Years

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What is the application of OFETs that utilizes (a) and (b)?

Large Area Electronics

- Functional units are distributed on a square, 10 cm – 10 m on a side.

Pressure sensors + OFETs **Photodetectors + OFETs**

Our previous works

Artificial skin (ISSCC2004)

Scanner (ISSCC2005)

This work

Actuators + OFETs

Braille display

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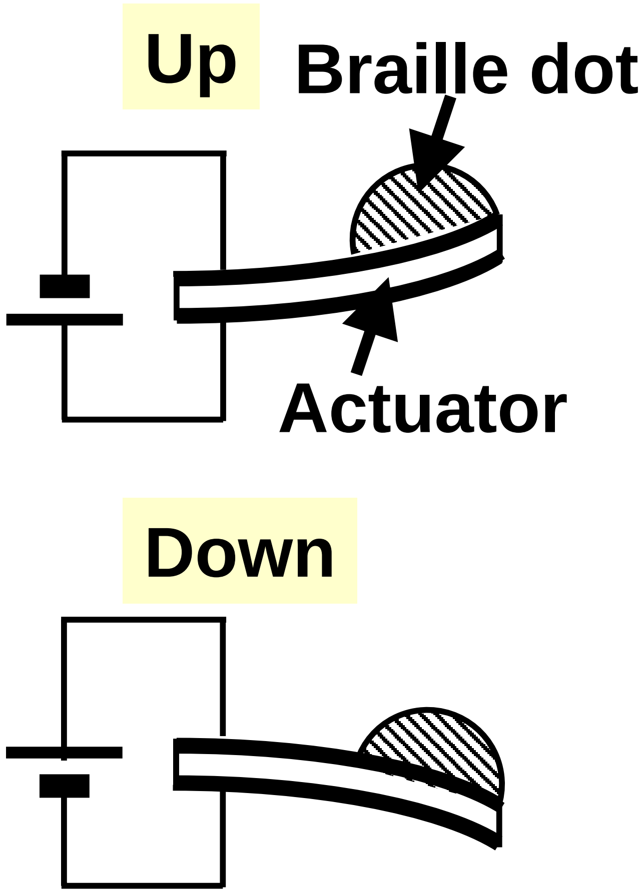
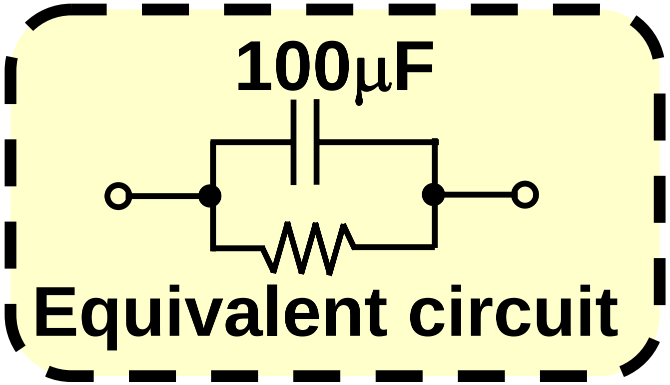
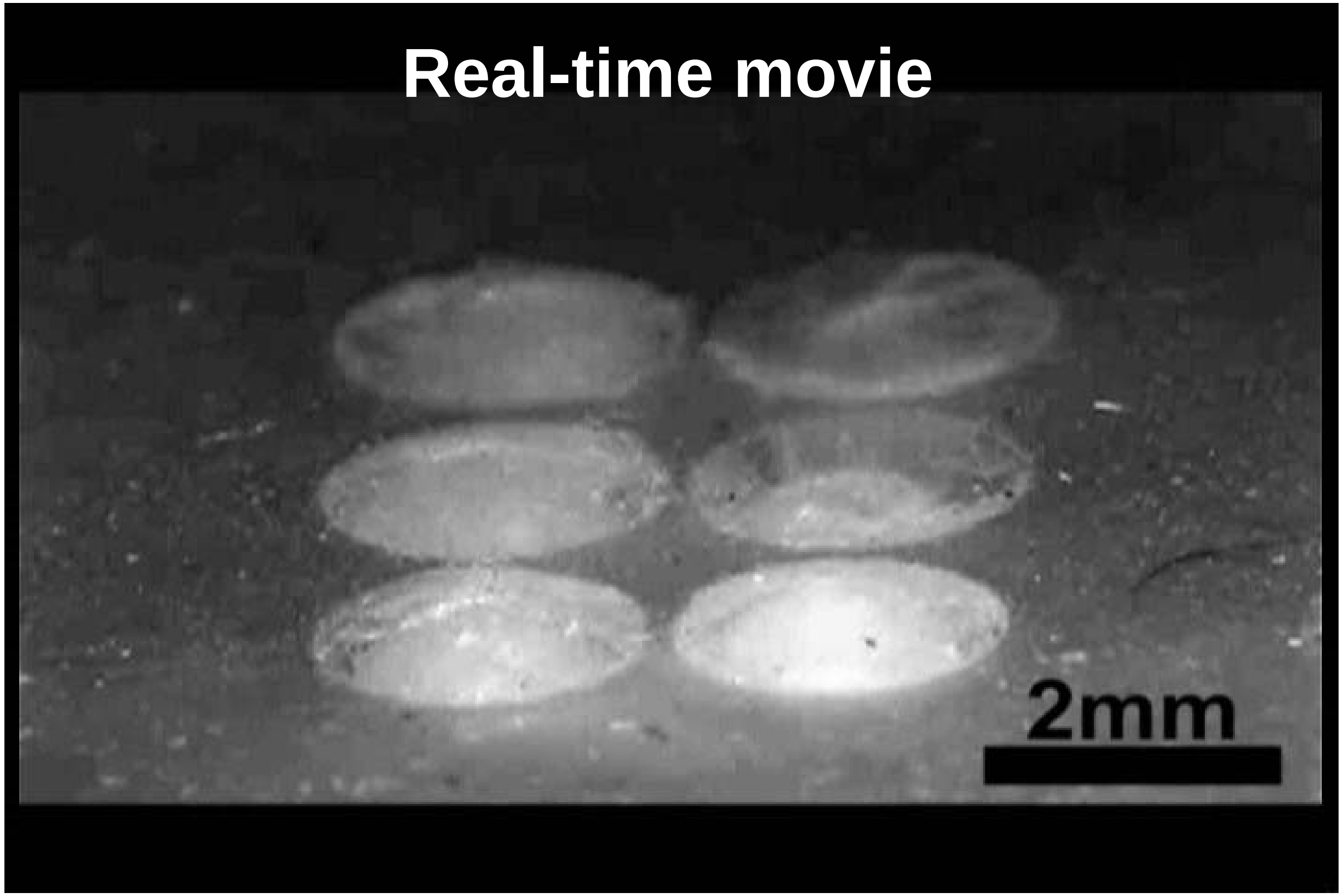
Plastic Actuators

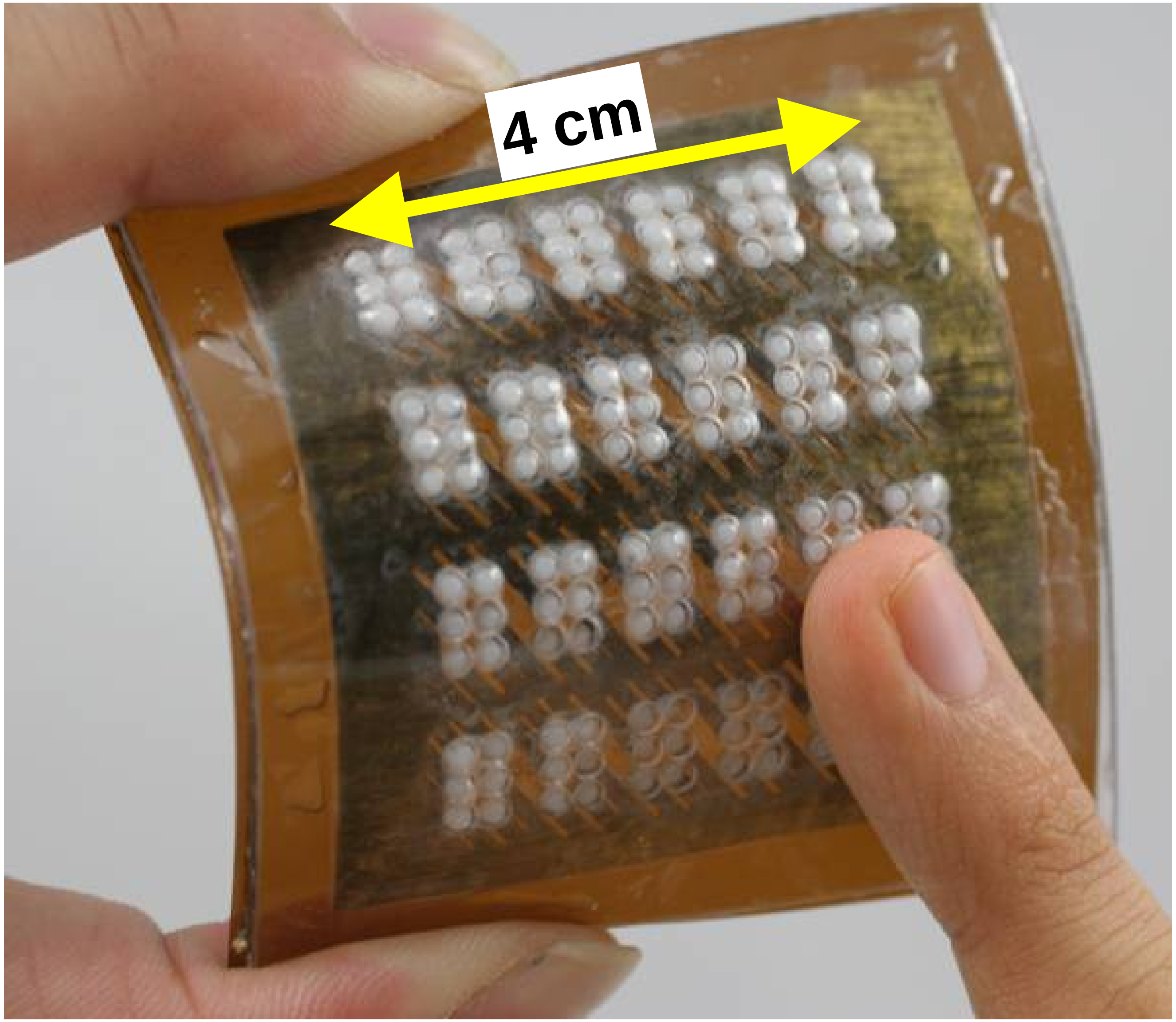






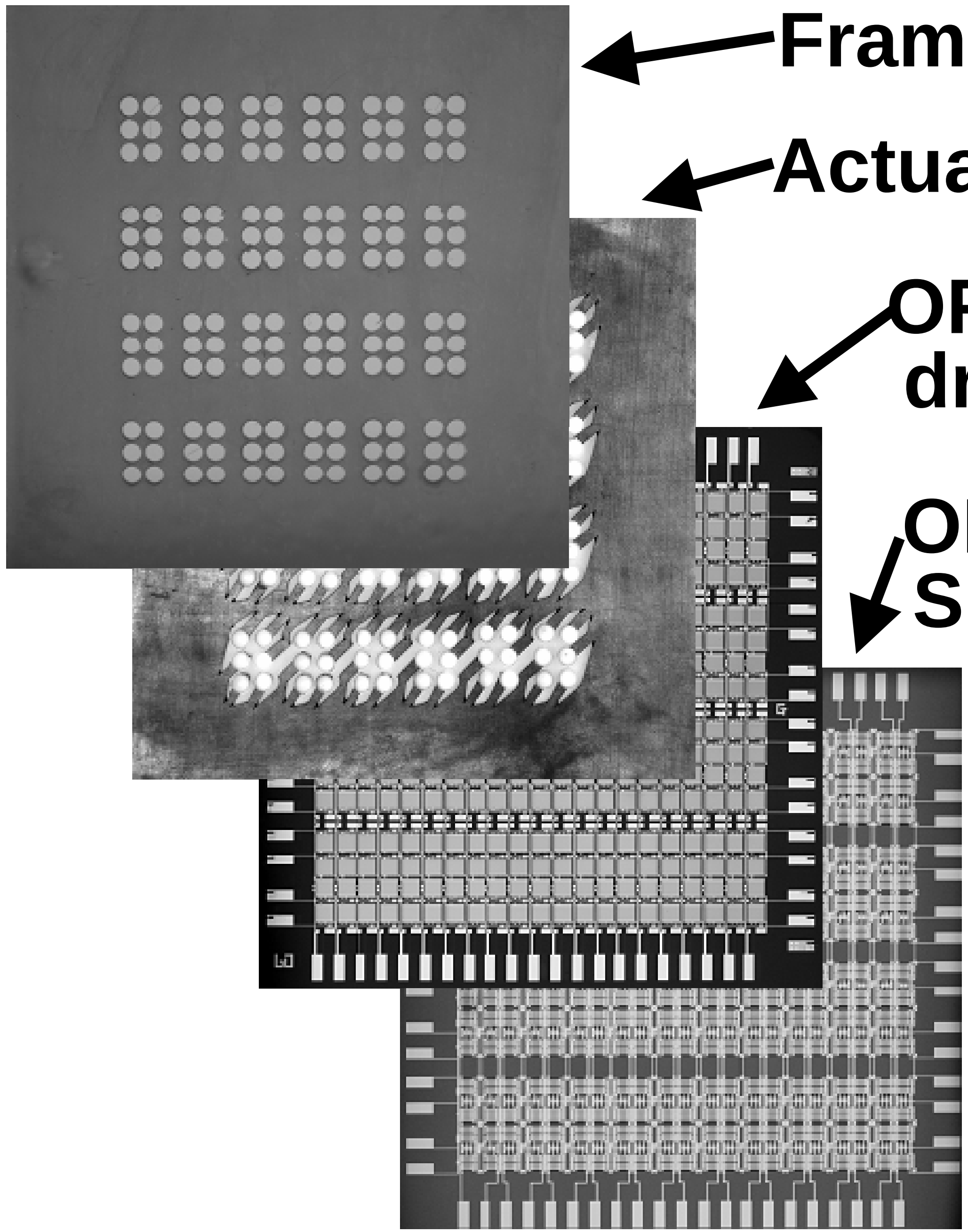
- The displacement of the actuators to read Braille is 0.2 mm.

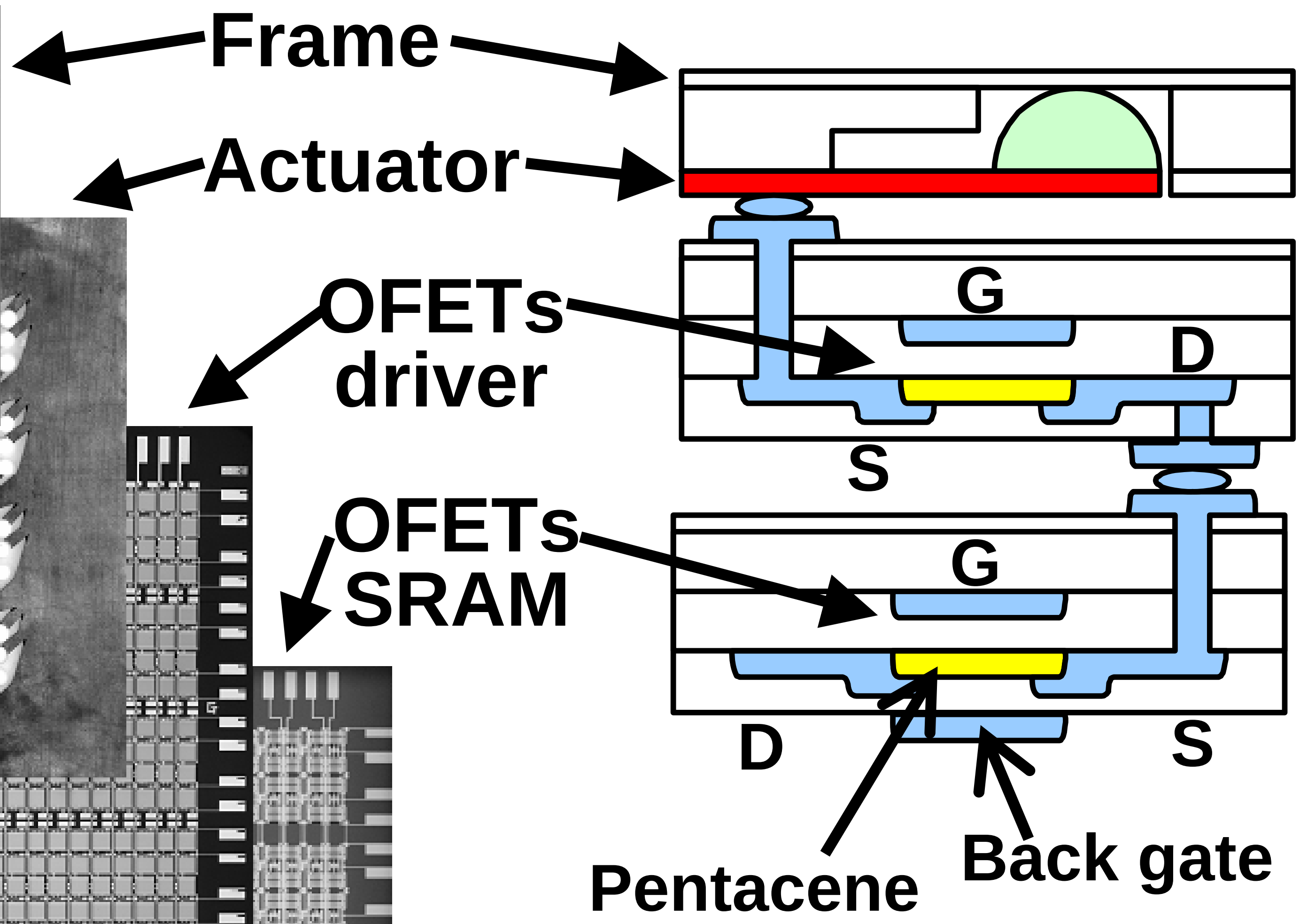
Developed Braille Sheet Display



- **6 x 4 Braille characters**
- **Each Braille character consists of 2 x 3 dots, and the display has a total of 144 dots.**
- **Thickness: 1 mm**

Device Structures

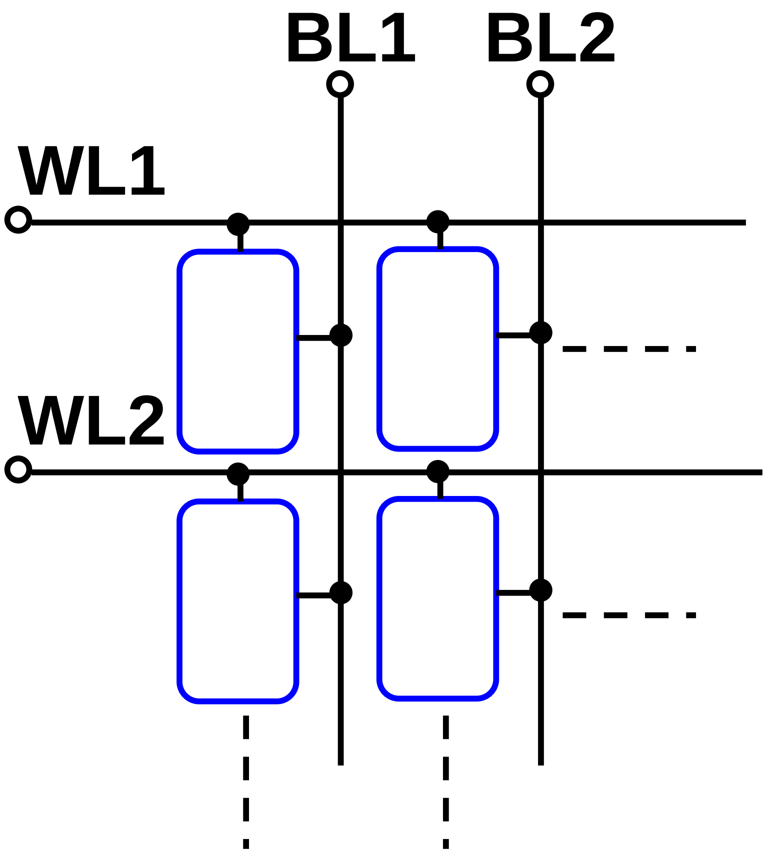




- 4 films are stacked.

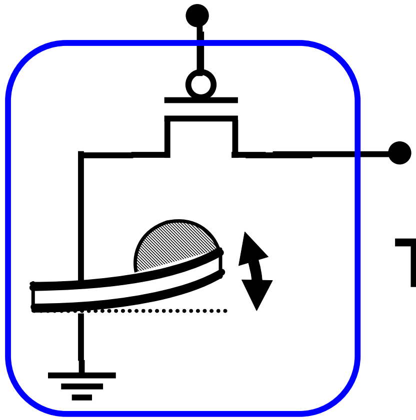
Why SRAM?

12 x 12 Braille dots array



T1: Time to change 144 Braille dots

w/o SRAM

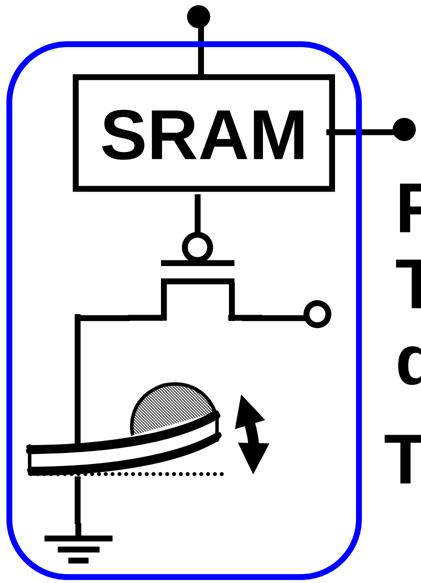


Sequential drive of actuators

T1 = 34 s x 144 = 4896 s

1/122

with SRAM



First, SRAM writiting.
Then, simultaneous drive of all actuators.

T1 = 5.76 s + 34 s = 40 s

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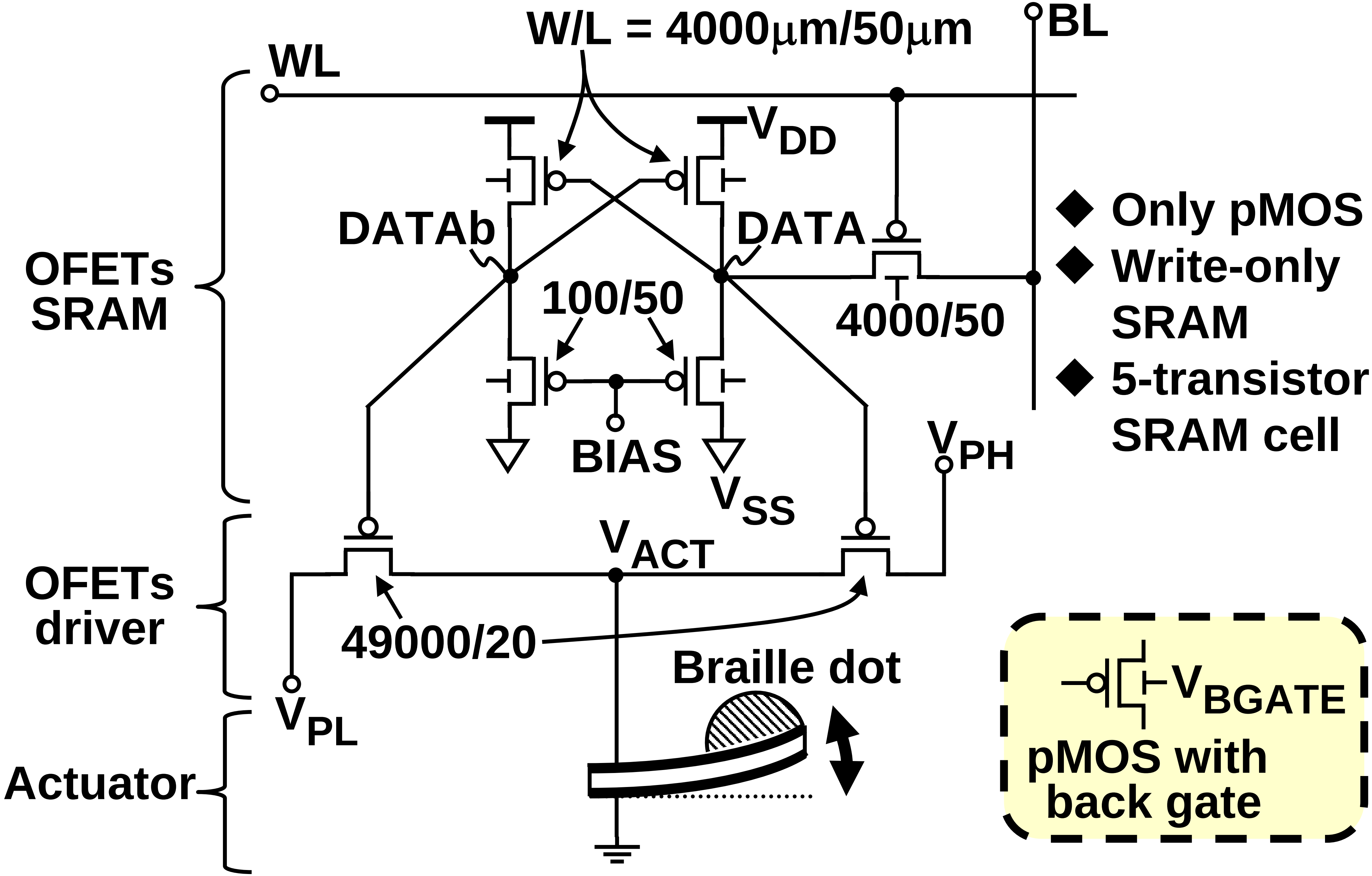
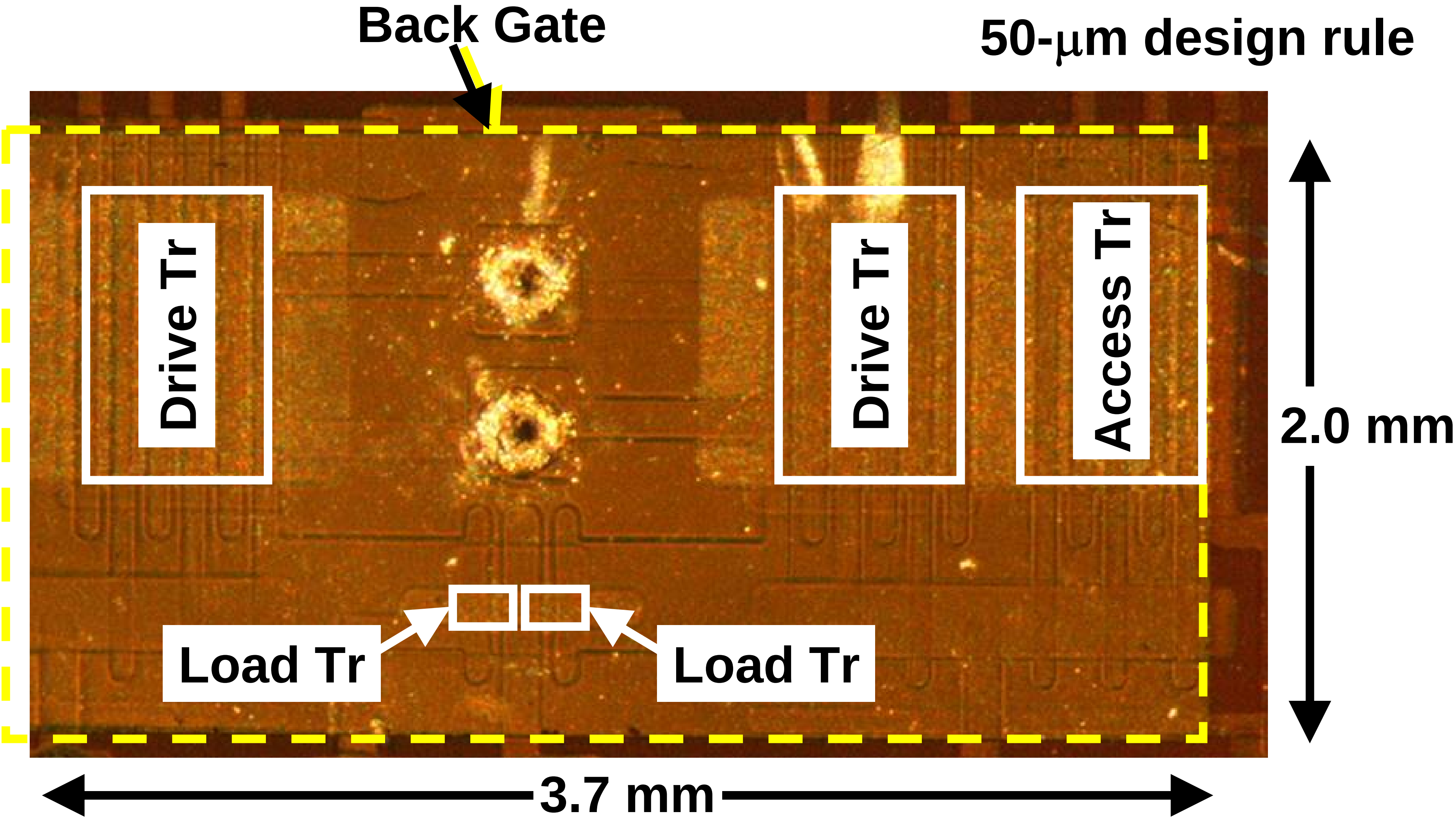
Unit Circuit for An Actuator



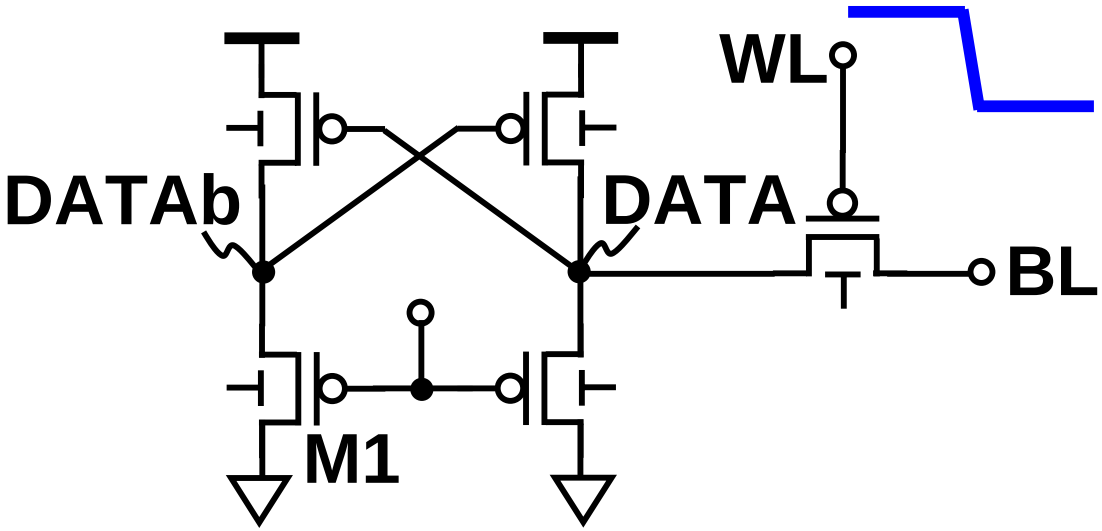
- Only pMOS
- Write-only SRAM
- 5-transistor SRAM cell

5-Tr SRAM Cell

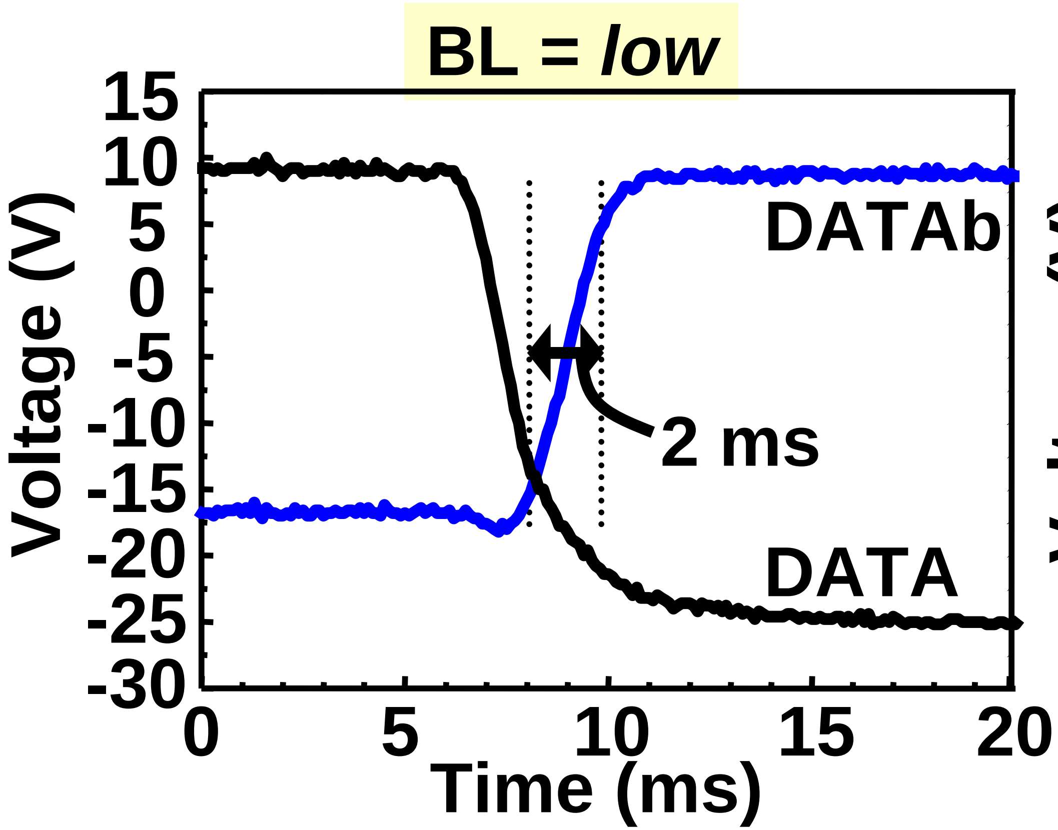


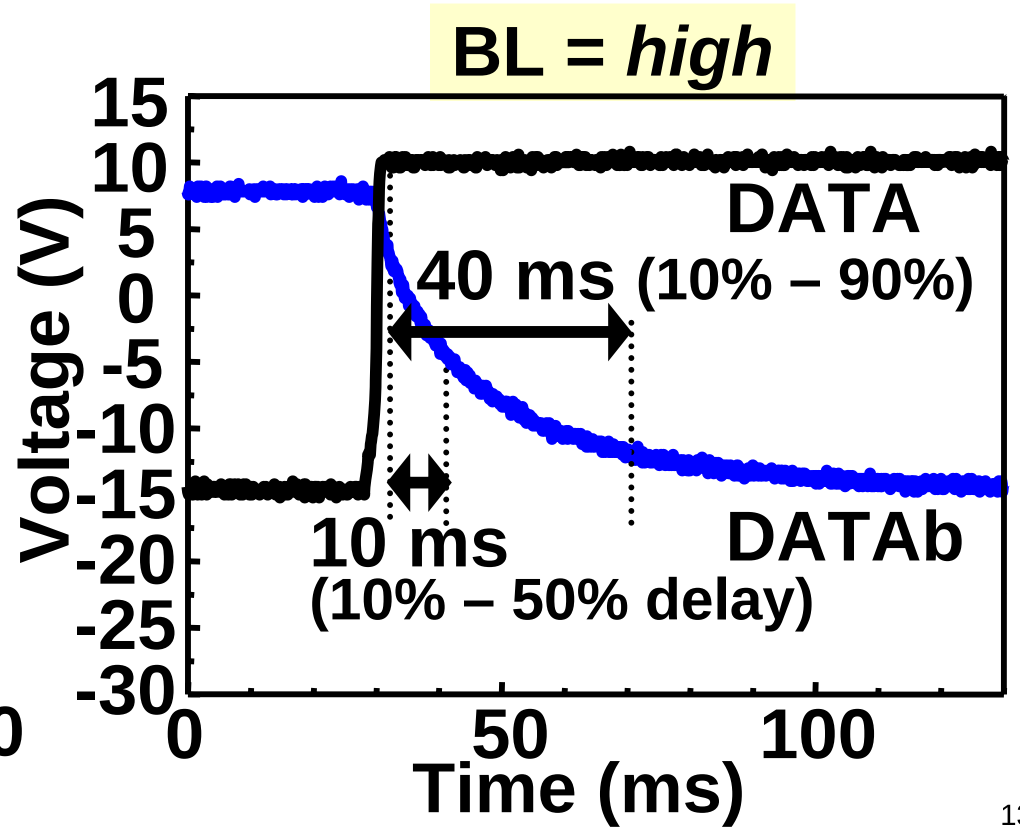
- **Compared with the conventional 6-Tr SRAM cell, 5-Tr SRAM cell reduces the cell area by 20%.**

Issue of 5-Tr SRAM Cell



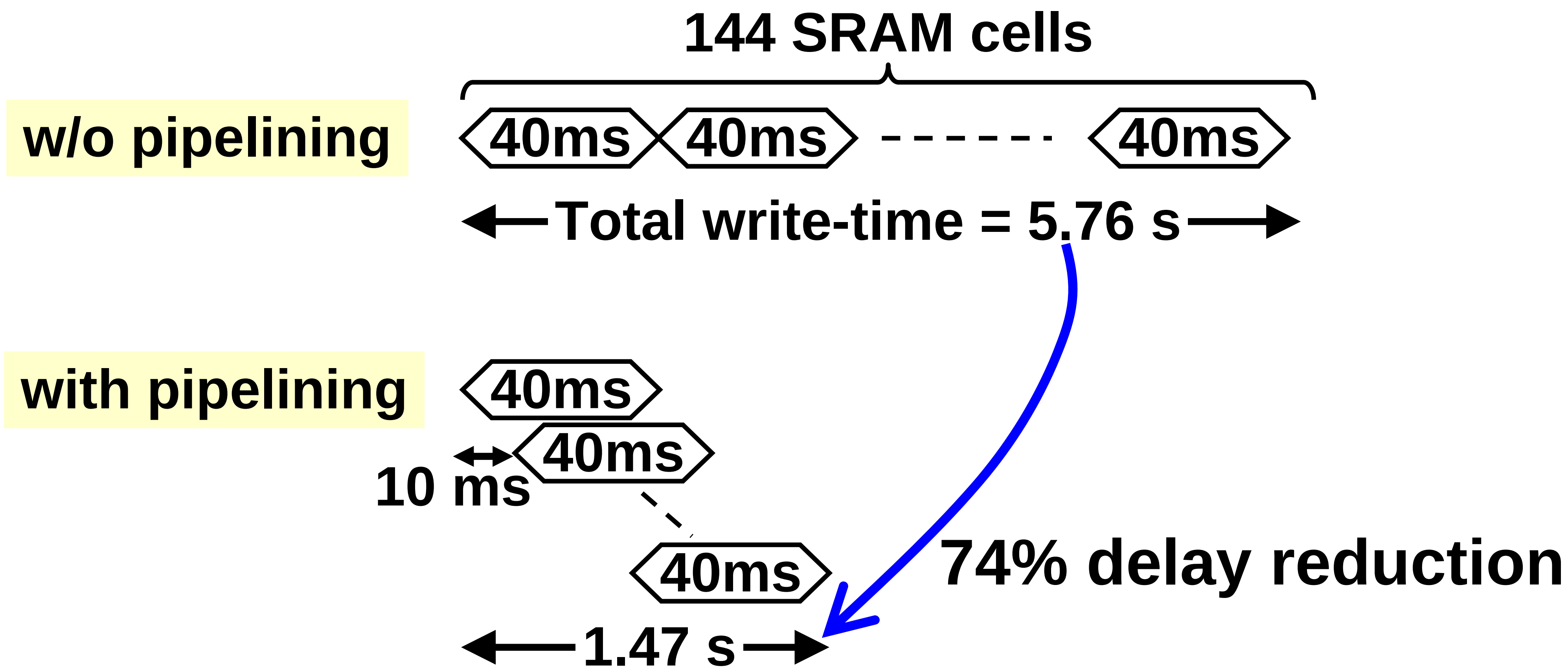
- Slow write-operation was measured, when BL is high.





Pipelining for Write-Operation

- Design target for the write-time of the whole SRAM (= 144 cells) is within 2 s.



- The slow transition time can be hidden by pipelining the write-operation.

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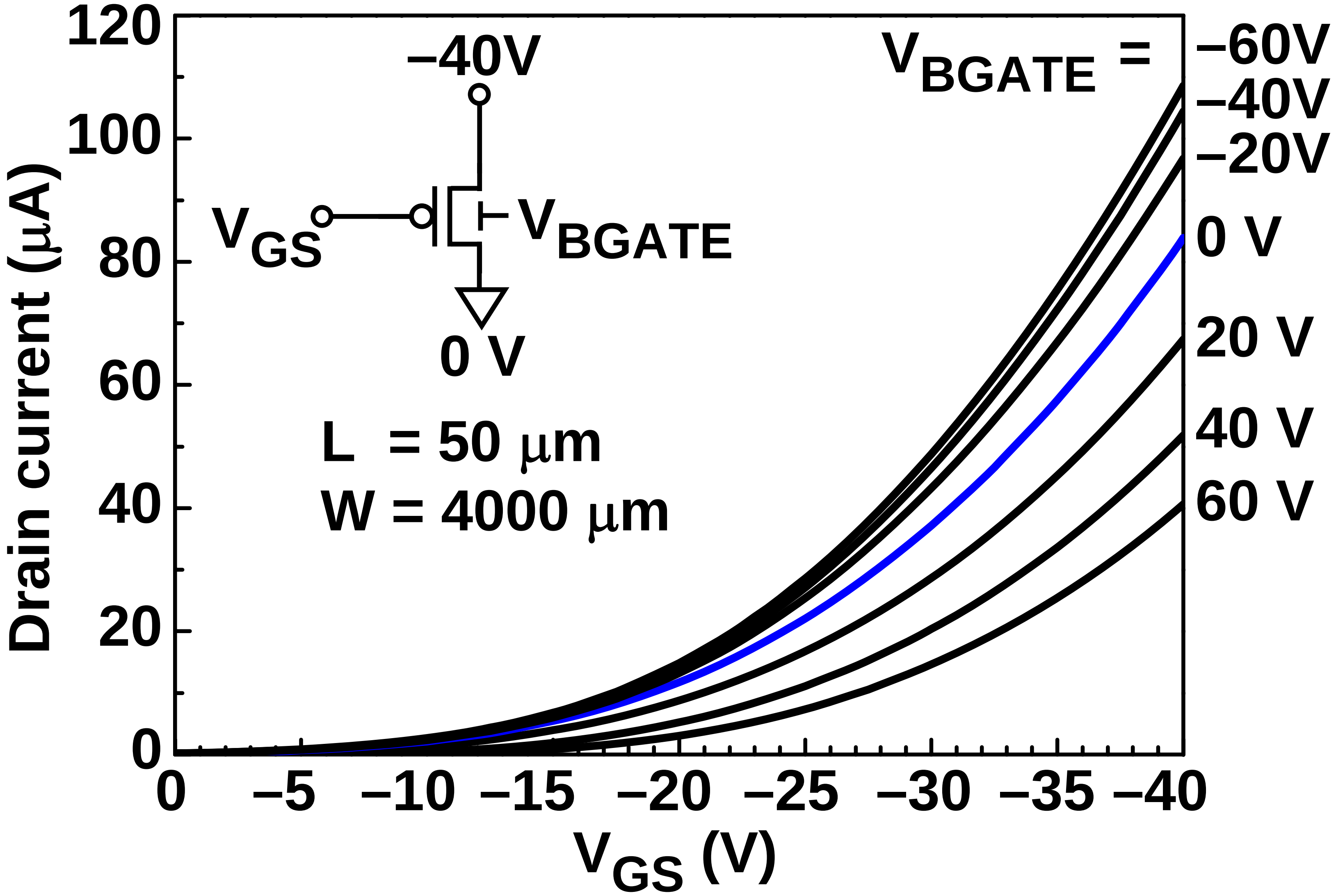
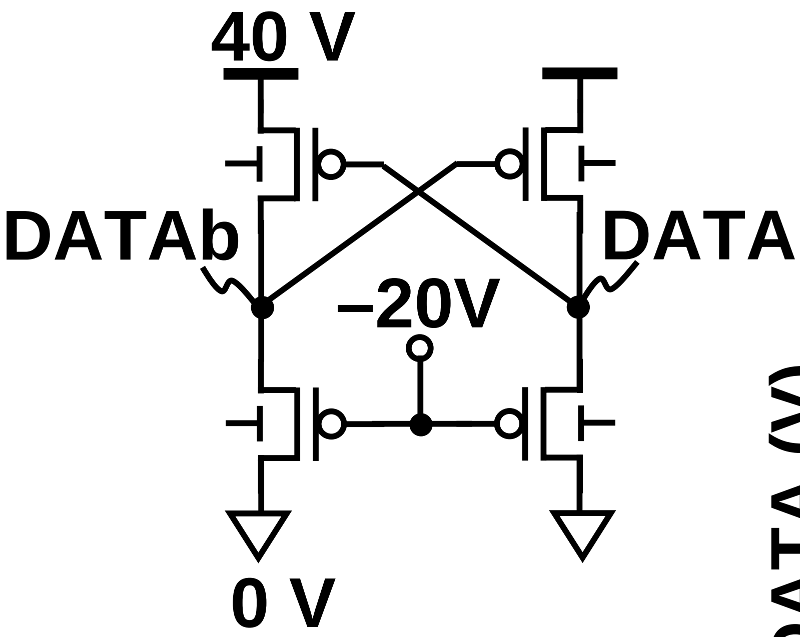
PMOS OFET with Back Gate

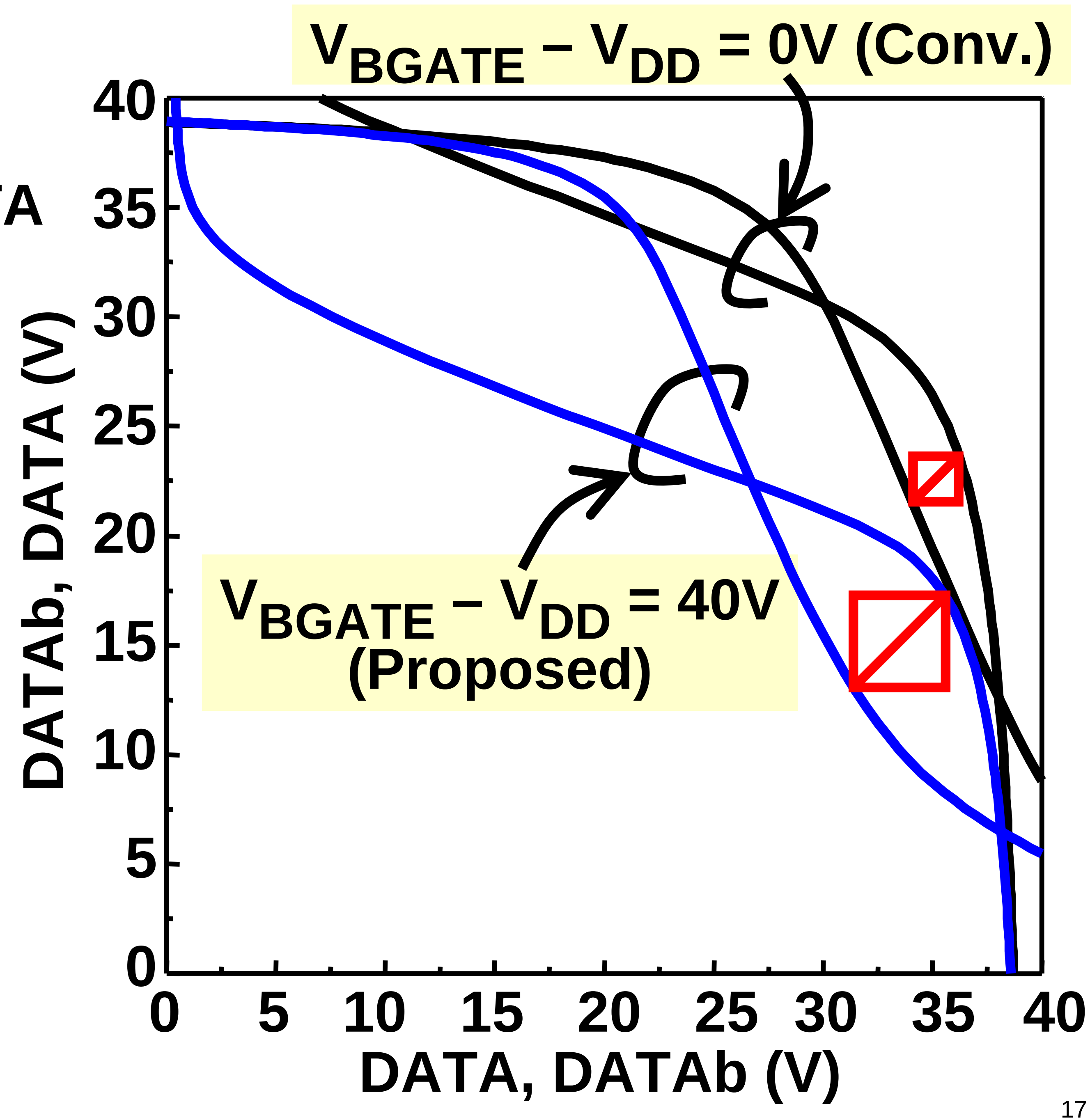


- The V_{TH} control technology using a back gate compensates for the immature V_{TH} control process technology and achieves a reliable SRAM operation.

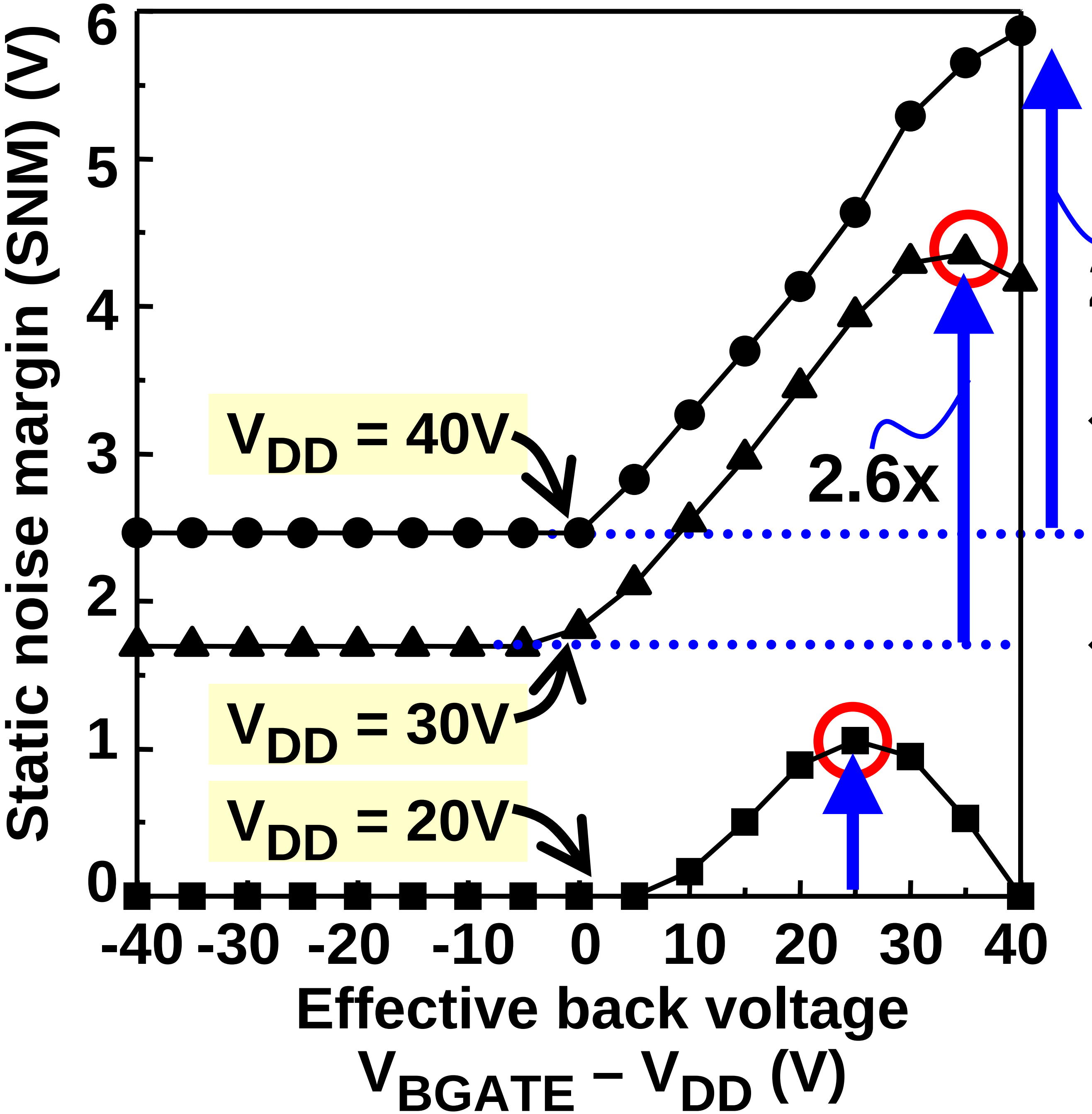
Butterfly Curves of SRAM



- Inverter gain is 2.7.
- V_{BGATE} increases the static noise margin.

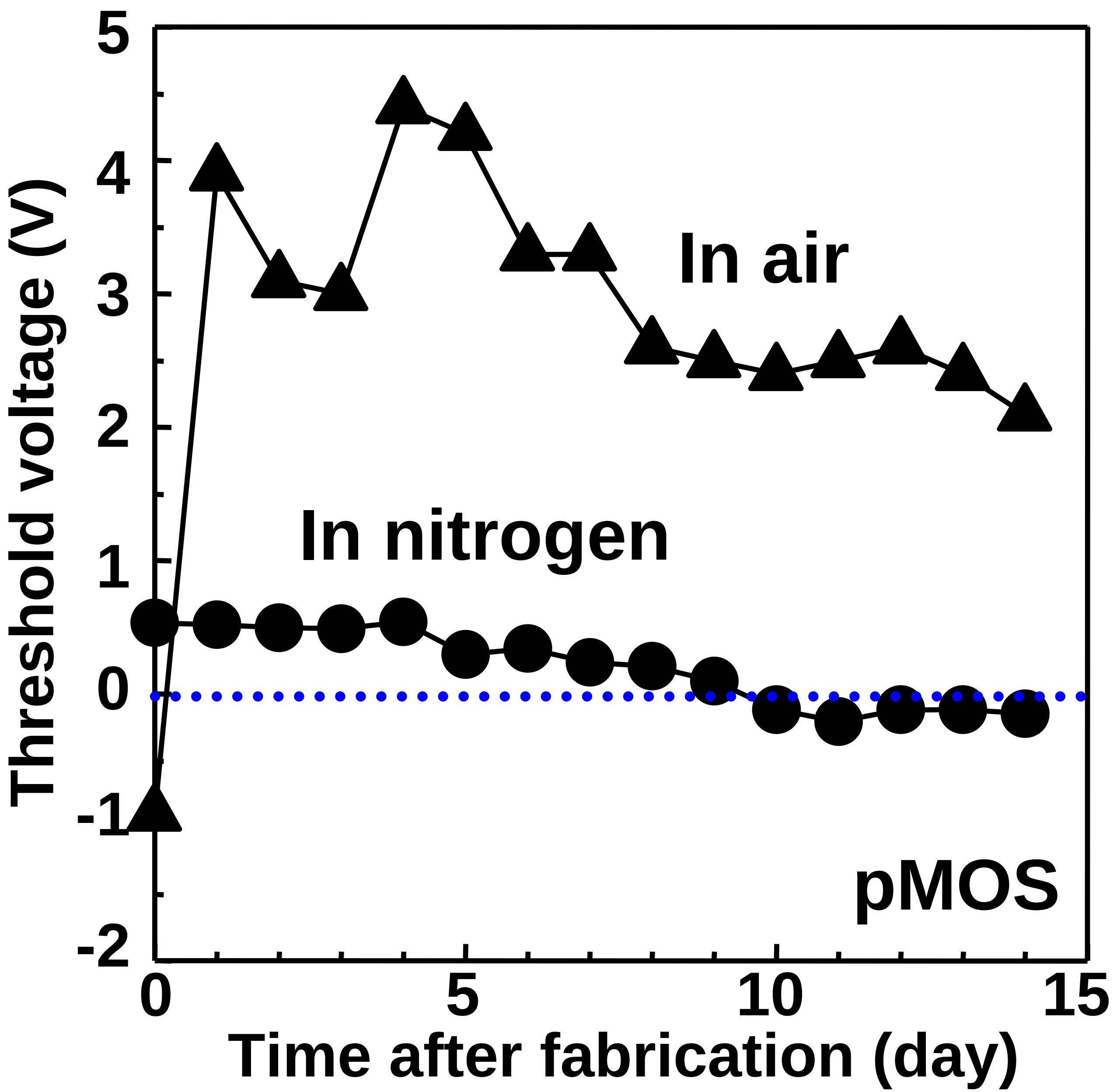


Static Noise Margin (SNM) of SRAM



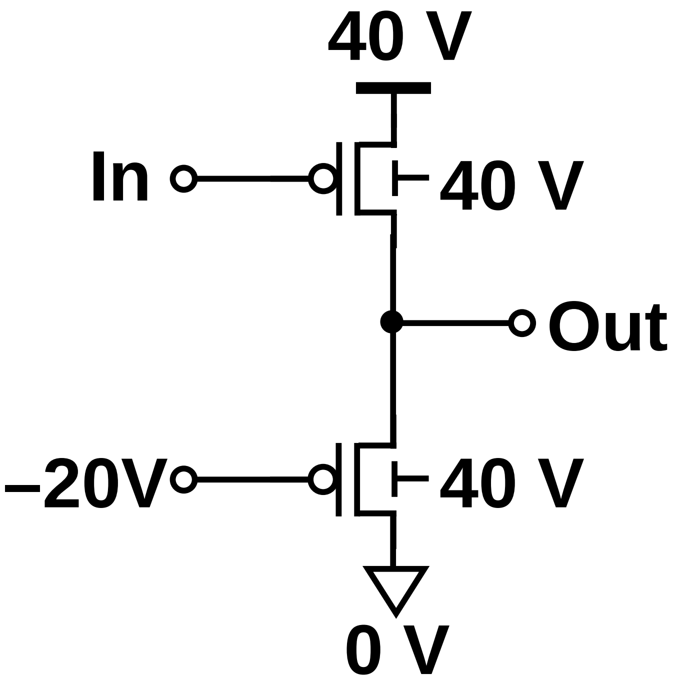
- When V_{DD} is 40V, SNM increases as V_{BGATE} increases.
- When V_{DD} is 30V and 20V, an optimum V_{BGATE} achieves the maximum SNM, because there is an optimum $|V_{TH}|$ of OFETs.

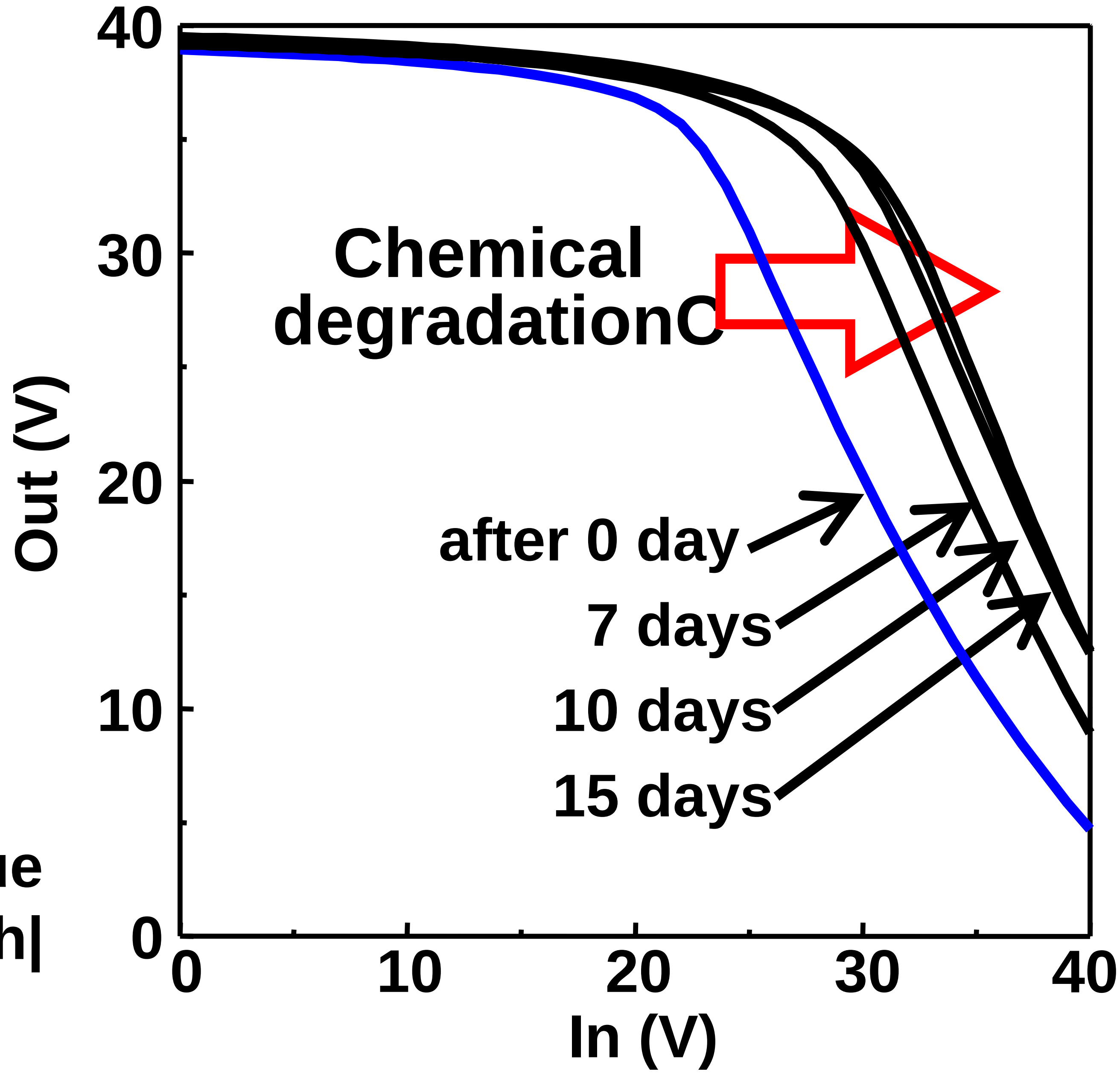
Chemical Degradation of OFETs



- OFETs are chemically degraded by the oxygen and the moisture in the atmosphere.
- The most serious problem with OFETs

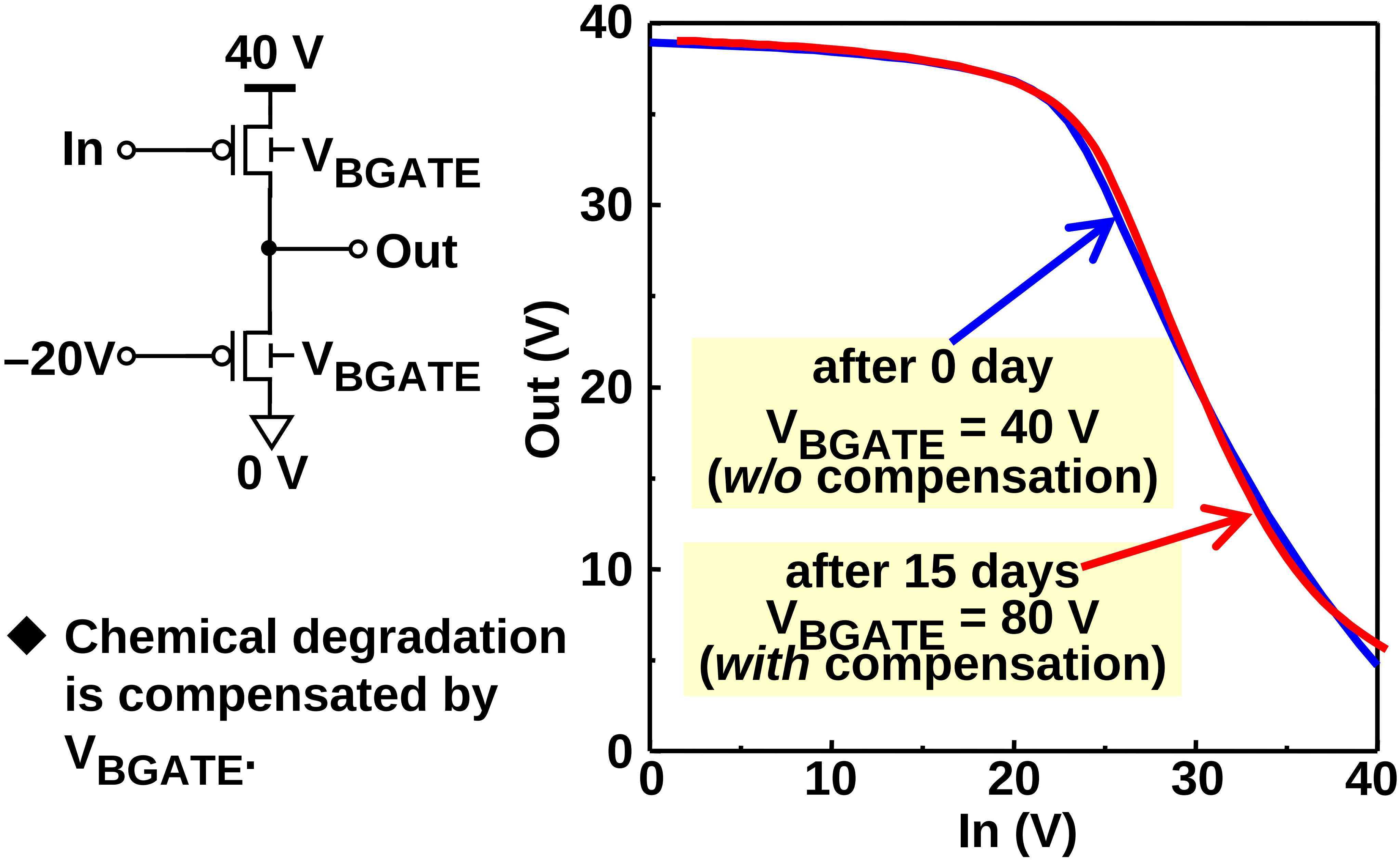
Aging of Inverter in SRAM





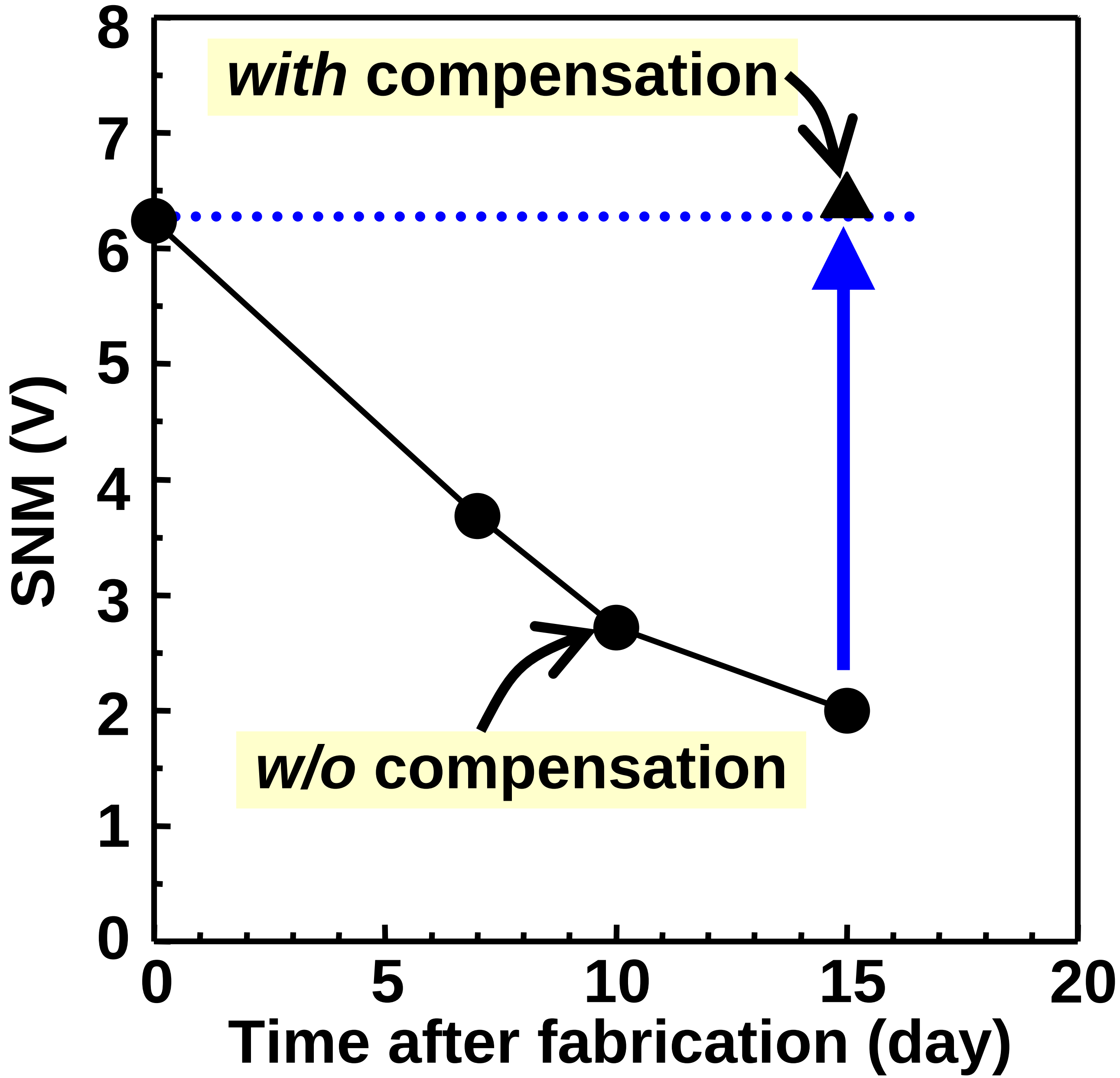
- Rightward shift due to the reduced |Vth| of OFETs

Compensation for Aging



- Chemical degradation is compensated by V_{BGATE}.

Aging of SNM and Compensation



- A constant SNM can be achieved with the back gate.
- The proposed compensation technology is essential to OFET applications.
- Manufacturing variation can also be compensated.

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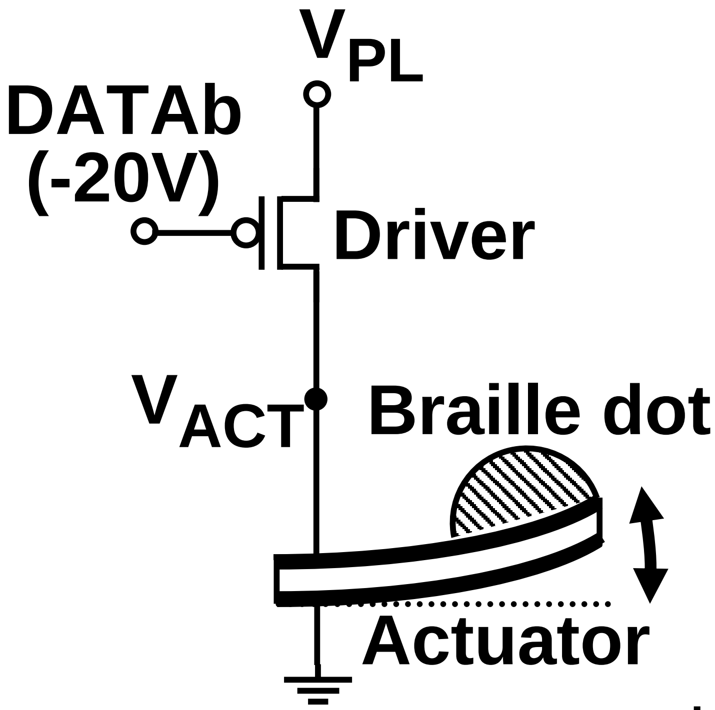
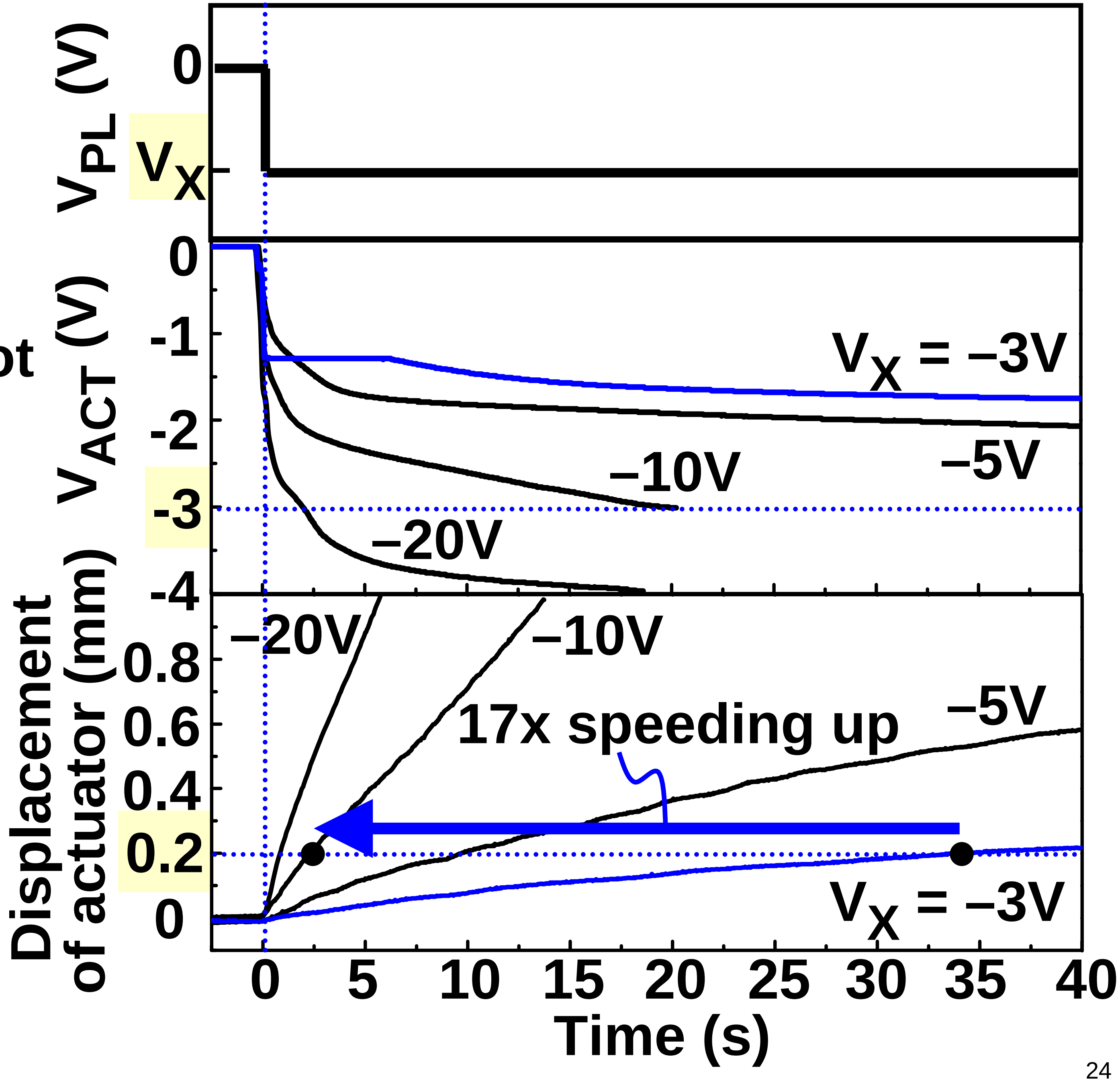
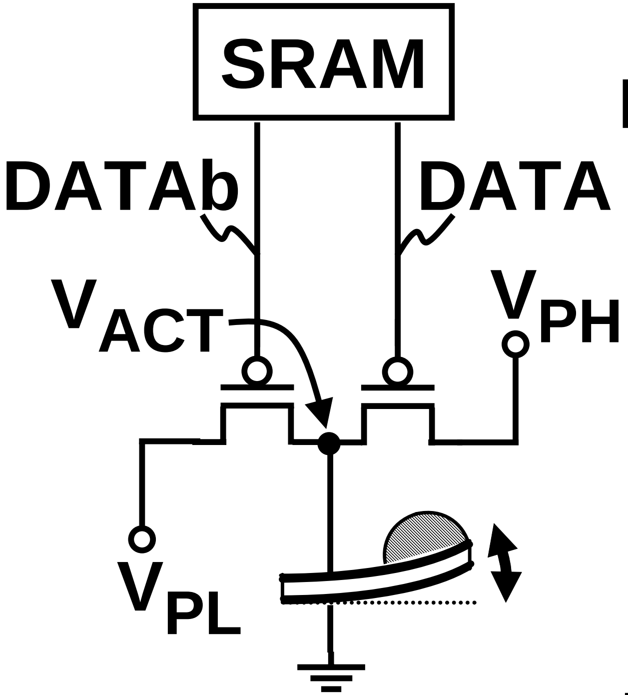
Overdrive Techniques for Driver

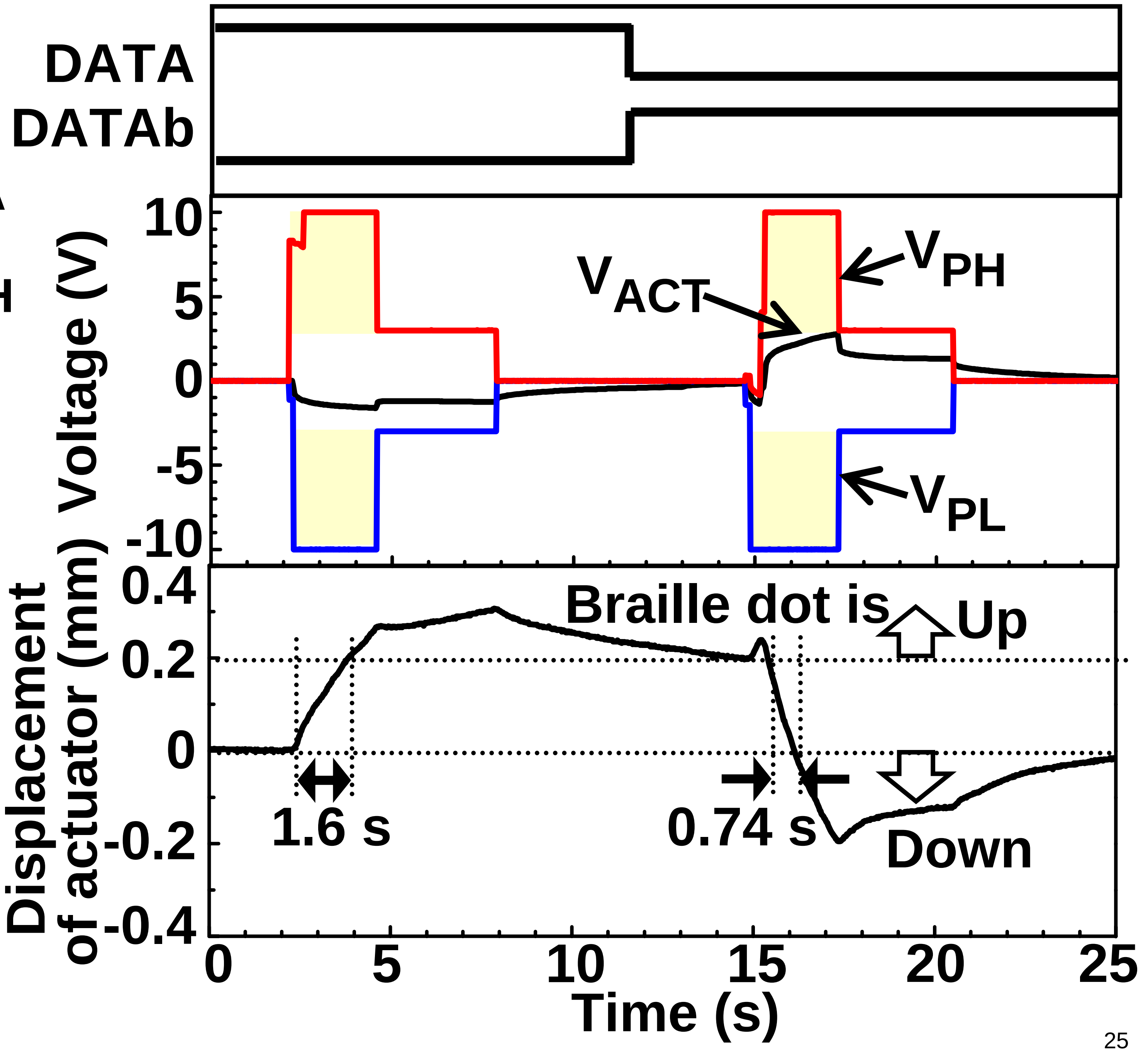




- By increasing V_X from -3 V to -10 V, the transition time is reduced from 34 s to 2.0 s, which satisfies our design target.

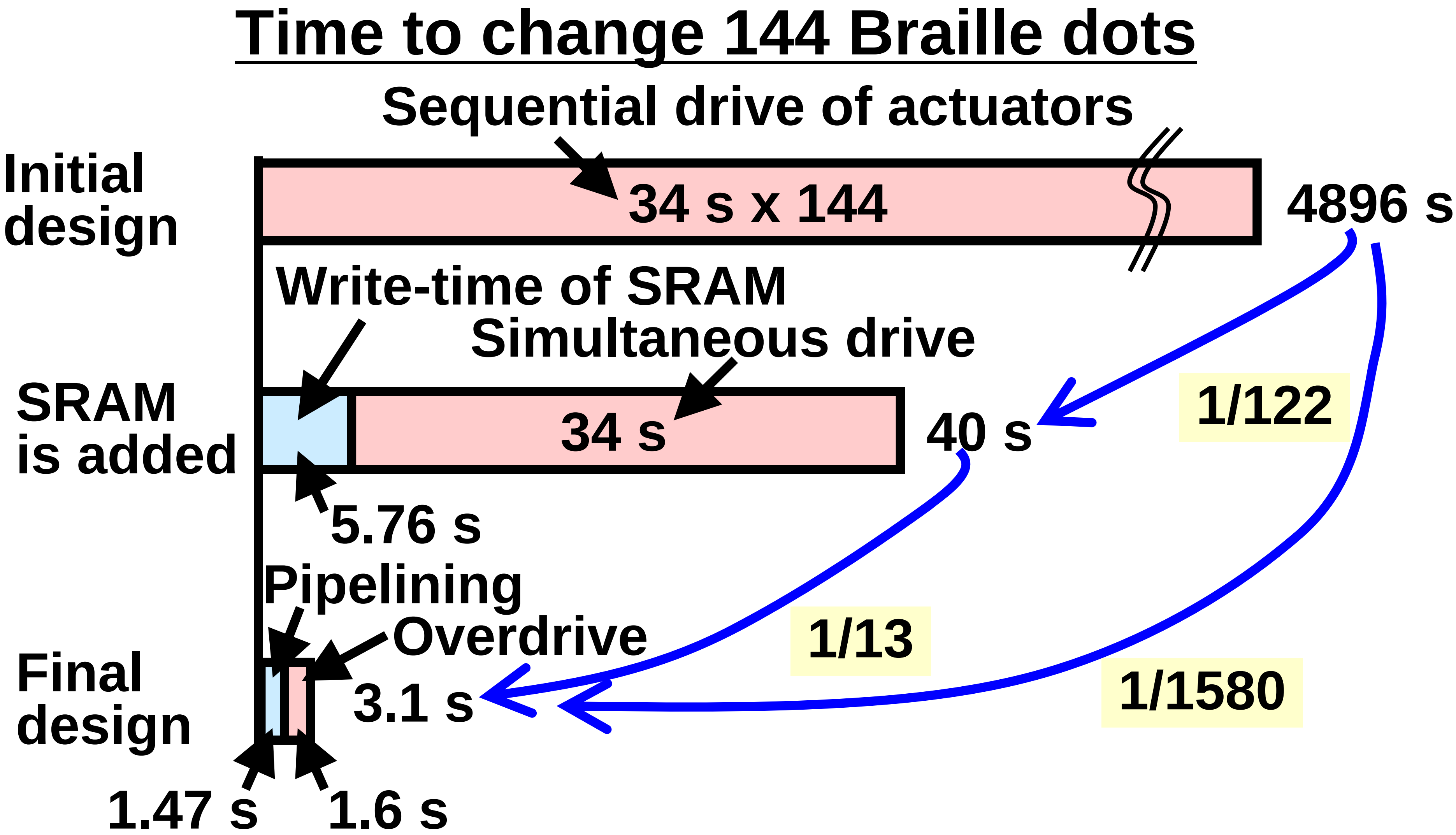
Operation of Braille Sheet Display





- By using overdriving in V_{PH} and V_{PL}, 1.6 s actuator transition time is achieved.

Summary of Speeding Up Braille Sheet Display



- **Developed circuit technologies increased the speed of the Braille sheet display 1580 times, and achieved the practical 3.1-ns operation.**

Summary

- OFETs were integrated with actuators, and a Braille sheet display was demonstrated.
- Pipelining the write-operation reduced the SRAM write-time by 74%.
- Threshold voltage control technology using a back gate increased the SNM of SRAM from 2.5 V to 5.9 V and successfully compensated for the chemical degradation of the OFETs after 15 days.
- The overdrive techniques for the driver OFETs reduced the transition time of the actuator from 34 s to 2 s.
- These developed circuit technologies will be essential for the future large area electronics made with OFETs.