Outline

- Background of low-power app's
- Concept of SCCMOS
- Comparison with other schemes
- Measured results
- Summary
Background of low-voltage applications

- Strong low-power requirement
- Power $\propto V_{DD}^2$
  - $\rightarrow$ Low $V_{DD}$ (0.5 - 0.8V)
  - $\rightarrow$ Low $V_{TH}$ (0.1 - 0.2V)
- 10mA-order leakage (1M-gate)
- Problem for mobile applications
Concept of SCCMOS

- **St'by:** $V_{DD} + 0.4V$
- **Active:** $V_{SS}$

$V_{DD}$ (0.5 - 0.8V)

Low-$V_{TH}$ cut-off MOSFET

Virtual $V_{DD}$

Low-$V_{TH}$
logic
circuit

pMOS insertion

Virtual $V_{SS}$

• **Active:** $V_{DD}$
• **St'by:** $V_{SS} - 0.4V$

nMOS insertion
Gate bias generator

St'by: $V_{DD} + 0.4V$
Active: $V_{SS}$

$V_{DD}$ (0.5 - 0.8V)

Low-$V_{TH}$ cut-off MOSFET

Virtual $V_{DD}$
Oxide reliability

Original

Virtual V_{DD} (0.8V)

1.2V

1.2V

Virtual V_{DD} (in standby) = V_{SS}

Higher reliability

V_{DD} (0.8V)

1.2V

0.8V

0.4V

Virtual V_{DD} (in standby) = V_{SS}

© IEEE 1998

12.4-5
MTCMOS vs. SCCMOS

- High-$V_{TH}$ MOSFET doesn't turn on at low $V_{DD}$.

MTCMOS

- Standby: $V_{DD}$
- Active: 0V
- $V_{DD}$ (0.6V)

SCCMOS

- Standby: $V_{DD} + 0.4V$
- Active: 0V
- $V_{DD}$ (0.5V)
VTCMOS vs. SCCMOS

- VTCMOS is not suitable for SOI technology.

**VTCMOS**

- St'by: $V_{DD}+1V$
- Active: $V_{DD}$
- Active: $V_{SS}$
- St'by: $V_{SS}-1V$

**SCCMOS**

- St'by: $V_{DD}+0.4V$
- Active: 0V

- $V_{DD}$ (0.8V)

- Low-$V_{TH}$

- Virtual $V_{DD}$

- $V_{TH}$ varies with body bias effect.
Applicability to DTMOS

- DTMOS suffers 10mA-order leakage (1M-gate).
- SCCMOS can cut off leakage when used with DTMOS.

**DTMOS**

St'by: \( V_{DD} + 0.4V \)  
Active: 0V

Low-\( V_{TH} \)

Virtual \( V_{DD} \)

- Inherent forward pn-junction
- \( V_{DD} \) is limited to 0.7V.
Chip microphotograph

- 0.3\(\mu\)m, triple-metal CMOS process
- \(V_{TH}=0.2V\)

- 100x100\(\mu\)m\(^2\)
- Pumping freq=10kHz
- 0.1\(\mu\)A (\(V_{DD}=0.5V\))
Delay characteristics (inverter & NAND)

- MOSFET gate widths are 2.4 μm.
- Fanout-3

Inverter

NAND

- SCCMOS
  0.2V circuit
  with 0.2V $V_{TH}$
  cut-off MOSFET

- MTCMOS
  0.2V circuit
  with 0.6V $V_{TH}$
  cut-off MOSFET

- Conventional
  All 0.6V circuit

- No cut-off MOSFET
  All 0.2V circuit
Losing information in standby

- **System level solution:** → Using scan-path flip-flops

- **Circuit level solution:**

```
+----------------+     +----------------+
|                |     |                |
|    CK-         |     | Current latch  |
|                |     | flip-flop      |
|    D-          |     | D              |
|                |     | CK             |
+----------------+     +----------------+

High-V_{TH} SRAM Cell
```

- N1
- N2
- Q
- $\overline{Q}$
- WL
- 0.5V
- -0.5V
Waveforms of special flip-flop

![Waveforms Diagram](image-url)

© IEEE 1998
Method to measure flip-flop delay

Current latch flip-flop

Edge-Trigger Pulse Generator (ETPG)

101 Stages

\[ t_{pd}(F/F + ETPG) \]

101 Stages

\[ t_{pd}(ETPG) \]

\[ t_{pd}(F/F) \]
Delay characteristics (flip-flop)

- Measurement
- SCCMOS
- MTCMOS
- Conv.
- No cut-off MOSFET

$t_{pd}$ [ns] vs. $V_{DD}$ [V]
Pass-transistor gate-array
Delay characteristics (pass-tr. logic)
Summary

- SCCMOS can operate down to 0.5V.
- SCCMOS can suppress leakage below 1pA per gate without speed degradation.
- Effective with SOI technology and/or pass-transistor logic.