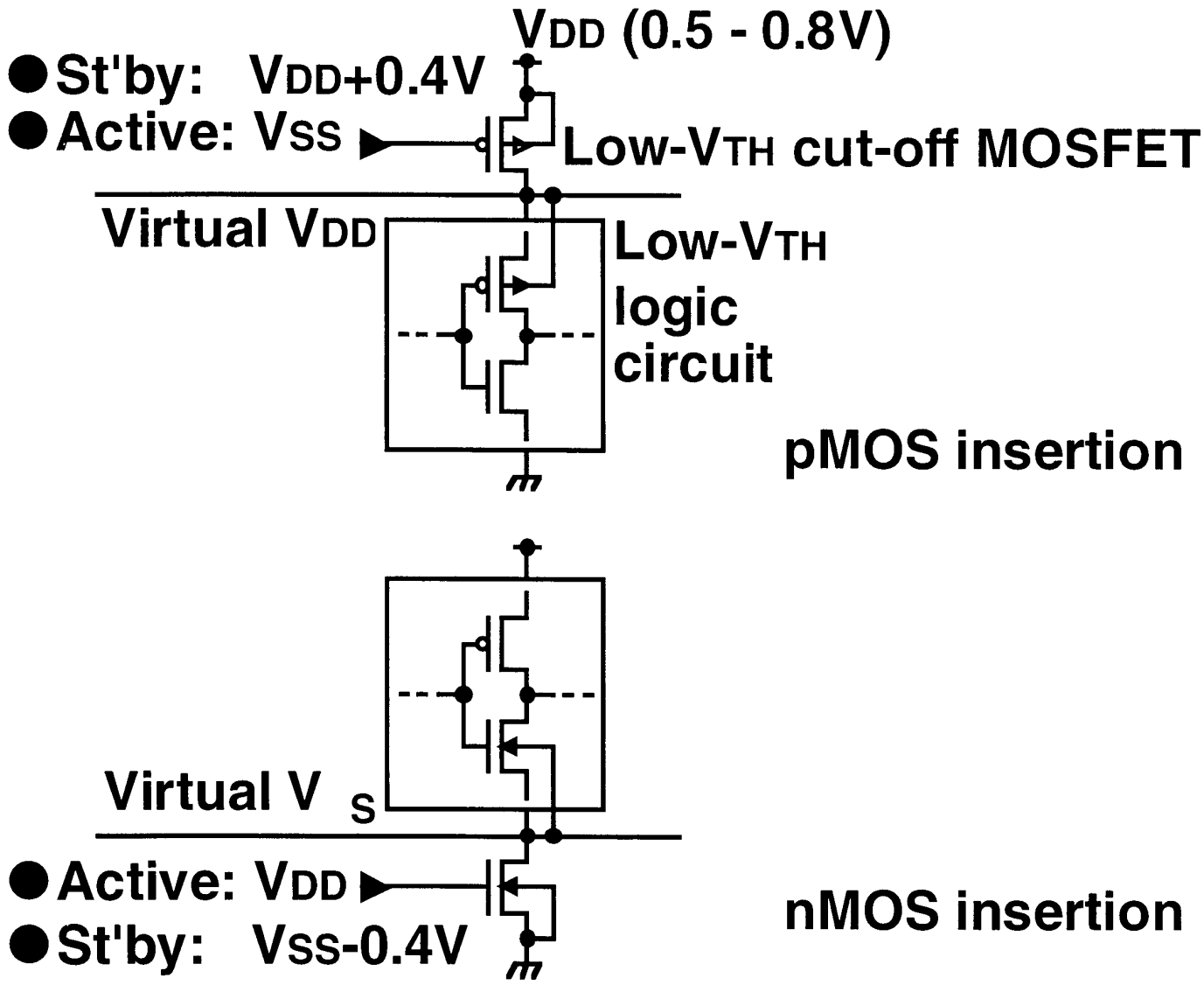
Outline

- Background of low-power app's
- Concept of SCCMOS
- Comparison with other schemes
- Measured results
- Summary

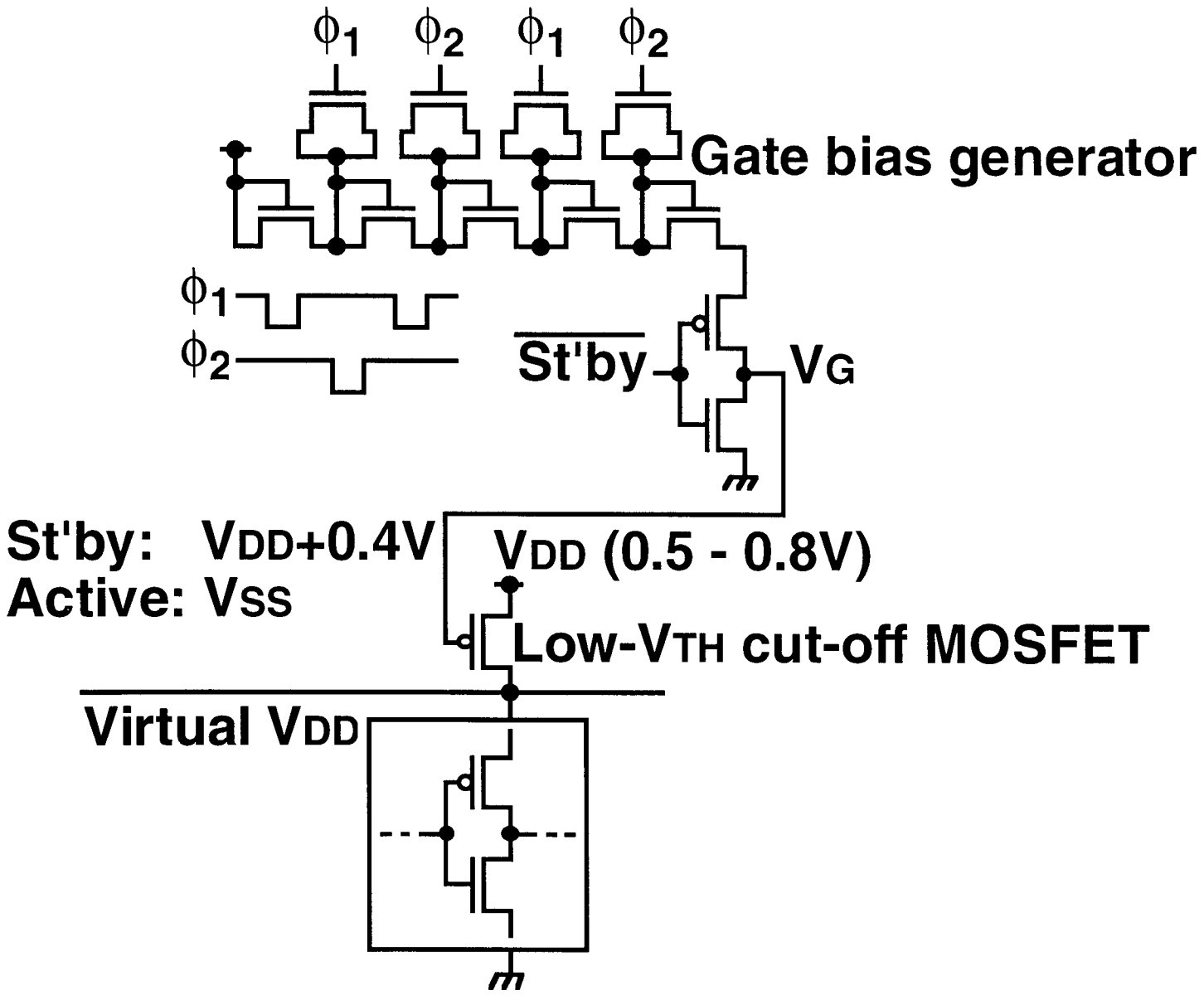
Background of low-voltage applications

- Strong low-power requirement
- Power $\propto V_{DD}^2$
  - $\rightarrow$ Low V_{DD} (0.5 - 0.8V)
  - $\rightarrow$ Low V_{TH} (0.1 - 0.2V)
- 10mA-order leakage (1M-gate)
- Problem for mobile applications

Concept of SCCMOS

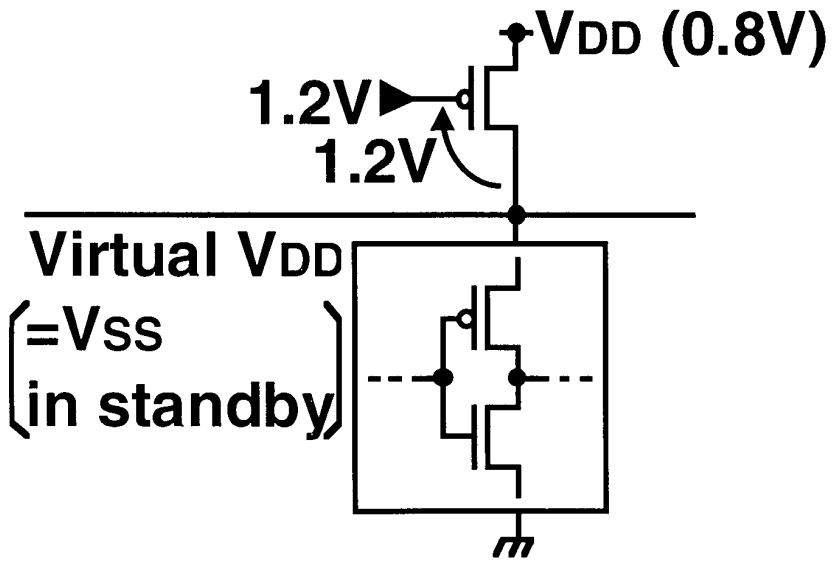


Gate bias generator

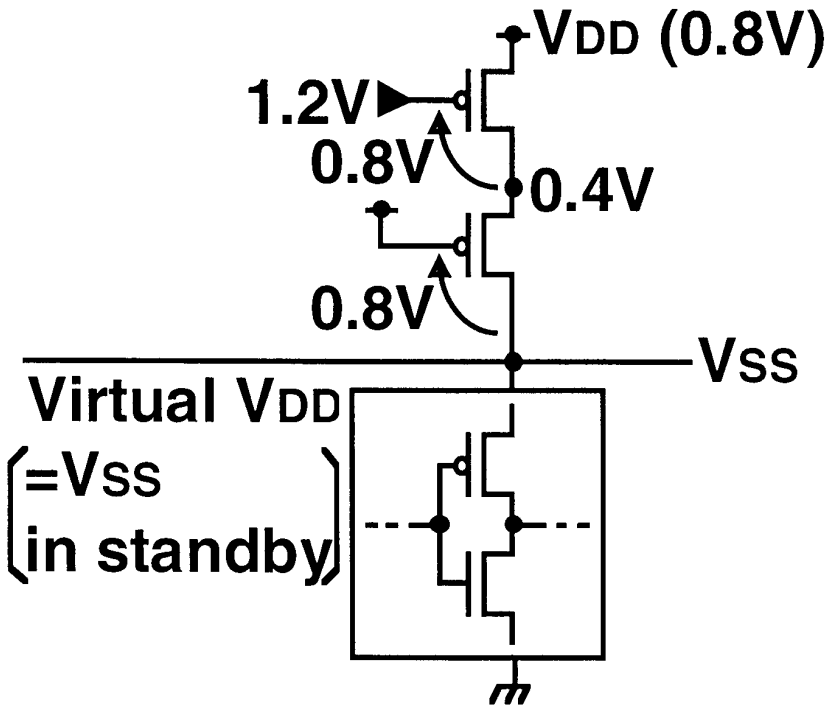


Oxide reliability

Original



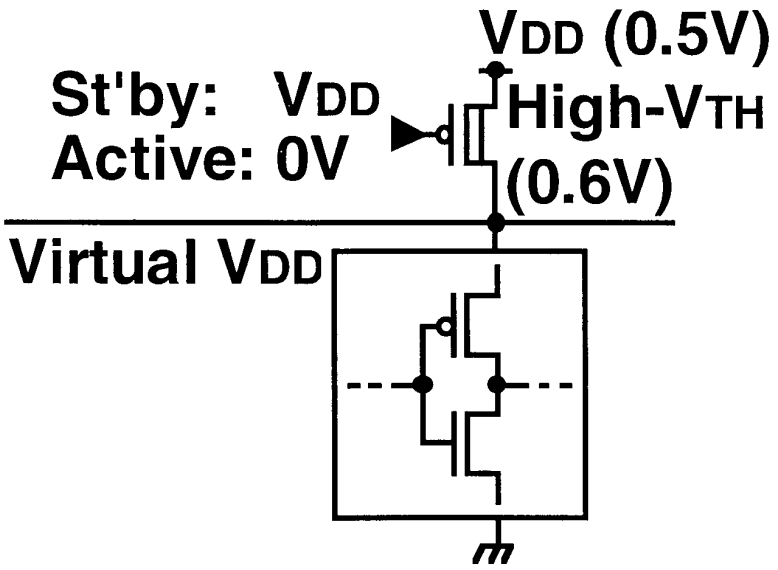
Higher reliability



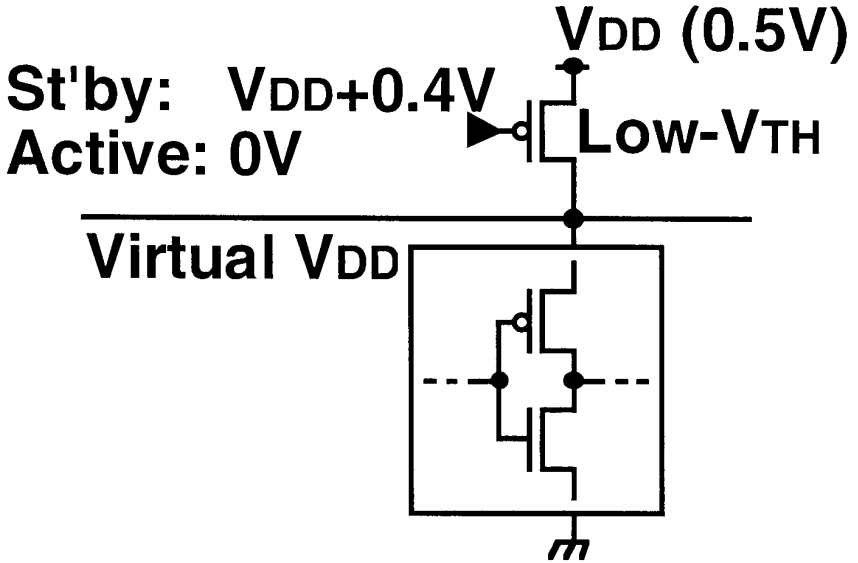
MTCMOS vs. SCCMOS

- High-V_{TH} MOSFET doesn't turn on at low V_{DD}.

MTCMOS



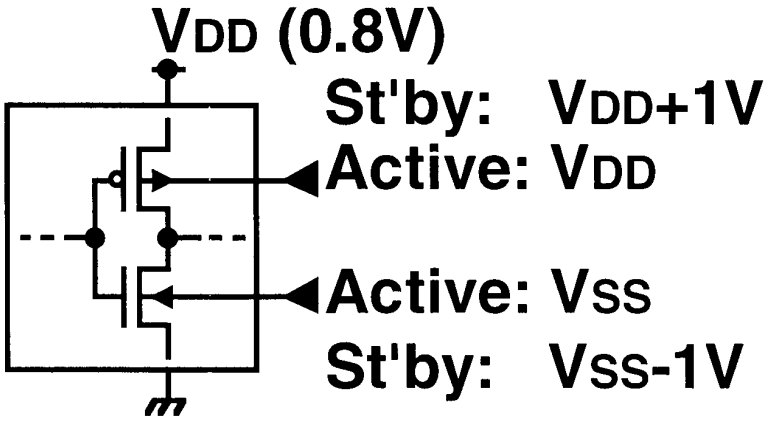
SCCMOS



VTCMOS vs. SCCMOS

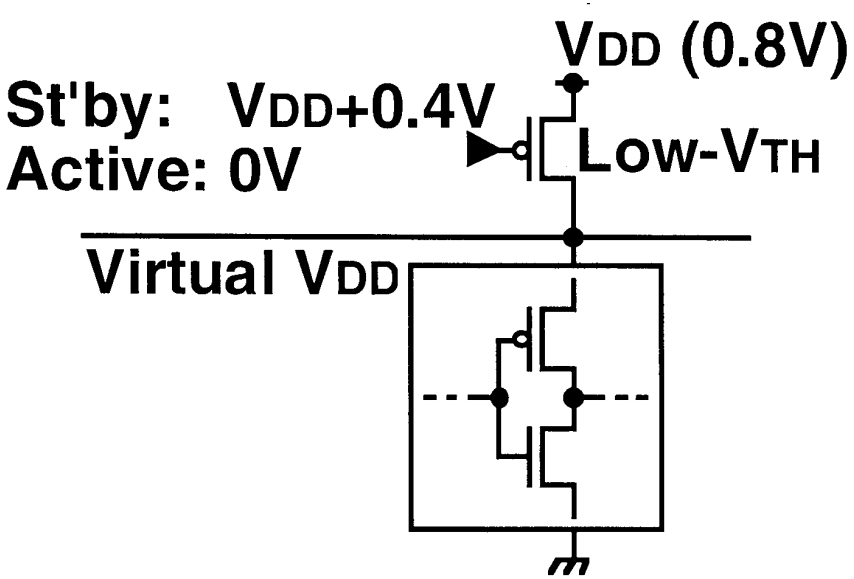
- VTCMOS is not suitable for SOI technology.

VTCMOS



- VTH varies with body bias effect.

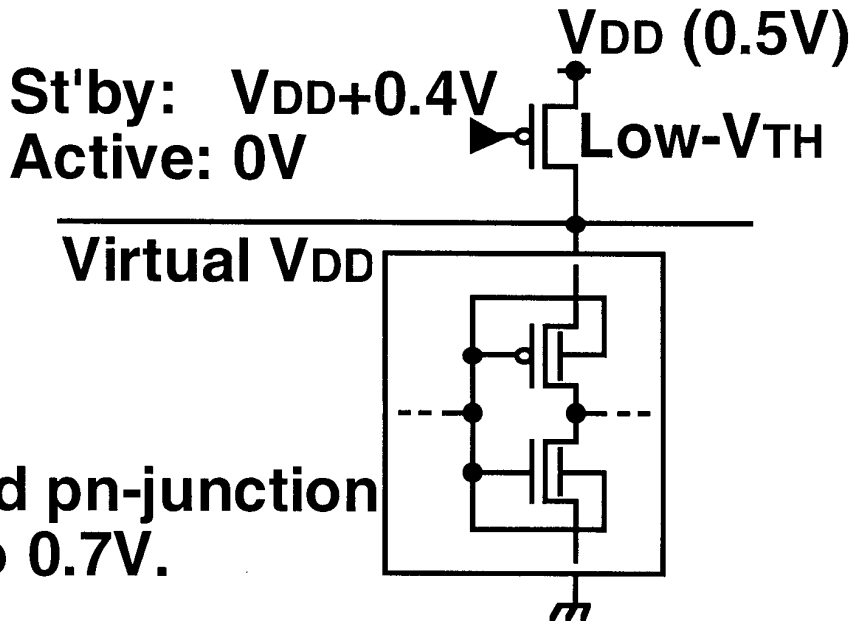
SCCMOS



Applicability to DTMOS

- DTMOS suffers 10mA-order leakage (1M-gate).
- SCCMOS can cut off leakage when used with DTMOS.

DTMOS

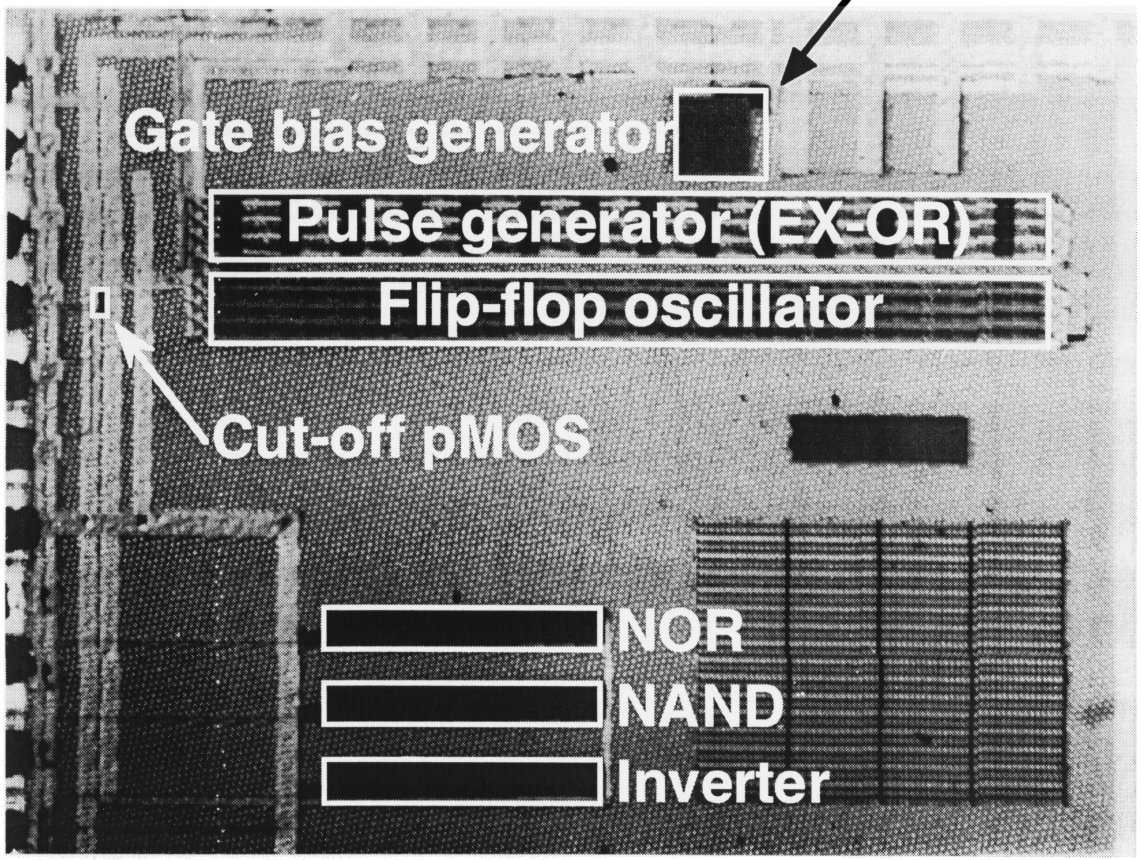


- Inherent forward pn-junction
- VDD is limited to 0.7V.

Chip microphotograph

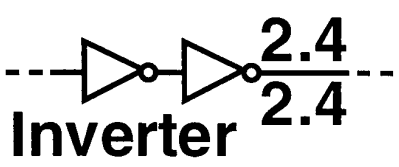
- 0.3μm, triple-metal CMOS process
- V_{TH}=0.2V

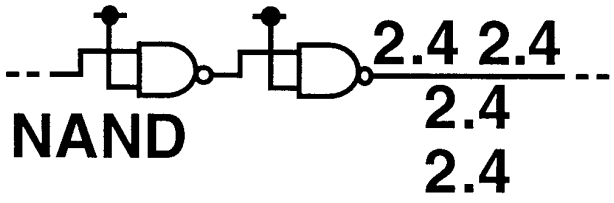
100x100μm²
pumping freq=10kHz
0.1μA (@V_{DD}=0.5V)

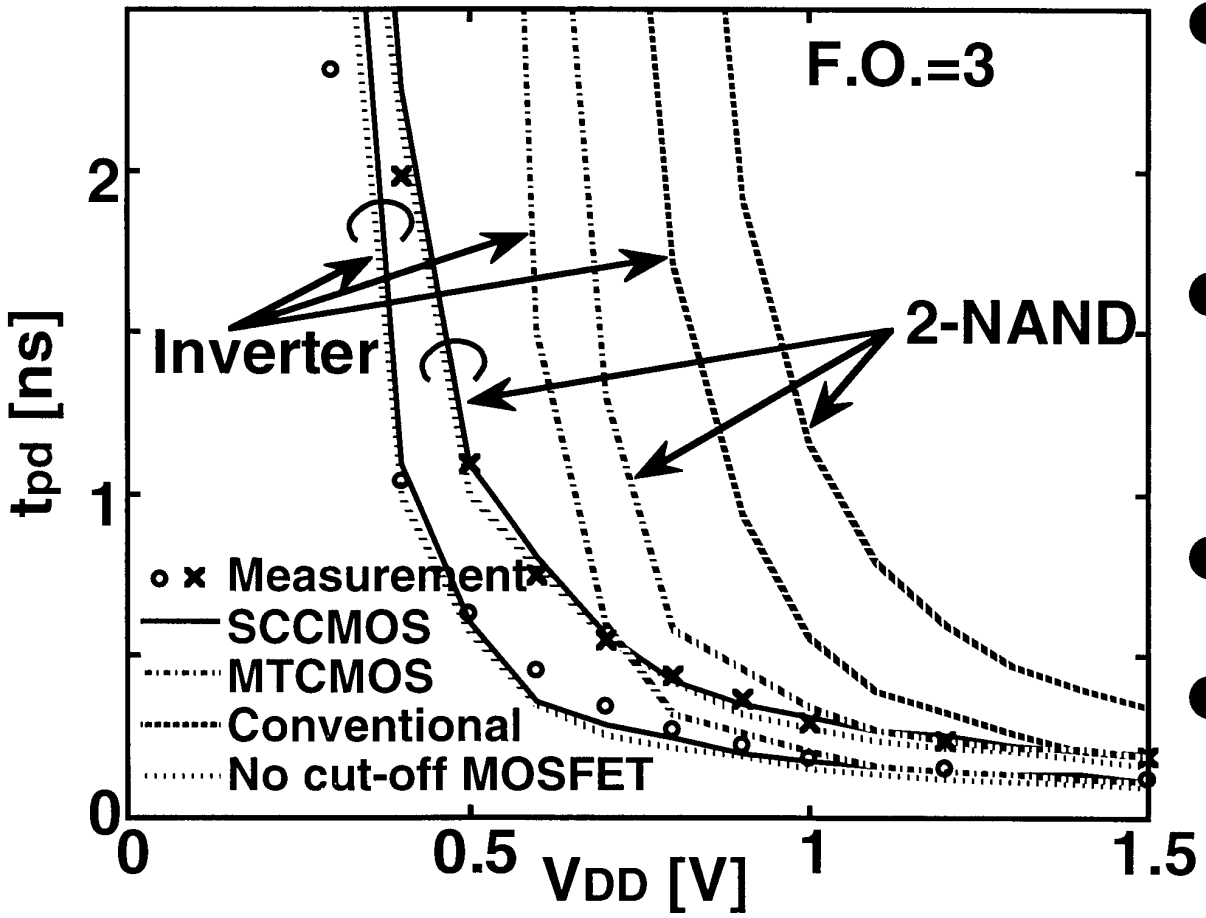


Delay characteristics (inverter & NAND)

- MOSFET gate widths are 2.4μm.
- Fanout-3



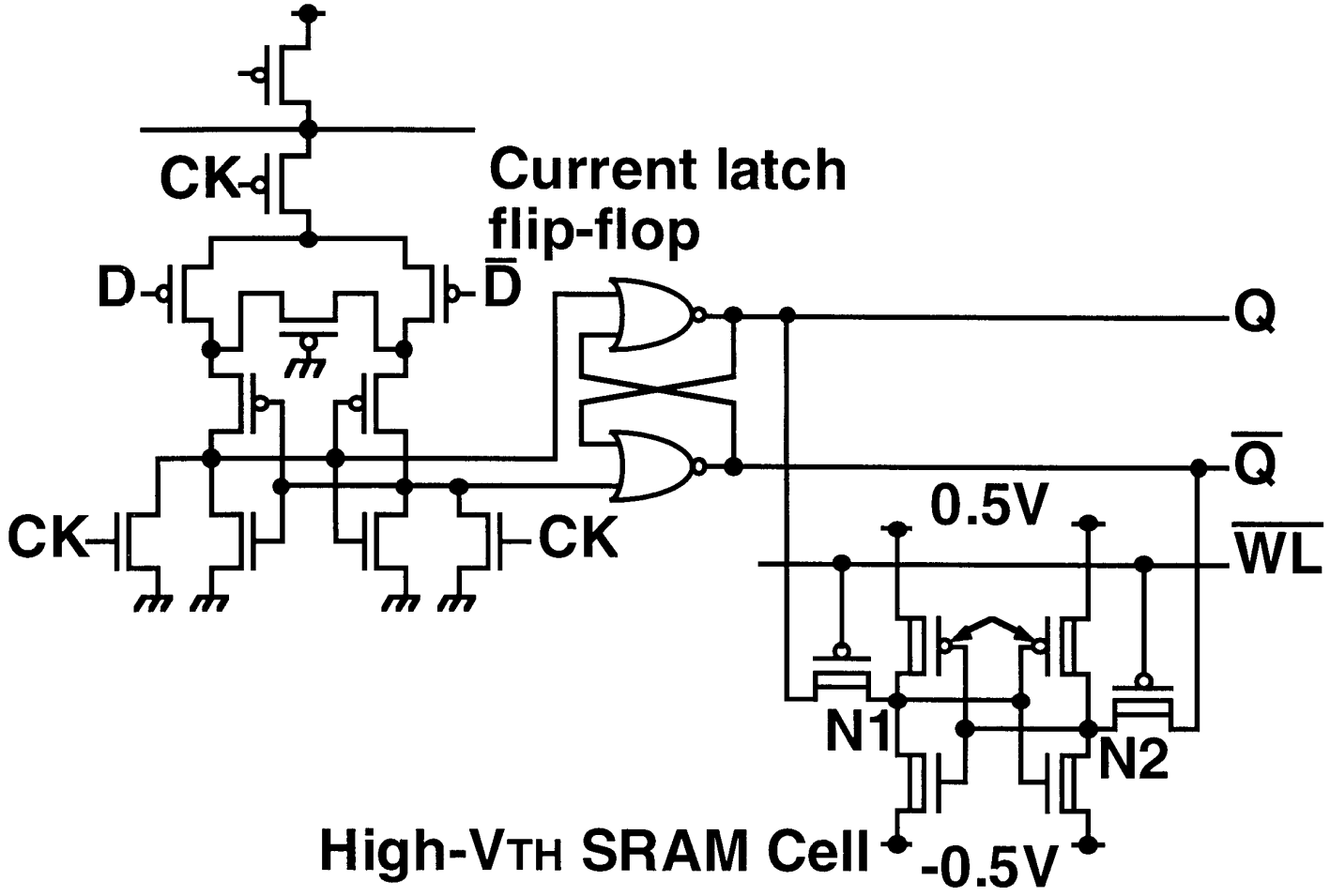




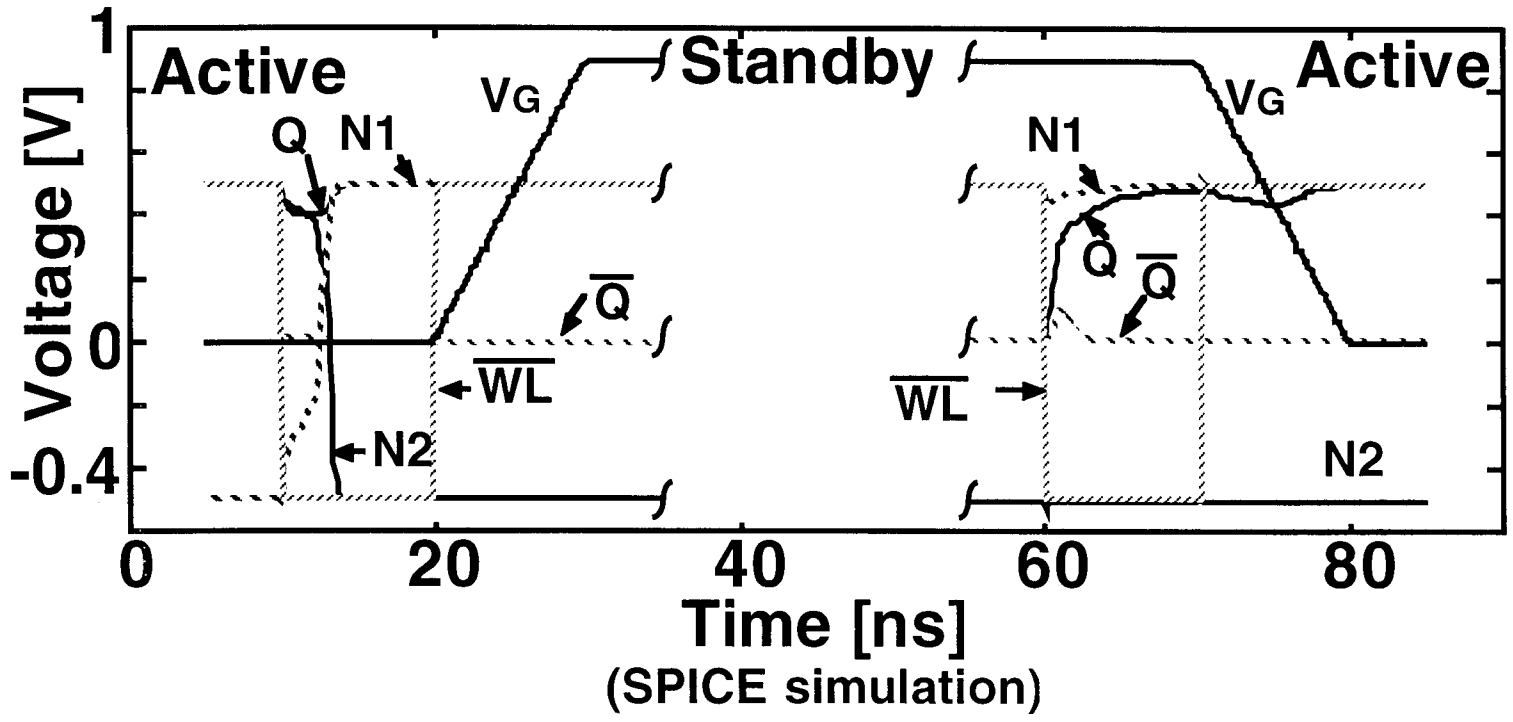
- SCCMOS
  0.2V circuit
  with 0.2V V_{TH}
  cut-off MOSFET
- MTCMOS
  0.2V circuit
  with 0.6V V_{TH}
  cut-off MOSFET
- Conventional
  All 0.6V circuit
- No cut-off MOSFET
  All 0.2V circuit

Losing information in standby

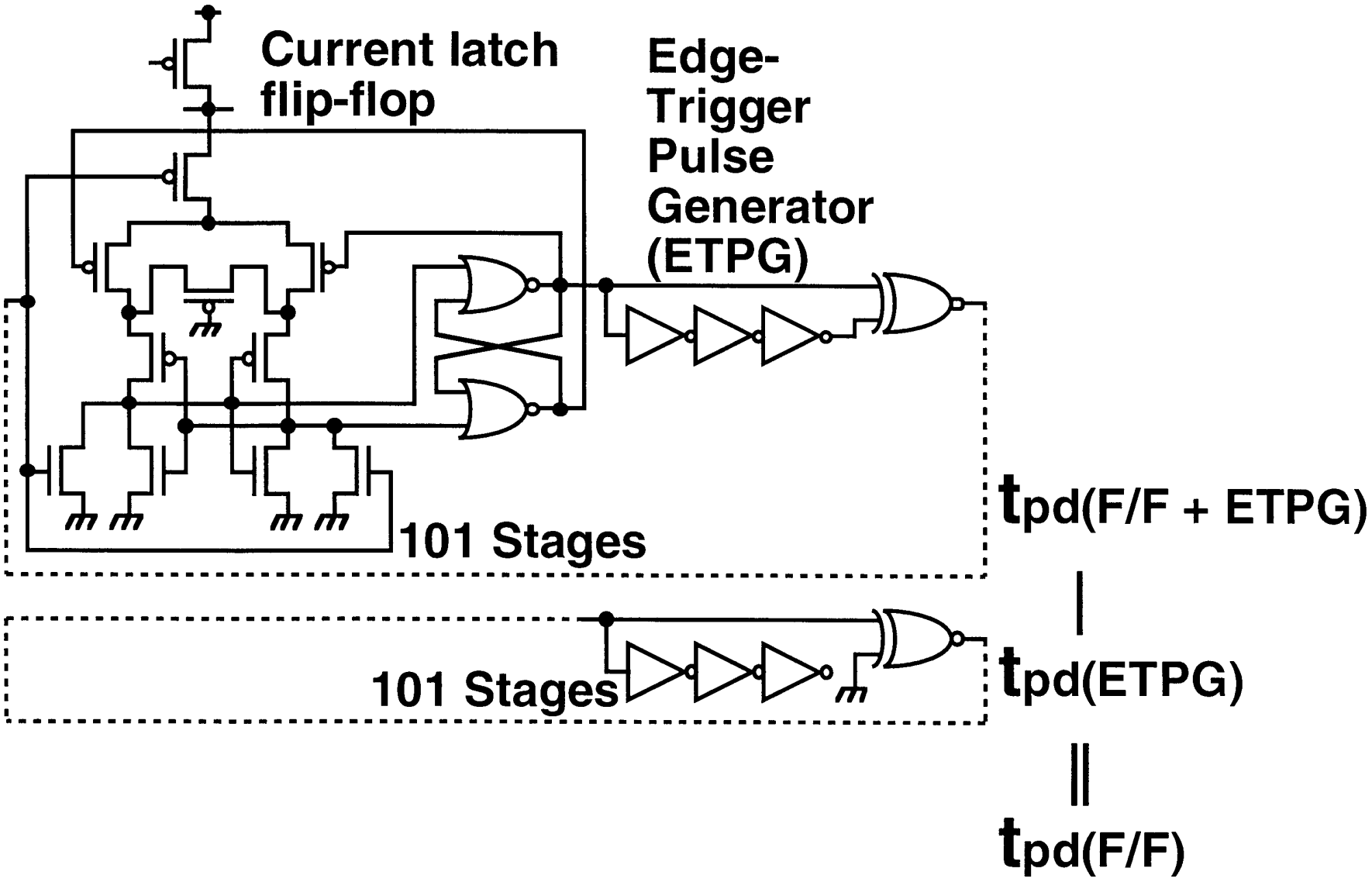
- System level solution: → Using scan-path flip-flops
- Circuit level solution:



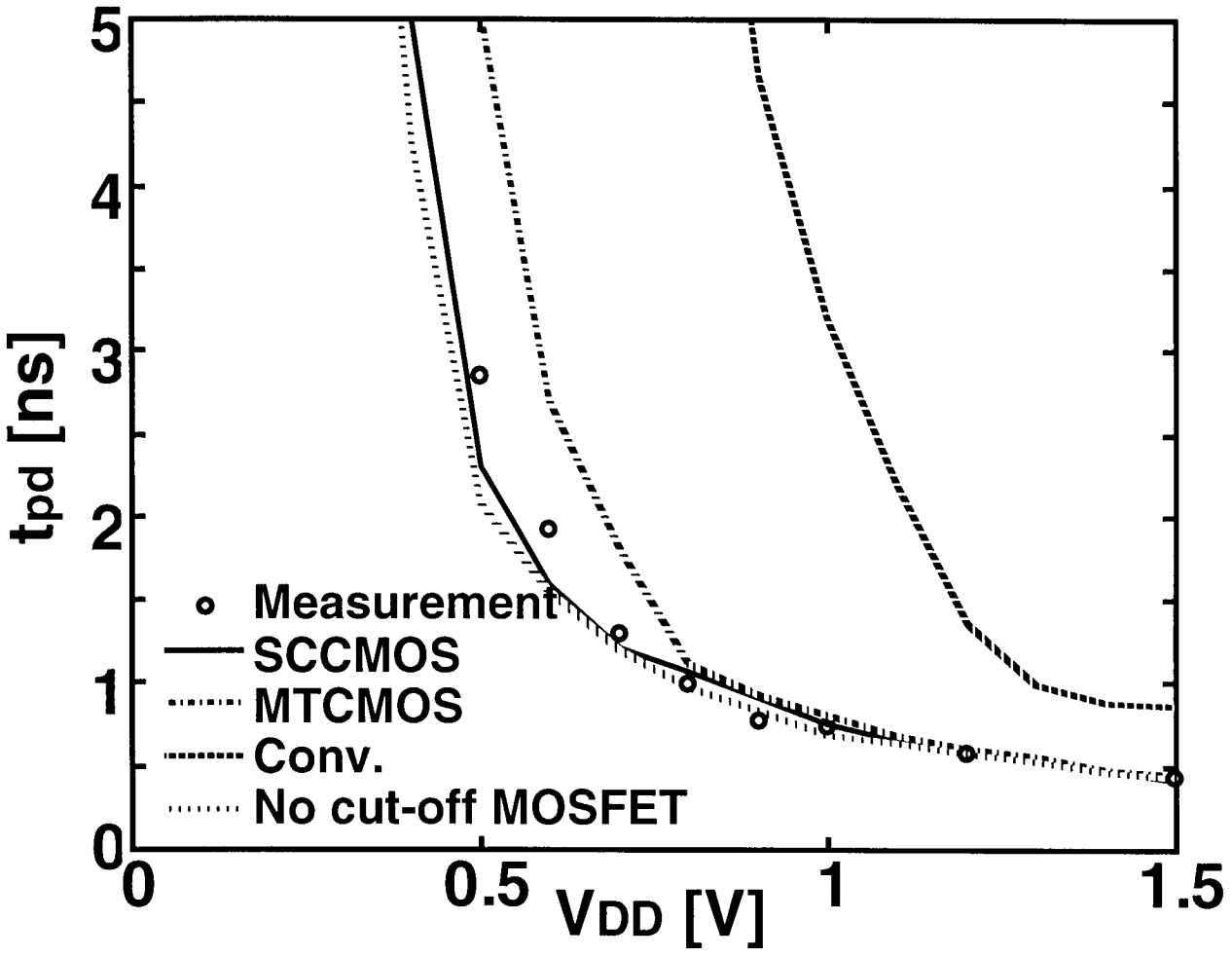
Waveforms of special flip-flop



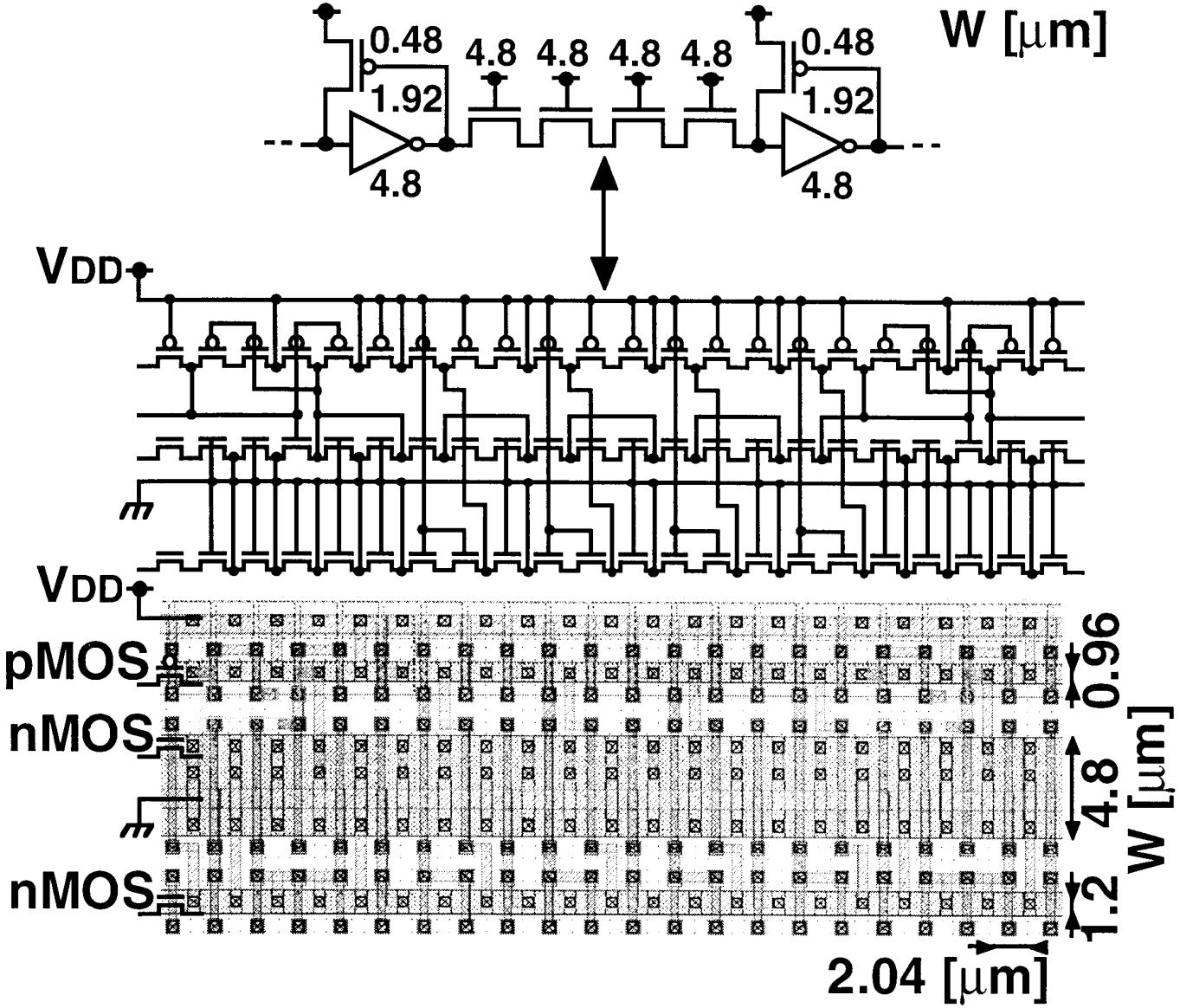
Method to measure flip-flop delay



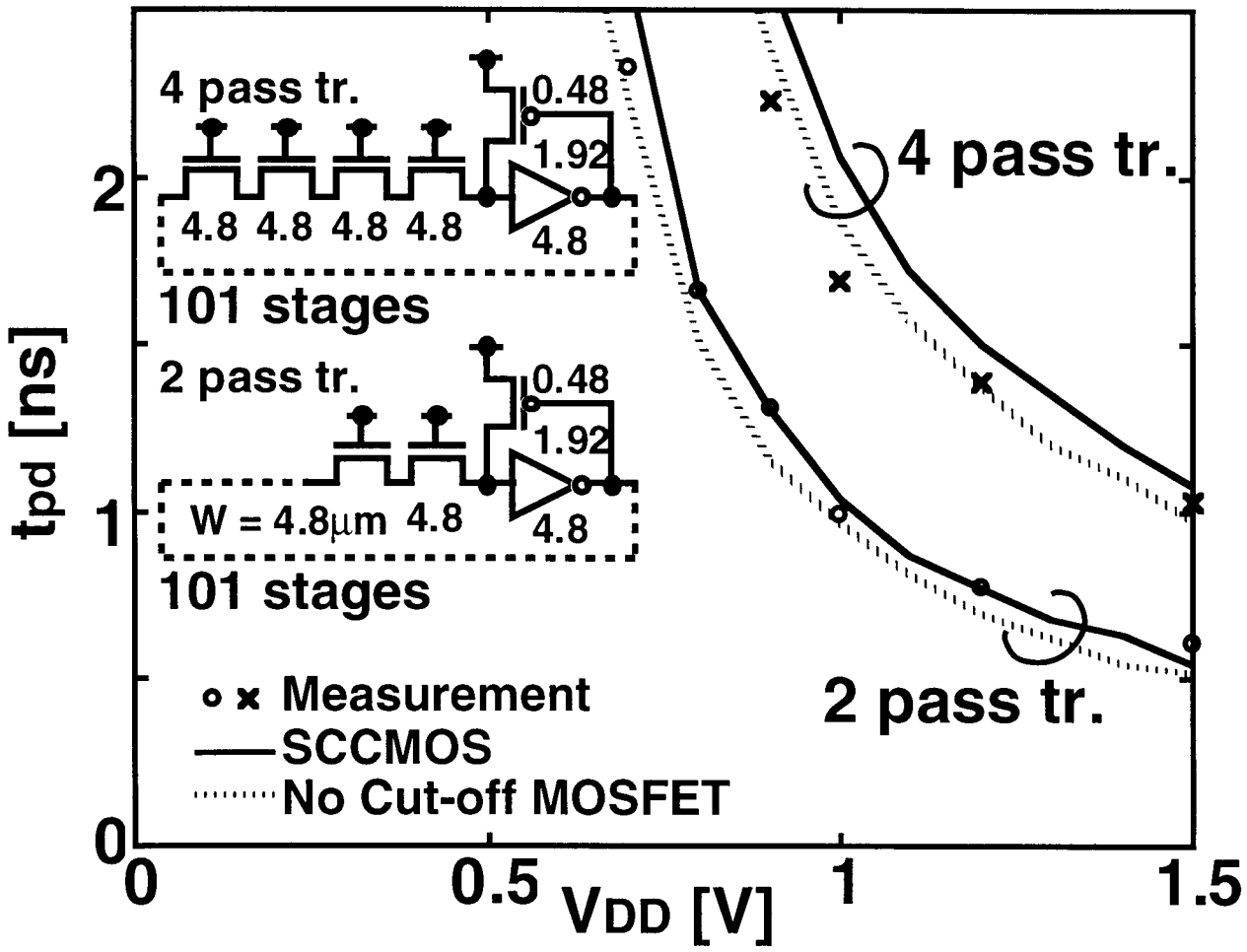
Delay characteristics (flip-flop)



Pass-transistor gate-array



Delay characteristics (pass-tr. logic)



Summary

- SCCMOS can operate down to 0.5V.
- SCCMOS can suppress leakage below 1pA per gate without speed degradation.
- Effective with SOI technology and/or pass-transistor logic.