A 60-dB Image Rejection Filter Using Δ-Σ Modulation and Frequency Shifting

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Abstract

We propose a novel image rejection scheme for a low-IF (low intermediate frequency) receiver. A Δ-Σ modulator converts I/Q signals to digital values, and then they are digitally processed. The Δ-Σ modulator is a second-order complex band-pass type; the proposed architecture is suitable for various multi-channel communications and/or cognitive radio. As the first step in the digital signal processing, a spectrum is shifted so that the desired signal band is centered at 0 Hz. Next, by LPFs (low-pass filters), an image signal and the quantization noise of the Δ-Σ modulator are removed. These LPFs also function as a decimation filter; thus a dedicated decimation filter is not needed, and an extra area and power for it are saved. The test chip occupies 0.75 mm2 in a 180-nm mixed-signal process. The power is 6.0 mW at 1.8 V. The IRR (image rejection ratio) achieves 60 dB.

1. Introduction

Low-IF (low intermediate frequency) receiver architecture has advantages in chip implementation.

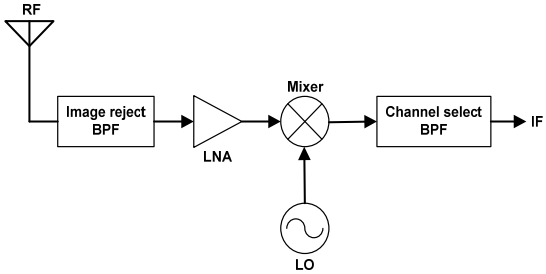

Figure 1. Block diagram of low-IF receiver.

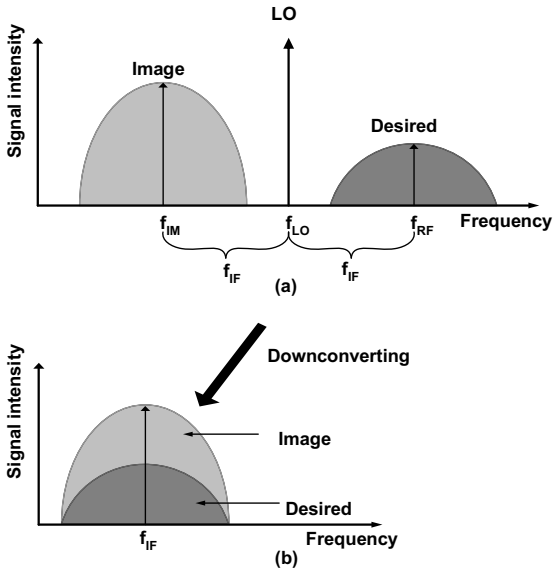

Figure 2. Image problem: Spectrums (a) before and (b) after downconverting.

Fig. 1 shows a block diagram of a low-IF receiver. Circuits can be integrated in a small area by using the widely-used super-heterodyne system. In addition, the low-IF architecture is resilient against parasitic effects such as DC offset voltages and self-mixing products [1]. It has, however, an "image problem" [2].

2. Image Problem

Fig. 2 illustrates the image problem. If there is an image frequency, it is folded over the desired

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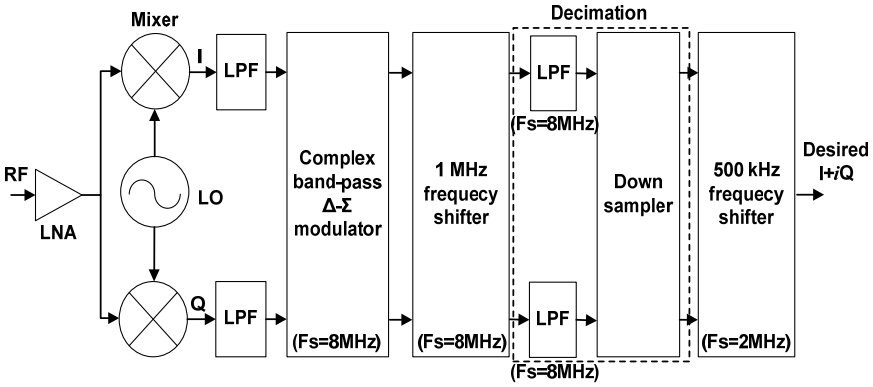

Figure 3. Proposed architecture.

frequency after mixing because $f_{RF} - f_{LO} = f_{LO} - f_{IM}$. Once they are overlapped, they cannot be distinguished.

The image problem incurs communication errors, in particular, when the image signal is stronger than the desired one. Generally, image signals may exist in any channels, which possibly interfere with the desired frequency. In low-IF receiver architecture, an IRR (image rejection ratio) of more than 60 dB is required to assure communication [3].

So, the image signal might come from an adjacent channel; however in reality, it cannot be totally removed with analog circuits. In the traditional approach, since image rejection has been made by a BPF (band-pass filter) or image rejection mixer comprised of analog circuits, an IRR is 20-30 dB at most [4]. To achieve a larger IRR, the image rejection BPF must have a steeper characteristic, but it is only realized with an external filter like a SAW (surface acoustic wave) filter. The external device is an extra overhead and suppresses design flexibility of the receiver.

By the way, the LMS (least mean square) algorithm has been already proposed for the image rejection [3]. It reduces a leakage factor of the image signal caused by mismatches in mixing. After mixing, the image and desired signals are converted into a digital domain. The image signal leaks and remains in the desire signal due to the mismatch; as well, the desired signal leaks into the image signal. Then, the desired and image signal bands containing the leakages are filtered, respectively. Finally, the image signal is suppressed by the LMS algorithm in digital signal processing.

In this paper, we propose a novel scheme for a digitally-assisted image signal rejection; two analog signals from I/Q mixers are converted into digital values by a complex band-pass Δ-Σ modulator, and then frequency shifting is exploited in the digital signal processing. This combination achieves a larger IRR because the desired signal is centered at 0 Hz by the frequency shifting and the image signal can be filtered out by a steep LPF (low-pass filter). Our proposed image rejection scheme is designed for 433-MHz sensor network application, but is easily extended to a general low-IF receiver. Note that, in this paper, mismatches in a mixer is not discussed; the proposed scheme can be, however, well matched with the conventional LMS algorithm because we process the signals in the digital domain.

3. Proposed Architecture

After an RF (radio frequency) signal is down-converted to ω_{IF}, output signals are handled as two real numbers: I for the real part and Q for the imaginary part. The I signal is regarded as cosine waves (clockwise and counter clockwise), and the Q signal is a sine wave as follows:

$$I + iQ = \cos(\pm\omega_{IF}t) + i\sin(\omega_{IF}t) = e^{i\omega_{IF}t}$$

From this equation, we have to reject the image frequency of $-\omega_{IF}$.

The proposed architecture is illustrated in Fig. 3. The RF signal is down-converted to the I/Q signals by an LO (local oscillator) and mixers. Then, the Δ-Σ modulator digitizes the I/Q signals into digital values.

F_S (system sampling rate) is 8 MHz for the Δ-Σ modulator, 1-MHz frequency shifter, LPFs, and down sampler.

The outputs of the I/Q mixers have a 1-MHz bandwidth. The I/Q signals are then band-passed and digitalized. Next, the signals are shifted by 1 MHz. At this point the desied signal band is centered at 0 Hz.

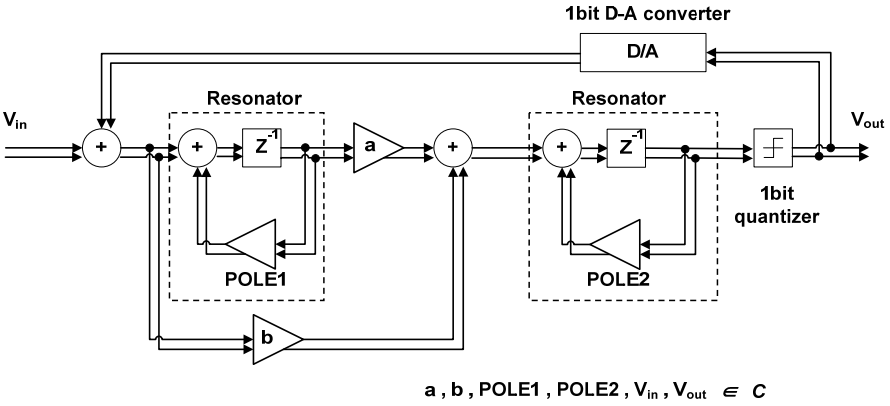

Figure 4. Block diagram of complex band-pass Δ-Σ modulator.

Then the signals are fed to the LPFs for the image rejection. After that, these signals are down-sampled from F_S (8 MHz) to 2 MHz. Here, the desired signal band has still remained around 0 Hz. To address this, the 500-kHz frequency shifter shifts it by 500 kHz. Note that the sampling rate of the 500-kHz frequency shifter is 2 MHz because the signals are already down-sampled to 2 MHz.

The detailed functions of the circuit blocks will be described below:

3.1. Complex Band-Pass Δ-Σ Modulator

As inputs, we have the two signals: I and Q. In the conventional scheme, two real ADCs are used in parallel; one is for the I channel, and another is for the Q channel [5]. When the outputs of the two real ADCs are combined to I + *i* Q, the noise shaping characteristics for the positive and negative frequencies become the same in the conventional scheme.

Instead, we utilize the complex ADC, and thus can discriminate between the positive and negative frequencies. In other words, we can fully handle the negative frequencies of $-F_S / 2$ to the positive one of $+F_S / 2$. As the Δ-Σ modulator, we adopt a second-order complex band-pass ADC (analog-to-digital converter) [5], which can efficiently filter a narrow band. This architecture is suitable for multi channel communication and/or cognitive radio.

Fig. 4 is the block diagram of the second-order complex band-pass Δ-Σ modulator. Design of the NTF (noise transfer function) is very considerable because the NTF fixes the specifications of the modulator: an SNR (signal-to-noise ratio) and bandwidth. We design the NTF as

$$NTF = \frac{(1 - ZERO1 \cdot z^{-1})(1 - ZERO2 \cdot z^{-1})}{(1 - POLE1 \cdot z^{-1})(1 - POLE2 \cdot z^{-1})}$$

In the above equation, *ZERO1* and *ZERO2* are transmission zeros of the NTF. *POLE1* and *POLE2* are poles. By assigning the transmission zeros to the desired band, the optimum noise shaping can be achieved.

3.2. 1-MHz Frequency Shifter and Decimation

After the analog I/Q signals were converted into digital numbers, the signal frequency is then shifted. The frequency shift is represented as

$$e^{i\omega_1 t} \cdot e^{i\omega_2 t} = e^{i(\omega_1 + \omega_2)t}$$

The amount of the frequency shifting is 1 MHz. By doing so, the desired signal band is centered at 0 Hz.

Fig. 5 depicts the block diagram of the 1-MHz frequency shifter. It is comprised of LUTs (lookup tables) for sine and cosine functions and switches for signal routing; the I and Q outputs from the Δ-Σ modulator control the switches. The LUTs feeds 1-MHz sine and cosine waves; the four switches multiply them by the Δ-Σ modulator's outputs.

Fig. 6 is a conceptual diagram of the frequency shifting. The desired signal band moves to 0 Hz; as well, the image signal is shifted to a negative high frequency. Therefore, we can simply attach real LPFs, which filter out the image signal band and quantization noise of the Δ-Σ modulator, too. Then, the outputs are down-sampled into the Nyquist frequency. This procedure is called decimation.

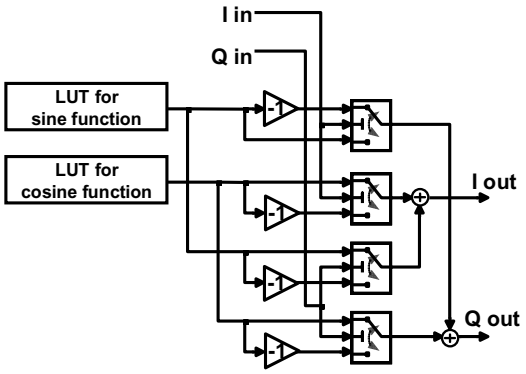

Figure 5. 1-MHz frequency shifter.

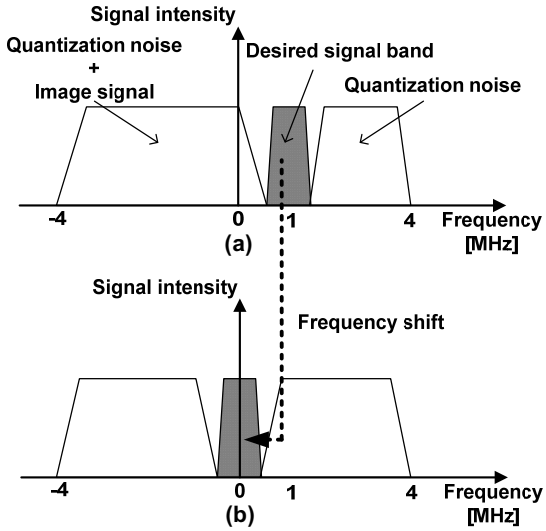

Figure 6. Spectrums (a) before and (b) after frequency shifting.

Note that these LPFs also serve as anti-alias filters. This means that a dedicated decimation filter is not needed, and an additional power and area for it can be reduced.

3.3. 500-kHz Frequency Shifter

After the image rejection and decimation, again frequency shifting is carried out because the desired band spreads from negative to positive frequencies around 0 Hz. Fig. 7 is the block diagram of the 500-kHz frequency shifter. The basis of the function is almost the same as the 1-MHz frequency shifter, but

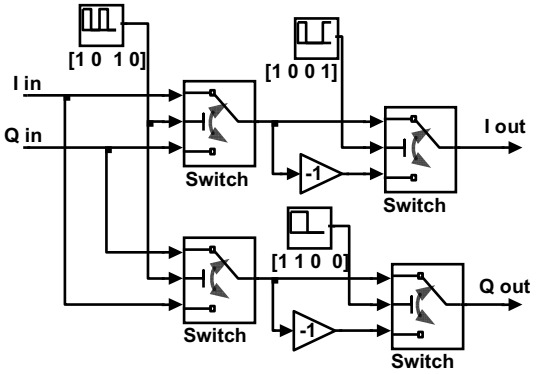

Figure 7. 500-kHz frequency shifter.

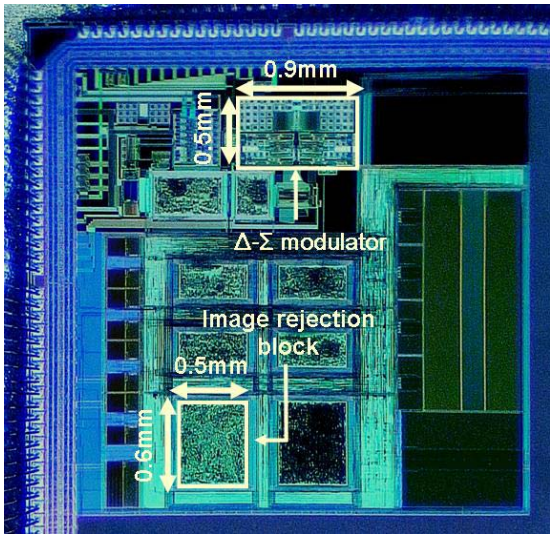

Figure 8. Die photograph.

switching with rounded sine and cosine waves is different. This frequency shifter achieves the 500-kHz frequency shift such as 1, i, –1, $–i$, by utilizing the 2-MHz sampling rate.

4. Chip Implementation

We designed and fabricated the test circuits of the Δ-Σ modulator and image rejection block (two frequency shifters and decimation filter) in a TSMC 0.18-um mixed-signal. The nominal supply voltage is 1.8 V. Fig. 8 is a photograph of a prototype chip. The respective areas of the Δ-Σ modulator and image rejection block occupy 0.9 x 0.5 mm^2 and 0.6 x 0.5 mm^2 (0.75 mm^2 in total).

The Δ-Σ modulator is implemented with switched-capacitor integrators and MIM (metal-insulator-metal)

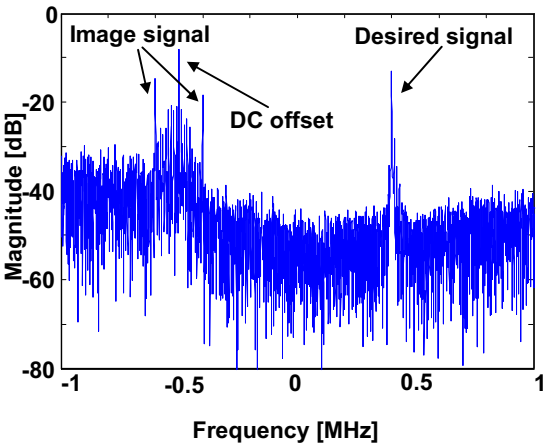

Figure 9. Measured results of output spectrums (I + i Q): Δ-Σ modulator's outputs before image rejection

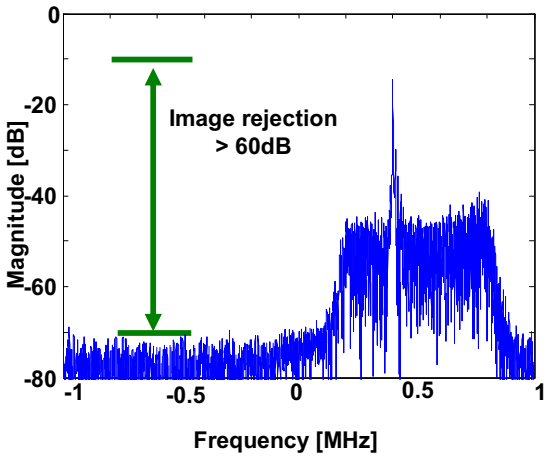

Figure 10. Measured results of output spectrums (I + i Q): Δ-Σ modulator's outputs after image rejection.

capacitors. The image rejection block is fully digital, which is synthesized with a standard cell library. The design specification of the chip is summarized in Table 1.

5. Experimental Results

The total power of the test chip is 6.0 mW at the supply voltage of 1.8 V. The Δ-Σ modulator dissipates 1.3 mW. The image rejection block consumes 4.6 mW.

Fig. 9 & Fig. 10 is a measured result of the image rejection. We input an image frequency of 100 kHz and a desired frequency of 900 kHz into the (the IF is 500 kHz). The respective signals are shifted to –400 kHz and +400 kHz by the frequency shifter. Fig. 9 shows the original input spectrum from the Δ-Σ modulator. The image and desired signals are at –400 kHz and +400 kHz. A DC offset generated by the Δ-Σ modulator is also observed.

Fig. 10 exhibits the image suppression in our proposed architecture. The image signal at –400 kHz and DC offset are vanished. The IRR of 60 dB is achieved.

6. Conclusion

We proposed a 60 dB image rejection filter, and verified its performance by a test chip. The image rejection is digitally processed after a Δ-Σ modulation. The desired signal band is centered to 0 Hz, and other signals including the image signal are filtered out by LPFs. These LPFs also act as a decimation filter. The

Table 1. Chip specification.

System		
Process	CMOS	180nm
Supply voltage	Single supply	1.8V
Carrier frequency		433.67-434.17MHz
LO frequency		432.87MHz
IF frequency		500kHz
Channel bandwidth		200kHz
Sampling rates	Δ-Σ modulator	8MHz
	1-MHz frequency shifter	8MHz
	Decimation	8MHz
	500-kHz frequency shifter	2MHz
SNR	Δ-Σ modulator	40dB
Power	Δ-Σ modulator	1.3mW
	Image rejection block	4.6mW
	Total	6.0mW

area of the test chip is 0.75 mm^2 in a 0.18-um mixed-signal process. The power is 6.0 mW at 1.8 V.

Acknowledgement

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