An Inter-Die Variability Compensation Scheme for 0.42-V 486-kb FD-SOI SRAM using Substrate Control

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Abstract

We propose a novel substrate-bias control scheme for FD-SOI SRAM that suppresses inter-die variability and achieves low-voltage operation. Substrate-bias control circuits automatically detect an inter-die threshold-voltage variation, and then maximize read/write margins of memory cells. We confirmed that a 486-kb SRAM operates at 0.42 V, in which an FS/SF corners can be compensated as much as 0.14 V or more.

Introduction

According to the ITRS Roadmap, SRAM will occupy more than 80% of a chip in 2013. This implies that SRAM is the most sensitive part to threshold variability and thus dominates operating margins on a whole chip. To suppress inter-die variability, a body-bias control scheme has been proposed in a classical bulk process [1]. In a bulk process, however, body bias is limited to around 0.6 V due to forward junction leakage; the threshold-voltage compensation turns out in a small range. To make matter worse, a reverse bias incurs GIDL in a short-channel bulk process. Another backgate-bias control scheme in an FD-SOI process adaptively changes backgate bias of memory cells in read and write operations [2], but the backgate bias itself and backgate contacts impose a cycle-time penalty and area overhead.

Proposed Substrate-Bias Control Scheme

In SRAM, a respective FS and SF corners determine minimum read and write operating voltages [3]. Because an FD-SOI has smaller intra-die variability than a bulk process [4], process variation from the FS to SF corners directly affects a yield of SRAM. Fig. 1 (a) illustrates the relationship between the process corners and read/write limits (i.e. read/write margins), when a supply voltage (Vdd) is changed.

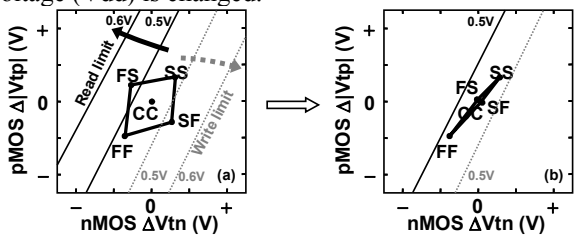

Fig. 1. Read/write margins:
(a) before and (b) after inter-die variability compensations.

Figs. 2 (a) and (b) are measured Id-Vgs curves of an nMOS and pMOS, respectively, when a substrate bias (Vsub) is applied from a substrate (see Fig. 1 (c)). The forward bias increases Vtn and decreases |Vtp|, whereas the reverse bias exhibits the opposite characteristics. In other words, the FS and SF corners can converge on the CC corner after applying the substrate bias, as shown in Fig. 1 (b). Note that this substrate-bias control changes threshold voltages of all nMOSes and pMOSes on the substrate; therefore, there is no area overhead in a memory cell (Fig. 2 (d)). In a future advanced process, the substrate bias can be lowered because a buried oxide is thinning.

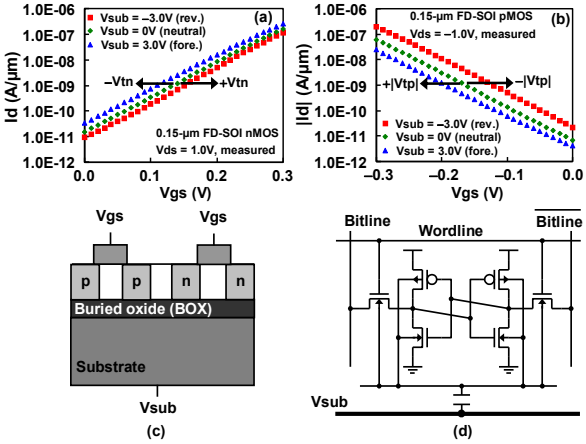

Fig. 2. FD-SOI devices: Id-Vgs characteristics of
(a) nMOS, and (b) pMOS when Vsub is changed,
(c) structure, and (d) memory cell.

Fig. 3 (a) depicts a block diagram of the proposed substrate-bias control circuit. The Vt detector in Fig. 3 (b) outputs information on an inter-die variation as a "Detect" signal. If a die is at the FS (SF) corner, "Detect" becomes a lower (higher) voltage than Vdd/2. Hence, to sense process variation, we should compare "Detect" with Vdd/2.

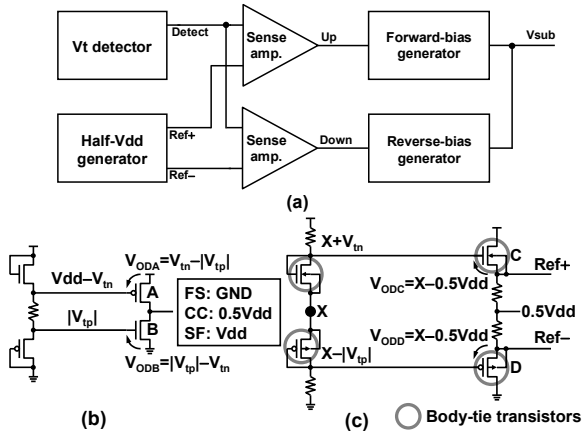

Fig. 3. Proposed body-bias control circuits:
(a) block diagram, (b) Vt detector, and (c) half-Vdd generator.

The half-Vdd generator using body-tie transistors in Fig. 3 (c) provides slightly higher and lower voltages than Vdd/2 (Ref+ and Ref–) regardless of process

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variation, which are to be compared with "Detect" in the sense amplifiers. Fig. 4 shows the simulated outputs of the Vt detector and half-Vdd generator. Based on the sense amplifier outputs, the substrate bias are controlled by feedback so that "Detect" is always between Ref+ and Ref–. In this way, the FS/SF corners converge on the CC corner.

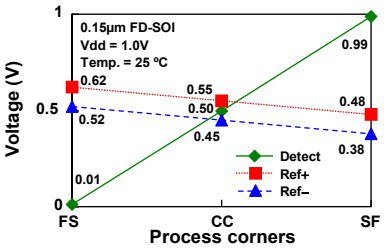

Fig. 4. Simulated outputs of Vt detector and half-Vdd generator (Vdd = 1.0 V, room temperature).

Measurement Results of Substrate-Bias SRAM

Fig. 5 is a chip micrograph of the proposed 486-kb substrate-bias SRAM (SBSRAM).

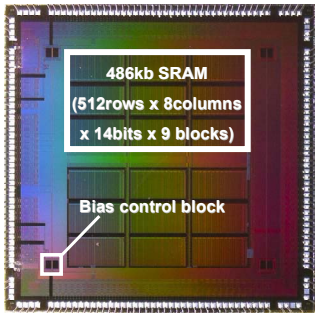

Fig. 5. A 486-kb SBSRAM in 0.15-μm FD-SOI process (512 rows x 8 columns x 14 bits/word x 9 blocks).

Fig. 6 illustrates the measured bit error rates (BERs) at the FS corner. Fig. 6 (a) is a case of read operation; the minimum read operating voltage (Vmin_r) is 0.56 V when Vsub = 0 V. By applying the reverse bias, Vmin_r is improved. In contrast, the forward bias degrades the read margin.

Fig. 6 (b) shows retention voltages; the retention voltage is 0.36 V at the neutral bias, and is improved with the reverse bias as well as the read operation.

Fig. 6 (c) is the BER in the write operation. At the neutral bias, the minimum write operating voltage (Vmin_w) is 0.36 V. Although Vmin_w must be deteriorated with the reverse bias physically, it is improved when Vsub = –2 V. This is because the retention voltage governs the write margin on this condition. As the reverse bias deepens to less than –2 V, again Vmin_w worsens, which is physically reasonable.

When Vsub = –4 V, we confirmed that the 486-kb SRAM works fine at 0.42V. In this case, Vmin_r is compensated as much as 0.14 V. Fig. 7 exhibits the leakage powers with and without the proposed substrate-bias control scheme. The SBSRAM saves the leakage power by 41%. Note that the low-voltage operation is also effective to gate leakage and NBTI in a future process.

Furthermore, the proposed scheme can be combined with other techniques that suppress intra-die variability [5-6]; the combination minimizes the both inter- and intra-die variability.

Acknowledgment

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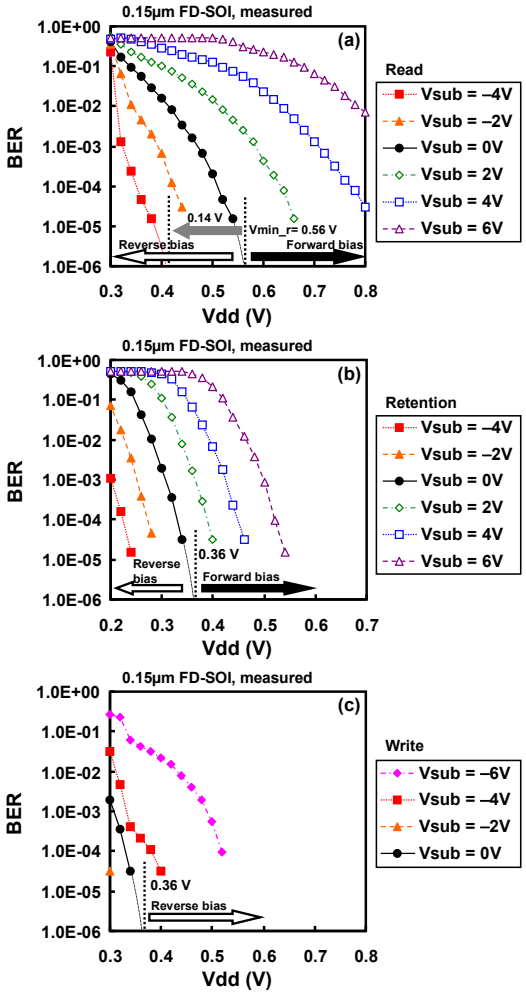

Fig. 6. Measured bit error rates (BERs): (a) read, (b) retention, and (c) write.

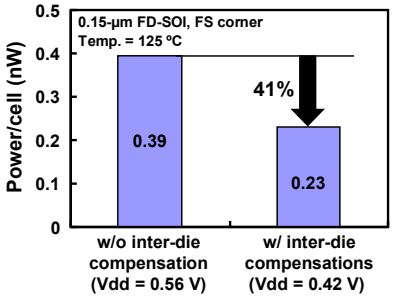

Fig. 7. Leakage powers.