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Design Rule for Frequency-Voltage Cooperative Power Control and Its Application to an MPEG-4 Decoder

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Abstract

Frequency-voltage cooperative power control (FVC) is considered a powerful method to reduce the power consumption of a program, because it utilizes the information of software loads dynamically. The authors first show through a mathematical analysis that FVC with only two frequency-voltage sets is sufficient for current low-Vdd CPU chips. Then we show an experimental result that FVC feedback control on an MPEG-4 video decoder can reduce the power to one-fourth.

Introduction

Power consumption has become one of the major problems in VLSI design, as the integration scale grows larger, especially in chips for mobile application. To reduce the power, many hardware and software techniques have been introduced. Frequency-voltage cooperative power control (FVC) is one technique, which lowers both clock frequency (F) and power supply voltage (V) when lower speed is required[1][2]. Though this technique is effective because both low F and V reduce the power, it requires an additional circuit with an LSI to lower them. This causes a new design problem: how to specify values of F and V. From this mathematical investigation, we have derived a design rule that solves this problem.

1. Modeling the frequency-power (F-P) relationship

We first define the frequency-power (F-P) characteristics of a LSI chip. Fig.1 shows a typical F-P characteristic curve showing the minimum power consumption of a chip when its operation clock frequency (F) is given. In the case of an LSI design, the F-P curve depends on many design parameters. We assume the curve can be modeled by (1).

$$P = k'F : F \leqq Fm,\ P = kF^{\gamma} : F \geqq Fm \qquad (1)$$

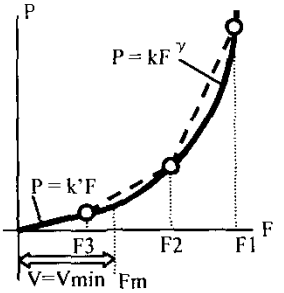

Fig.1 assumed F-P relation

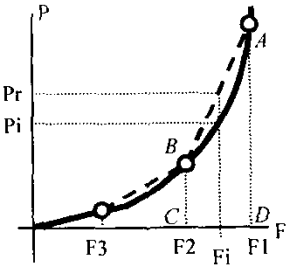

Fig.2 evaluation of power loss at Fi and between F2 and F1

The curve consists of two parts: the left half is a straight line beginning at the origin, and the right half is an algebraic curve of order γ. Both halves meet at the point defined as frequency Fm. In the left half, the power is linearly proportional to frequency, meaning that the operation voltage is constant, because any LSI chip has a minimum operation voltage (Vmin). In the right half, the operation voltage increases in accordance with frequency. Both F and V affects power, which thus increases with an order γ greater than 1.0. Though there is no physical evidence that supports use of (1), through our experience we consider that it is good enough for modeling a real chip.

2. F-P relationship on discrete clock frequency

Fig.1 assumes that F and V can be set to any value or can be changed continuously. This requires a large circuit and is not practical in LSIs for commercial use. We thus assume that the clock frequencies are defined discretely, namely, F1, F2, F3, and so on. Then the F-P curve is represented as the dashed line in Fig.1, i.e., approximating the curve piecewise-linearly with nodes at the defined frequencies [1][2]. Fig.2 shows how we can evaluate the power loss in the discrete clock frequency (DCF) condition. The chip can complete the task requiring Fi with the power Pi ideally. However, it consumes real power Pr because of DCF, and the ratio of Pi to Pr gives us the relative power loss.

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3. Power loss calculation

As our goal is to determine the frequency set F1, F2, F3, ..., we introduce some more definitions next. First, the highest frequency F1 is given *a priori*, according to the requirements for an application or to the circuit specification. Second, we introduce a new parameter β representing the ratio F1/F2 so that we can determine F2 from F1. (F3 and latter ones can be determined in the same manner if required.) Third, the "junction point frequency" Fm is represented implicitly as in (2) and (5). After these definitions we derive two equations: the maximum power loss and the average one, both is relative to the ideal.

Because the F-P curve model (1) is homogeneous, we can exclude the parameters k and k' from the expressions of relative power loss shown below.

A. Maximum loss

Relative loss R, equals to Pr/Pi, at each F is given by (2), where the F is implicitly represented by α, i.e., normalized by F2 (Fm $\leqq$ F assumed here):

$$R(\alpha) = (\alpha^{\gamma}(K\beta - \beta^{\gamma}) + \alpha^{\gamma-1}(\beta^{\gamma} - K))/(\beta - 1) \quad \text{where } K = (Fm/F2)^{\gamma-1},\ \alpha = F2/F \tag{2}$$

To find the maximum power we differentiate (2) with α and find the zero of the differential. The result $\alpha 0$ is represented as (3):

$$\alpha 0 = (\gamma - 1)(\beta^{\gamma} - K) / \gamma\beta(\beta^{\gamma-1} - K) \tag{3}$$

Substituting α of (2) by (3) gives the maximum loss.

B. Average loss

It is considered useful to know the average loss of a DCF control, for Fi may vary widely in a real application. When there are many tasks that require certain Fi, namely, Fi(1), Fi(2), and so on. Our aim is to compute the ratio:

$$\sum_{n} Pr(Fi(n)) \Big/ \sum_{n} Pi(Fi(n)) \tag{4}$$

However, if the Fi's are distributed in the range from F2 to F1 uniformly, the two sums in (4) can be approximated by the area under the curve; i.e., the ideal power consumption by the hatched area in Fig.2, and the real one by that of the trapezoid *ABCD*. Thus we can get (5), where Fm position is normalized by F1:

$$\frac{\rho^{\gamma-1}(\gamma+1)(1+1/\beta\,\rho^{\gamma-1})(1-1/\beta)}{(\gamma+1)(1/\rho^2 - 1/\beta^2) + 2\rho^{\gamma-1}(1-1/\rho^{\gamma+1})} \quad \text{where } \rho = Fm/F1 \tag{5}$$

4. Numerical results

Tab. 1 lists the calculated power loss from (3) and (5), for typical β, γ and Fm. In the table, the ratio is represented; i.e., 1.00 means no power degradation. Under condition (a) (Fm equals to F2), considering that γ seldom exceeds 2.5, we can conclude that β of 2.0 is enough for power reduction with only 13% average loss. Under condition (b) (Fm at the midst of F1 and F2) the power loss is much worse, though, it still remains around 20%, which is considered acceptable for most LSI design. The authors recommend that β of 2.0 is appropriate for an FV-control.

TABLE 1 POWER LOSS RATIO

	β \ γ	1.5	2.0	2.5	3.0
(a) Fm = F2	1.5	1.01 1.02	1.03 1.04	1.05 1.08	1.08 1.13
	2.0	**1.03** **1.05**	**1.07** **1.13**	**1.13** **1.24**	1.20 1.41
	3.0	1.06 1.12	1.15 1.33	1.27 1.69	1.40 2.26
(b) Fm = (F1+F2)/2	1.5	1.03 1.06	1.06 1.12	1.09 1.19	1.13 1.26
	2.0	**1.05** **1.10**	**1.11** **1.22**	**1.17** **1.36**	1.24 1.52
average (5) maximum (3)	3.0	1.09 1.17	1.18 1.38	1.28 1.63	1.39 1.94

5. Applying the design rule to MPEG-4 power control

To confirm our power loss evaluation we adapted an FV-control method to a Hitachi SH-4 CPU chip running an MPEG-4 decoder. The decoder is software-implemented except the video-IO. To change the F and V dynamically a "voltage-hopping algorithm" was attached to the decoder program[3]. Tab. 2 lists the F-P characteristics of the CPU; it shows that γ is 1.6 (i.e., less than 2.5, the criterion), so β of 2.0 is appropriate. F1 is selected as 200MHz, the highest frequency for an SH-4. F2 becomes 100MHz accordingly. This F2 is already under Fm, so additional frequencies are not required except zero, the sleep mode.

Tab. 2 also lists the operation statistics when a typical MPEG-4 stream (31.0% average load) is input. From this statistics we estimate the power reduction ratio as 22.6% from the original. With referring Tab. 1 again, we can conclude the ratio can never be under 20% even if an ideal (continuous) FV generator circuit is attached to the SH-4.

TABLE 2 FV-CONTROL OF AN MPEG-4 DECODER

op. mode	High	Low	Sleep
V [V]	2.0	1.2	-
F [MHz]	200	100	0
P [mW]	600	200	20
exec. Time (%)	3.3	53.5	43.2
ave. power	135.6 (22.6% to High mode)		

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