Managing Leakage in Charge-Based Analog Circuits with Low-V_{TH} Transistors by Analog T- Switch (AT-Switch) and Super Cut-off CMOS

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Abstract

Analog T-switch scheme is introduced to suppress subthreshold-leakage problems in charge-based analog circuits such as switched capacitor and sample and hold circuits. A 0.5-V sigma-delta modulator is manufactured in a 0.15-µm FD-SOI process with low V_{TH} of 0.1V using the concept. The scheme is compared with another leakage suppressed scheme based on Super Cut-off CMOS (SCCMOS) and the conventional circuit which are also fabricated. The sigma-delta modulator based on analog T-switch realizes 6-bit resolution through reducing non-linear leakage effects while the conventional circuit and the scheme based on SCCMOS can achieve 4-bit and 5-bit resolution, respectively.

Keywords: subthreshold leakage, low V_{TH}, FD-SOI, switched capacitor, and sigma-delta modulator

Introduction

Low-voltage, low-power yet inexpensive VLSI's are getting focus recently. To this end, analog building blocks tend to be embedded in scaled digital circuits as a part of SoC implemented with advanced VLSI technology.

Several sub-1V sigma-delta modulators and ADCs are reported but all are implemented in a high-threshold voltage process [1,2,3]. The International Technology Roadmap for Semiconductors (ITRS) predicts that the threshold voltage (V_{TH}) of high-performance logic technology will ever decrease. In the above-mentioned environments, very low V_{TH} process compatible with the mainstream scaled digital circuits are to be used. In the low V_{TH} process, however, non-linear subthreshold leakage current can be a critical issue on analog circuits in press [4].

To suppress the subthreshold-leakage problems for switched capacitor (SC) circuit, a scheme based on Super Cut-off CMOS (SCCMOS) [5] was proposed in press [4]. This scheme, however, handles voltage outside the power rails and thus oxide-stress relaxed level shifter and a negative voltage generator such as charge pump circuit is required [6].

In this paper, analog T-switch scheme, which can realize reverse gate-source voltage (V_{GS}) without voltages outside the power rails, is introduced to suppress subthreshold leakage for charge-based analog circuits, and the performance and advantages are discussed by comparing with the conventional scheme and the SCCMOS scheme.

Circuit Design

Figure 1 shows a schematic of a switched capacitor integrator using the proposed analog T-switch scheme for leakage suppression. $M_{1a\sim c}$ and $M_{2a\sim c}$ are the analog T-switch that consists of two series-connected MOSFET's and intermediate voltage controlling MOSFET. Figure 2 explains why the leakage can be suppressed. The analog ground is set to a proper voltage between V_{SS} to V_{DD}. $V_{DD}/2$ is used as an example in this paper. All MOS switches are driven by non-overlapping clocks whose swing is between V_{SS} to V_{DD}.

During the sampling phase, the gate voltage of M_{3b} is set to V_{SS} and that of M_{3a} is set to V_{DD} to cut them off deeply. When the input signal is around V_{DD}, which corresponds to upper left figure in Fig. 2, the node "A" is set to V_{IN} through M_{2a} and M_{2b}. Although M_{3a} is still leaky, the gate-source of M_{3b} is reversely biased by $V_{DD}/2$ and M_{3b} is completely cut off. If $V_{DD}/2$ is 0.25V, the leakage is reduced by two orders of magnitude.

When the input signal is around V_{SS}, as in upper right figure, the gate-source of M_{3a} is reversely biased although the M_{3b} is leaky. In this case, M_5 is also reversely biased since the node "B" is always set to $V_{DD}/2$ through M_4.

During the evaluation phase shown in the lower figures, the gates of M_{1a} and M_{1b} are both set to V_{SS} and the gates of M_{2a} and M_{2b} are set to V_{DD} to cut them off. The node "C" and node "D" are connected to $V_{DD}/2$ in this phase through M_{1c} and M_{2c} respectively. Then, both of the V_{GS} of M_{1b} and M_{2b} are reversely biased and they are deeply cut off even though M_{1a} and M_{2a} are leaky. M_4 is also reversely biased since the node "B" is always set to $V_{DD}/2$ through the M_5. Since this integrator scheme is insensitive to parasitic capacitances integrator, added parasitic capacitance introduced by the proposed scheme do not affect the operation [7].

Experimental Results and Discussion

Both of the analog T-switch scheme and the conventional scheme are applied to 1st-order low-pass sigma-delta modulators implemented in the afore-mentioned 0.15-µm FD-SOI technology. The same circuit topology, parameters, and layout style except for the switch array are adopted in order to fairly compare various switched-capacitor circuits. The circuit is operated under 0.5-V V_{DD}.

Figure 3 shows measured SNR's and SNDR's. For the comparison, SNDR by SCCMOS scheme is also plotted. The conventional scheme achieves the peak SNR of 44dB. The SNDR of the conventional scheme, however, is degraded to 31.5dB which is below 5-bit resolution. The maximum power consumption is 71μW. The proposed scheme achieves the peak SNDR of 39.6dB which realizes more than the 6bit resolution with the maximum power consumption of 75μW. The peak SNDR and the dynamic range are improved over the conventional approach at the same time. The SNDR by the analog T–switch exceeds that of the SCCMOS by 5.8dB. This result indicates that the analog T-switch scheme can cut off the leakage more deeply than the SCCMOS approach since more reverse V_{GS} is applicable without voltage over-stress across gate oxide.

The cause of the degradation of SNDR in the conventional approach due to the charge loss associated with the leakage of low-V_{TH} transistors is shown in Fig. 4. This leakage current introduces non-linear errors during the evaluation phase of SC circuit and thus the error caused by the leakage current cannot be compensated by digital manipulation.

Figure 5 shows measured output power spectra. The output bit streams are processed using Matlab. The output spectrum of the conventional scheme is taken at the input level of –7.6dB and the large harmonic tones that degrade SNDR are observed. This is due to the leakage current that introduces non-linear errors. The proposed scheme shows the peak SNDR at the input level of –7.6dB. It is seen that higher-than-the-third order tones are greatly suppressed compared with the conventional circuit.

The chip microphotographs of the sigma-delta modulator using the analog T-switch, SCCMOS and the conventional scheme are shown in Fig.6. Area is 130μm×190μm. Although the switch transistor area of the analog T-switch increases to 3.3 times of the switch transistor area of the conventional circuit, the switch array area is almost unchanged. This is because the switch transistors are placed according to the pitch of capacitors and even if the number of switch transistors are more it does not give much area overhead. TABLE I summarizes comparison between two types of leakage suppressed switch scheme and the conventional scheme.

There are two useful circuit configurations in the analog T-switch family. One is an NMOS switch substitute and the other is a PMOS switch substitute as shown in Fig. 7. The analog T-switch version of the NMOS and PMOS switches can be considered as leakage-suppressed NMOS and PMOS switches, respectively, for wide range of applications. One of such applications is found in a sample & hold circuit with switched current configuration. SPICE simulation results on the switched current sample & hold using the conventional leaky switches and using the analog T-switch scheme are shown in Fig.8. Device model employed is the afore-mentioned 0.15-μm FD-SOI. The conventional leaky switch cannot sufficiently cut off node TP from IN during a hold phase. Since C_1 is small, TP tends to tracks the voltage of IN, and waveform is sinusoidal as a result. On the contrary, TP is isolated from the node IN in the implementation with the analog T-switches. The analog T-switch concept is considered to be applicable to other charge-based analog circuit.

Conclusion

Analog T-switch scheme is introduced and applied to a 0.5-V sigma-delta modulator implemented in a 0.1V-V_{TH} 0.15-μm FD-SOI process and experimentally verified. The analog T-switch realizes 6-bit resolution by reducing non-linear leakage effects caused by the leakage and loss of charge through low-V_{TH} transistors. The performance of the circuit based on the proposed analog T-switch exceeds that of the SCCMOS and the conventional scheme. The analog T-switch can be applied to extremely low-V_{TH} devices even to depletion MOSFET's, since reverse V_{GS} is effectively achieved without voltage over-stress to gate oxide.

The analog T-switch is shown to be also applicable to other charge-based analog circuit using sample and hold circuit. The proposed T-switch scheme and the SCCMOS both suppress non-linear leakage-current effects in charge-based analog circuits and boosts circuit performances in the forthcoming leaky low-V_{TH} transistor generations.

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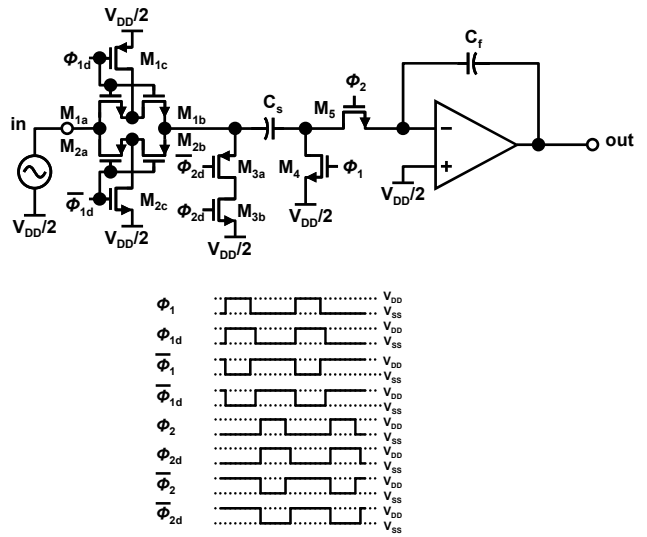


Fig.1. Schematic of a switched capacitor integrator using the A T-switch scheme. $M_{1a\text{-}c}$ and $M_{2a\text{-}c}$ are T-switch.

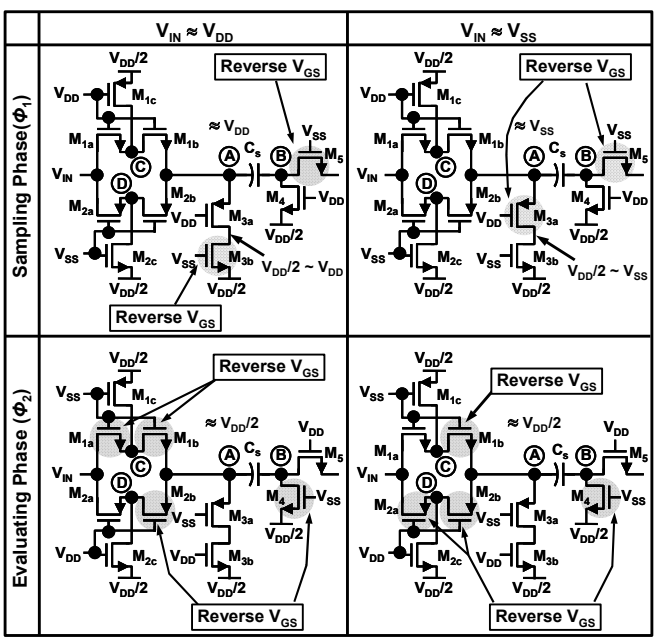


Fig.2. Principle of the analog AT-switch scheme. Subthreshold leakage is suppressed by reverse-V_{GS} handling voltage outside the power rails.

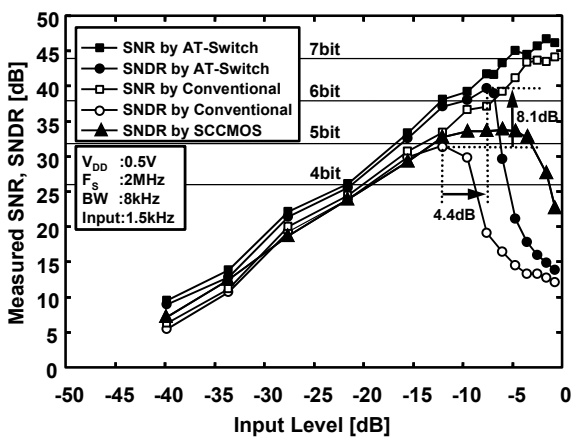


Fig.3 Measured SNR's and SNDR's. The SNDR by SCCMOS is also plotted for the comparison.

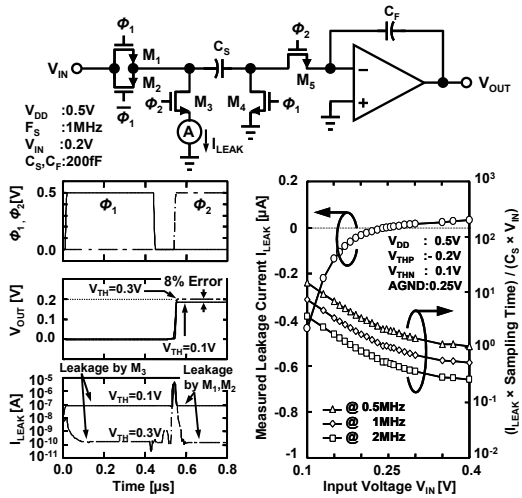


Fig.4. Schematic, SPICE simulation, and Measured Leakage of a conventional switched capacitor integrator.

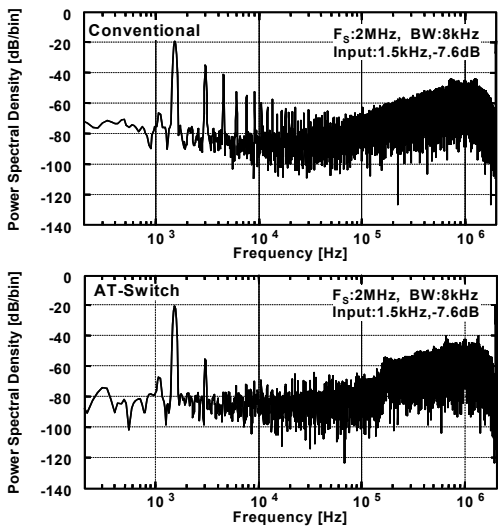
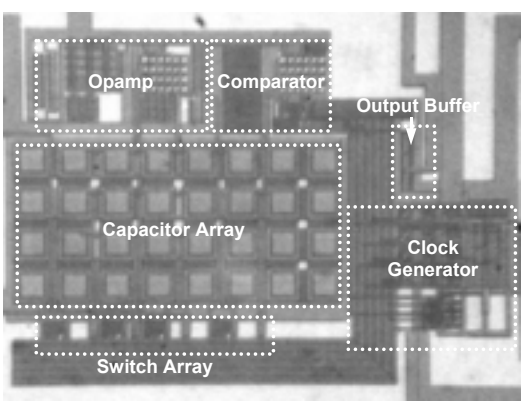


Fig.5. Measured output power spectra.



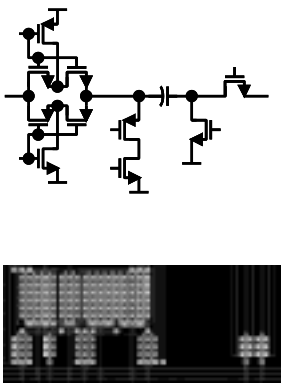
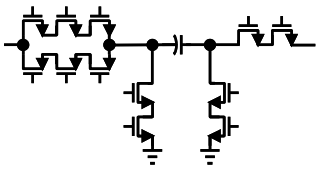
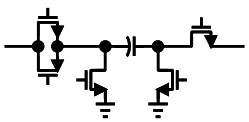
(a) Whole sigma-delta modulator using proposed AT-switch

(b) Switch array of the SCCMOS

(c) Switch array of the conventional

Fig.6. The chip microphotographs of the sigma-delta modulator analog T-switch, SCCMOS and the conventional

TABLE I
SUMMARY OF COMPARISON ON LEAKAGE SUPPRESSED SWITCH SCHEME

	AT -Switch	SCCMOS	Conventional
Switch Array Number of MOS in Each Integrator, Schematic, Layout	10 transistors 	12 transistors  	5 transistors  
Switch Array Area	3.3** 4% of Total Area*	4.4** 5% of Total Area*	1** 1% of Total Area*
Level Shifter		Required 3% of Total Area*	
Clock Bus Width	1**	2** 5% of Total Area*	1**
Applicable Analog GND	around $1/2V_{DD}$	V_{SS} to $1/2V_{DD}$ (NMOS) $1/2V_{DD}$ to V_{DD} (PMOS)	V_{SS} to $1/2V_{DD}$ (NMOS) $1/2V_{DD}$ to V_{DD} (PMOS)
Extra Supply Voltage		V_{DDH}(ex V_{DD}+0.2V) V_{SSL}(ex V_{SS}-0.2V) (V_{DDH} 0.6μW, V_{SSL} 3.9μW)	
P-well Isolation		Required (Triple well, Deep n-well, FDSOI))	
Oxide Stress	Inherently Free	Relaxed by Stack Structure	Inherently Free
Applicable V_{TH} of MOS Switch	Extremely Low-V_{TH} (ex. <0.1V) Depletion MOS	Low V_{TH} (ex. V_{TH}=0.2V@0.5V V_{DD})	Medium V_{TH}
Parasitic Capacitance by M_4, and M_5	1**	4**	1**
0.5V Sigma-Delta ADC Peak SNDR	39.6dB	33.8dB	31.5dB

* Total area of sigma-delta modulator: 130μm×190μm
** Normalized by conventional

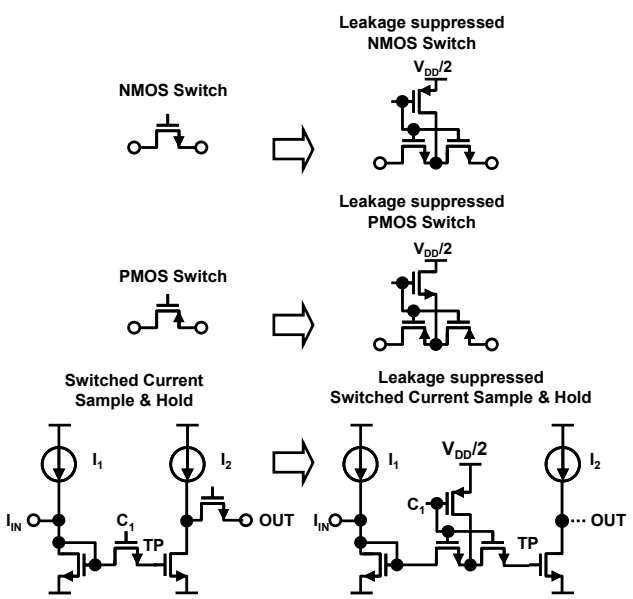


Fig.7. Leakage suppressed switches using AT-switch scheme.

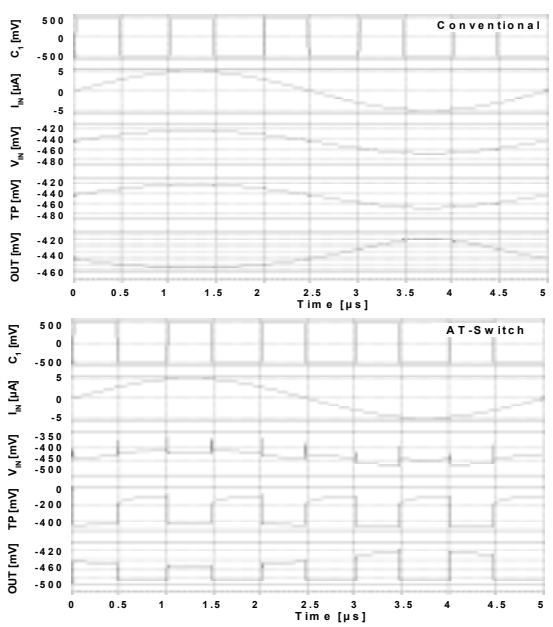


Fig. 8.Simulation results of switchet current sample & hold. Upper: conventional leaky switch, Lower: AT-switch scheme.