Experimental Verification of Row-by-Row Variable V_{DD} Scheme Reducing 95% Active Leakage Power of SRAM's

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Abstract

Low-power SRAM has become a critical component in recent VLSI systems. This paper reports an SRAM reducing 95% of active leakage power. The SRAM is successfully implemented and reliably measured for the first time, with self-aligned timing generation to avoid malfunction during V_{DD} transition. The cycle time overhead is 9%, and the area overhead is 3.5%.

Keywords: low active leakage, low power, self-alignment row-by-row variable V_{DD}, and SRAM

Row-by-Row Variable Voltage Scheme

In order to meet the requirements of battery-operated portable equipments, several low standby-power SRAM solutions have been proposed [1-3]. When an SRAM is accessed, whether for a read or a write operation, only a minuscule portion gets activated. All un-selected rows are just consuming leakage power for data retention. Several proposals have been made for leakage power reduction but most of them are applicable only to dormant SRAM blocks. An exception is row-by-row variable voltage (RRVV) scheme, which is applicable even to SRAM blocks that are in operation, and can reduce active leakage. The concept of the RRVV scheme is illustrated in Fig. 1 where a row decoder generates not only a word-line (WL) signal but also an additional cell voltage control signal.

When a row is not accessed (dormant row), either the cell supply voltage, cell V_{DD}, is lowered to a standby value, V_{DDL}, or cell V_{SS} is increased to the higher value, V_{SSH}. Changing V_{SS}, however, increases the cell area by more than 15% and can not be employed without much cost increase, while changing cell V_{DD} requires minimum increase in area. Thus, row-by-row variable V_{DD} scheme is preferable from the area standpoint. When a row is activated, on the other hand, the cell V_{DD} is set to the high voltage, V_{DDH}. V_{DDL} has to be low enough (< 350mV) to achieve more than one order of magnitude leakage reduction and high enough to preserve the stored data.

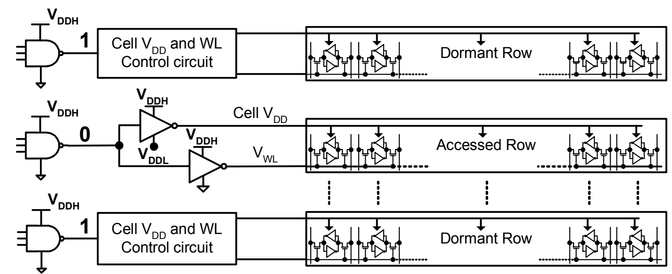

Fig. 1. Row-by-row variable voltage (RRVV) scheme

We found that there is one critical problem in the RRVV scheme. A bit-line (BL) is usually set to V_{DDH} or V_{DDH}-V_{TH} depending on whether the BL precharge occurs through PMOS or NMOS, respectively. As a result, when the row is sleeping, cell node voltage is lower than the BL voltage. If WL goes high before the cell V_{DD}, the two data storing nodes in the cell are charged from the BL. This situation is similar to a write operation and results in the destruction of the stored data. Figure 2 illustrates the situation. Due to this problem, a straightforward and simple implementation of the RRVV scheme does not work properly.

Since the cell V_{DD} line has a larger capacitance than WL, it is usually slower in operation. Then, the WL voltage becomes higher than cell V_{DD} in the rising edges leading to a corrupted butterfly curve as shown in Fig. 3, and to the destruction of the data stored in the memory cell. Without a proper timing control, the same situation can occur at the falling edges of WL and cell V_{DD} when a row is deactivated. In order to solve the above-mentioned problem, care should be taken. What complicates the situation is that both of the WL and the cell V_{DD} line are subject to different RC delays

that may fluctuate from chip to chip. Thus, self-aligned timing generation is needed to achieve the goal.

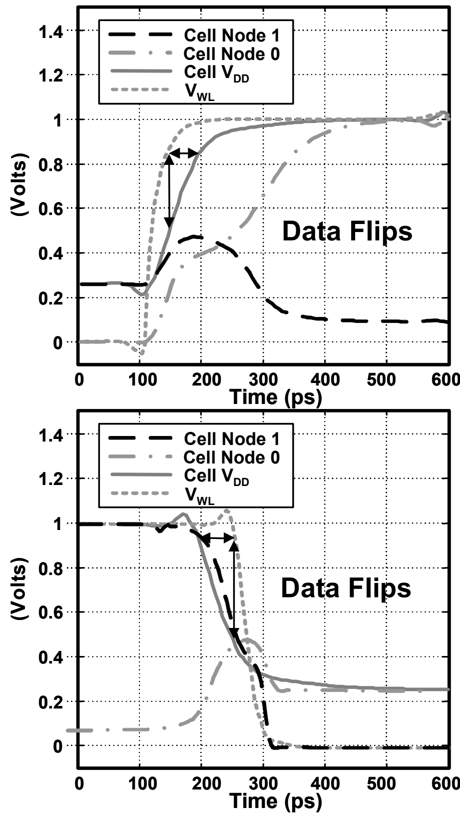

Fig. 2. Malfunction in original RRVV scheme

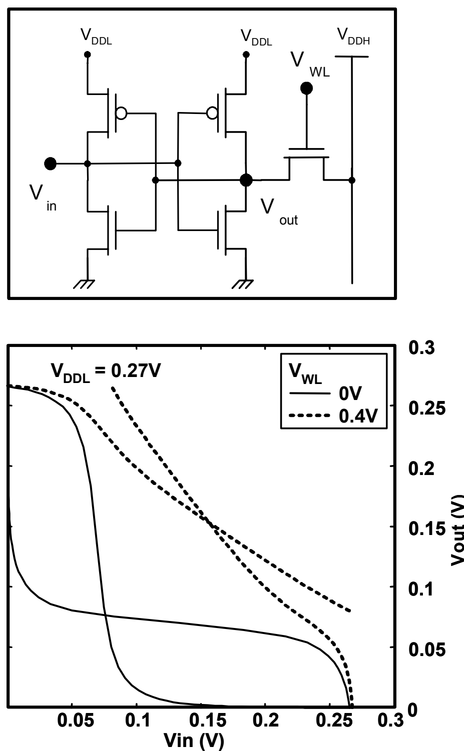

Fig. 3. Corrupted butterfly curve in original RRVV scheme

Self-alignment Row-by-Row Variable Voltage Scheme

In Fig. 4, a self-alignment row-by-row variable voltage (SARRVV) scheme capable of fulfilling the timing requirement for the cell V_{DD} and WL is proposed. The SARRVV scheme is based on a feedback mechanism that takes into account the RC delay fluctuation. For each row, there are two feedback signals: V_{SVF}, which is the feedback signal that controls the timing when the row goes into sleep mode, and V_{WF}, which is a WL feedback signal for a wake-up process. The scheme is split into two parts. The first one resides on the decoder side (front circuit) and the second one is placed at the end of the line (back circuit). DEC is the conventional output of a NAND row decoder. When a row is selected, node A starts rising, and at the same time WL is cut out from the ground, but still holds its value V_{SS}. Cell V_{DD} starts to rise and after some RC delay of cell V_{DD}, the signal reaches node B. V_{WF} starts falling and when the transition edge of V_{WF} reaches node C, WL is pulled up. This way we can ensure that for all the cells in this row, the WL is activated after cell V_{DD} reaches V_{DDH}. When the row is deselected; DEC goes to V_{DD}. The node D immediately starts changing from V_{DDH} to V_{SS}. Cell V_{DD} (node A) will stay high until the feedback signal V_{SVF} is set high (node F) by the decreasing node E. Thus we can ensure that the cell access transistors have been turned off before cell V_{DD} is lowered to V_{DDL}.

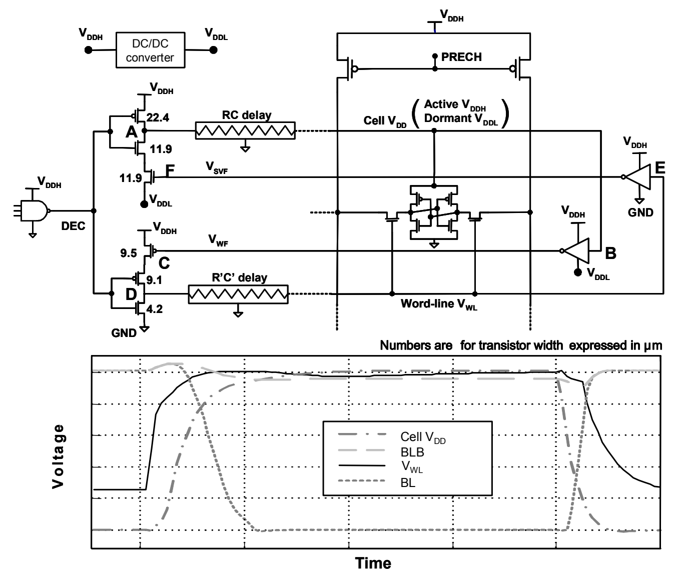

Fig. 4. Self-alignment row-by-row variable voltage (SARRVV) scheme

Since the stored charge in the dormant cell nodes is small, the cell data is more susceptible to coupling noise from BL and feedback signals. A shielding cover is provided to

protect the cell nodes from the coupling noise disturbance by using Metal-2 layer as is illustrated in Fig. 5. Metal-4 layer is used for feedback signals and thus the cell area overhead for the proposed SARRVV scheme is zero.

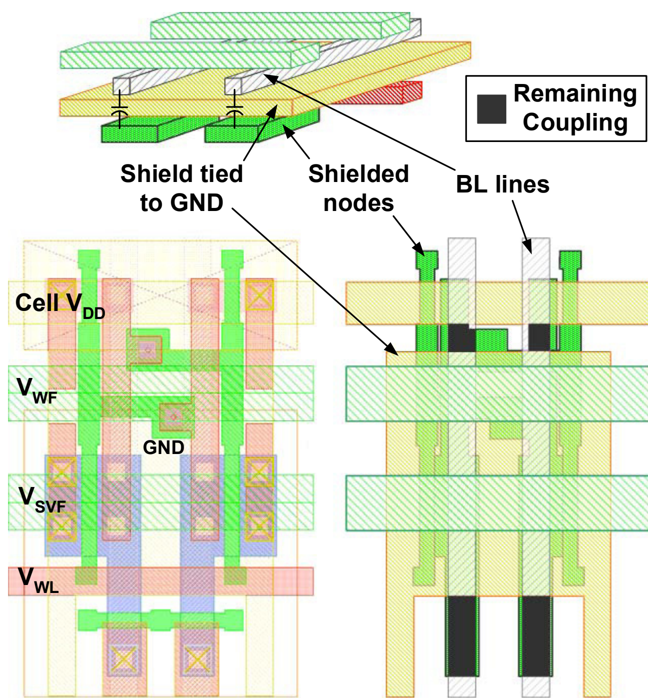

Fig. 5. SRAM cell layout in SARRVV scheme

Simulation and Measurement results

To estimate the delay overhead added by the SARRVV scheme, we consider the time difference between the timing when BL is discharged 50% for the conventional circuit and the same timing for the proposed circuit. SPICE simulation (V_{DDH} = 1V, V_{DDL} = 270mV) shows a 260-ps delay overhead, which corresponds to 9% of the 3-ns clock cycle. One of the benefits of the SARRVV scheme is that the rising edge of WL does not have to be delayed for preventing WL multi-selection problem. Consequently, the actual delay overhead is smaller than 9% of the cycle.

A 16-Kbit (256 columns x 64 rows) SARRVV SRAM test chip has been manufactured using a 0.15-µm FD-SOI process with five metal Layers. Figure 6 illustrates the measured waveforms of one of the data output buffer at V_{DD} of 1V, and a clock frequency of 1MHz. Seven write cycles to different addresses followed by seven read cycles from the same addresses are illustrated. The written and read data match.

The Shmoo plots are shown in Fig. 7. For each point in the Shmoo plot, all addresses are tested with multiple read and write operations using random data. A program for writing and reading to/from all addresses is written and executed with a logic tester. Since the nominal supply voltage for the used process is 1V, V_{DDH} is set between 0.8V and 1.1V, with a step of 0.05V. V_{DDL} varies between 200mV and 800mV with a step of 10mV. We tested the circuit for the typical ($V_{TH\text{-}NMOS}$ = 0.155V, $V_{TH\text{-}PMOS}$ = -0.254V) and fast ($V_{TH\text{-}NMOS}$ = 0.11V, $V_{TH\text{-}PMOS}$ = -0.208V) corners. The lower boundary for V_{DDL} is due to the V_{TH} variation inside the cell and corresponds to the minimum retention voltage. At the nominal supply voltage of 1V, the SARRVV operates successfully for V_{DDL} varied from 260mV to 500mV.

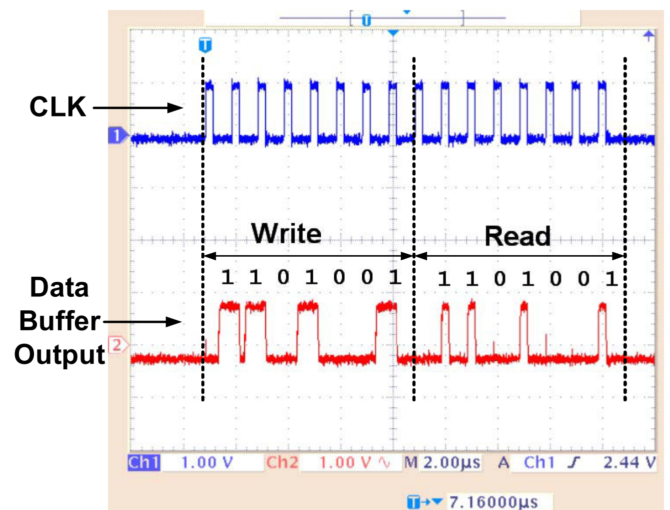

Fig. 6. Output Waveforms of fabricated SARRVV SRAM chip

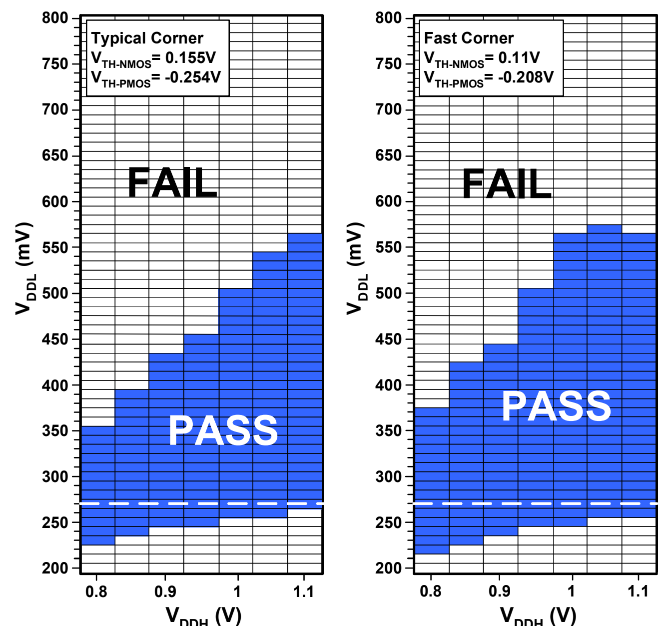

Fig. 7. Shmoo plots of SARRVV SRAM

Figure 8 shows measured and simulated leakage power of the cell array as a function of V_{DDL}. The leakage power has two components, a BL leakage component and a cell leakage component. The SARRVV can reduce the cell leakage power by 96% at 0.3V V_{DDL}. Even though the BL leakage component is much less affected, BL leakage through the cell access transistors is much smaller than the cell leakage since the V_{TH} of the transfer gates tends to be higher than the cell transistors due to the usage of longer channels. In total, more than 95% active leakage power reduction is achievable.

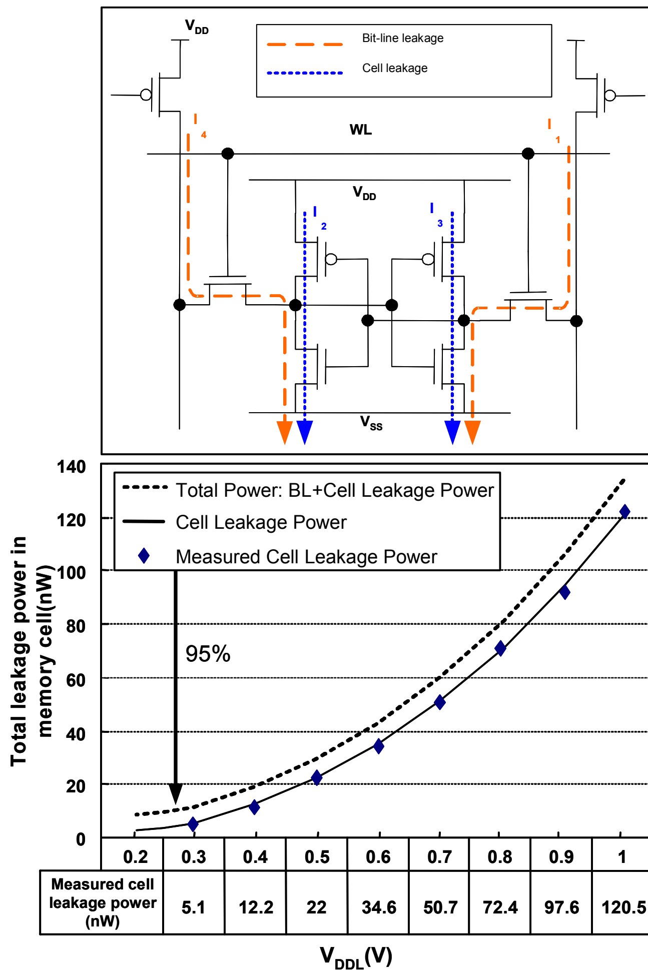

Fig. 8. Measured and simulated leakage power of SARRVV SRAM cell

The micrograph of the chip is shown in Fig. 9. The total area is 604 x 347μm^2. Although there is no overhead for memory cell area, the self-aligned timing control circuit gives rise to area overhead. A 256-bits row occupies 604μm in length and the SARRVV control circuits occupy 31.9μm in length leading to an overhead of 5%. Moreover, according to the ITRS roadmap, the cell array efficiency is typically 0.7. This means that the SARRVV scheme area overhead reduces to 5% x 0.7 = 3.5% of the total SRAM area considering the peripheral circuits. For larger capacity SRAMs, the area overhead is reduced even down to around 2%.

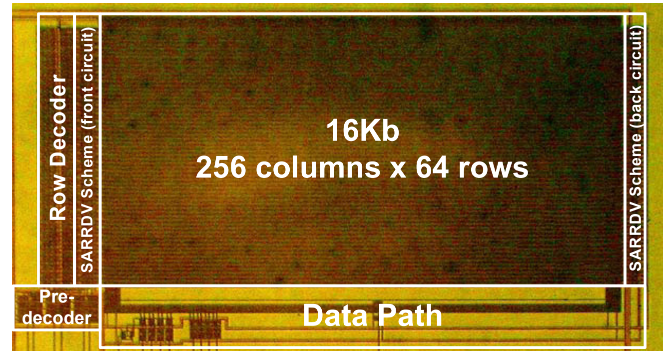

Fig. 9. Chip micrograph

Summary

The self-alignment row-by-row variable voltage (SARRVV) scheme SRAM is proposed. The SARRVV always keep the cell V_{DD} higher than WL voltage to avoid malfunction, and can reduce active leakage power by 95%. The cycle time overhead is less than 9%, and the area overhead is 3.5% in 0.15μm FD-SOI technology.

Acknowledgment

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