An Area-Conscious Low-Voltage-Oriented 8T-SRAM Design under DVS Environment

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Abstract

This paper demonstrates that an 8T memory cell can be alternative design to a 6T cell in a future highly-integrated SRAM, in a 45-nm process and later with large threshold-voltage variation. The proposed voltage-control scheme that improves a write margin and read current, and the write-back scheme that stabilizes unselected cells are applied to the 8T SRAM. We verified that the low-voltage operation at 0.42 V in a 90-nm 64-Mb SRAM is possible under dynamic voltage scaling (DVS) environment.

Keywords: SRAM, 8T, DVS

Area Comparison between 6T and 8T

In an SRAM design, a read and write margins must be both guaranteed at all process corners. Although the 6T memory cell shown in Fig. 1(a) has been widely used so far, it is difficult to ensure the both read and write margins without an area penalty. Large channel width (W) of the access transistors (Na1 and Na2) is effective to expand the write margin without write performance degraded, while the read margin is improved by large W of the drive transistors (Nd1 and Nd2) or large β ratio (W ratio of the driver transistor to the access transistor).

On the other hand, an 8T memory cell shown in Fig. 1(b) has a separated read port comprised of two transistors (Na3 and Nd3). Hence, there is some area overhead compared with the 6T cell when the read port is merely appended. As depicted in the figure, the area of the 8T cell is 1.3 times larger than that of the conventional 6T cell in a 90-nm node. However, note that we can lower the drive transistor's W in the 8T cell, because the read margin does not need to be considered thanks to the separate read port.

A design rule and channel length (L) are scaled down as a process technology is advanced, but they worsen Vth variation (random variation) and the operating margins. Fig. 2 shows the memory-cell area comparison when the operating voltage is 1.0 V and 0.8 V that is a lower voltage. The Vth variation of 6σ is considered. In the comparison, we assume that the nominal Vth is the same among the process nodes, and the minimum W and L are scaled by 0.7 time per generation. In the 6T cell, the drive-NMOS's W cannot be scaled down while that in the 8T cell can. At the 45-nm node, the lines intersect if the operating voltage is 1.0 V, and the area of the 8T cell becomes smaller at the 32-nm node. If the operating voltage is 0.8 V, the 6T-cell area cannot be shrunk and is saturated due to the large W of the drive transistors. The 8T cell is superior to the 6T cell in terms of area in the future process even if it is used as a single-port SRAM.

Voltage-Control Scheme for 8T cell

A voltage-control scheme is applied to the 8T memory cell in order to lower the minimum operating voltage, considering DVS environment where a variable supply voltage (Va) and the maximum voltage (Vmax) are available [1]. The memory-cell voltage (VDD in Fig. 1) is set to Va although a write-WL (WWL) voltage is always set to the Vmax when asserted, which expands the write margin as illustrated in Fig. 3. The proposed voltage-control scheme makes a larger write margin as Va is lowered. In addition to the write-margin improvement, we can reduce the area of the 8T cell when Va is less than Vmax (DVS environment), because we can make the drive NMOSes (Nd1 and Nd2) smaller than that at the 1.0 V. See the part of the 8T w/ VC in the 0.8V operation in Fig. 2.

As well as the WWL voltage, the read-WL (RWL) voltage is always set to Vmax in order to improve a read current at a low operating voltage. As shown in Fig. 4, even if the "0"-readout current (Iread0) is degraded and the "1"-readout current (Iread1) is increased by Vth variation, the Iread0 should be larger than the Iread1 in order to distinguish between "0" and "1". The high RWL voltage improves the minimum operating voltage from 0.54 V to 0.46 V thanks to the voltage-control scheme.

Write-Back Scheme

If a single-WL structure unlike the divided WL [2] was utilized, stored data in half-selected cells (half-select means that a WWL is asserted but a WBL and WBL_N remain uncertain) would be destroyed in a write operation because of the high WWL voltage and low WBL/WBL_N voltage [3]. To solve this issue, we implement a write-back scheme to the 8T SRAM. Fig. 5 is the waveforms in the write cycle. While CLK is "H", the RWL is activated even in the write cycle and stored data in all selected cells are read out to the D-latches. After CLK is switched to "L", Dataout is written back to the half-selected cell by using the MUX.

Results and Summary

We designed a 90-nm 64-kb 8T-SRAM test chip with the voltage-control and write-back schemes as shown in Fig. 6. The area overhead of the proposed SRAM is 8.5%, which is caused by the write-back MUX and RWL/WWL level shifters that amplify the WL voltages from Va to Vmax.

Fig. 7 exhibits the bit-error-rate (BER) improvement by the voltage-control scheme at the 90-nm node. The proposed scheme improves the minimum operating voltage from 0.64 V (restricted by the write margin in the conventional scheme) to 0.42 V, in a 64-Mb SRAM. In other words, the proposed 8T SRAM achieves both the small area and low-power operation in the future process, which is suitable for DVS systems.

Acknowledgments

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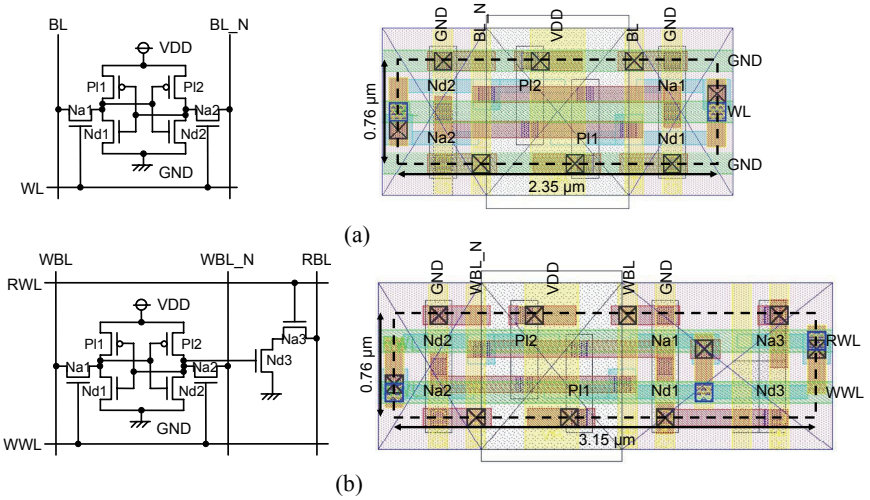
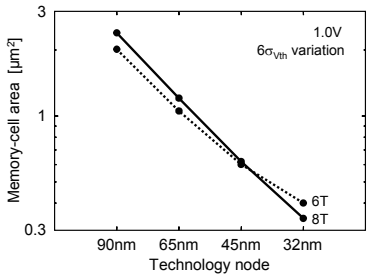
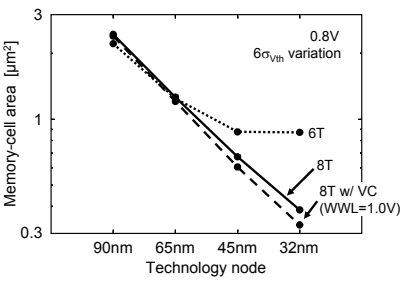


Fig. 1. Schematics and layouts of (a) 6T and (b) 8T cells designed with a 90-nm logic rule.



1.0V			90nm	65nm	45nm	32nm
6T	Tr. width [µm]	Access-NMOS	0.20	0.14	0.13	0.13
		Drive-NMOS	0.50	0.42	0.46	0.63
	β ratio		2.50	3.00	3.54	4.85
	Tr. length [µm]		0.10	0.07	0.05	0.035
	Cell area [µm²]		2.01	1.05	0.60	0.40
8T	Tr. width [µm]	Access-NMOS	0.20	0.14	0.13	0.13
		Drive-NMOS	0.20	0.14	0.10	0.07
	β ratio		1.00	1.00	0.77	0.54
	Tr. length [µm]		0.10	0.07	0.05	0.035
	Cell area [µm²]		2.39	1.20	0.62	**0.34**



0.8V			90nm	65nm	45nm	32nm
6T	Tr. width [µm]	Access-NMOS	0.24	0.21	0.22	0.24
		Drive-NMOS	0.72	0.70	1.09	2.26
	β ratio		3.00	3.33	4.95	9.41
	Tr. length [µm]		0.10	0.07	0.05	0.035
	Cell area [µm²]		2.21	1.24	0.87	0.87
8T	Tr. width [µm]	Access-NMOS	0.24	0.21	0.22	0.24
		Drive-NMOS	0.20	0.14	0.10	0.07
	β ratio		0.83	0.67	0.45	0.29
	Tr. length [µm]		0.10	0.07	0.05	0.035
	Cell area [µm²]		2.44	1.26	**0.67**	**0.38**
8T w/ VC	Tr. width [µm]	Access-NMOS	0.20	0.14	0.10	0.10
		Drive-NMOS	0.20	0.14	0.10	0.07
	β ratio		1.00	1.00	1.00	0.70
	Tr. length [µm]		0.10	0.07	0.05	0.035
	Cell area [µm²]		2.39	**1.20**	**0.60**	**0.33**

Fig. 2. Area comparison between 6T and 8T memory cells in a 1.0V and 0.8V operations.

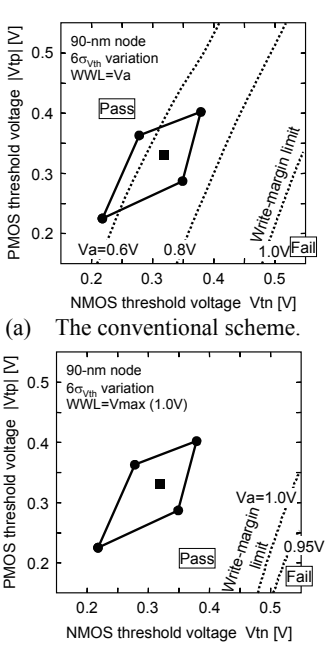


Fig. 3. Write-margin improvement by the proposed voltage-control scheme.

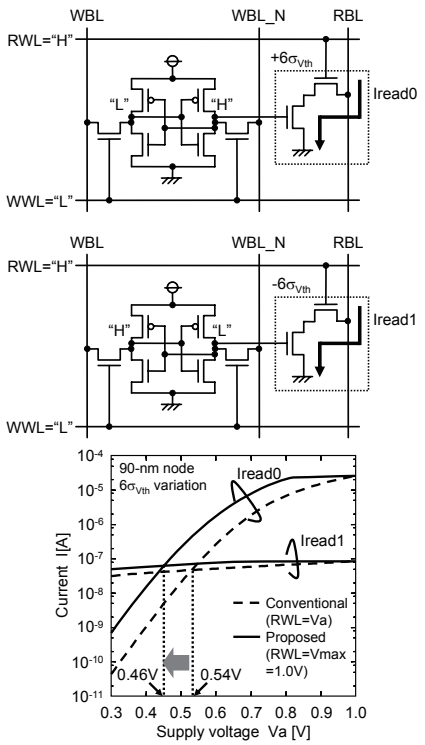


Fig. 4. Read-current improvement by the proposed voltage-control scheme.

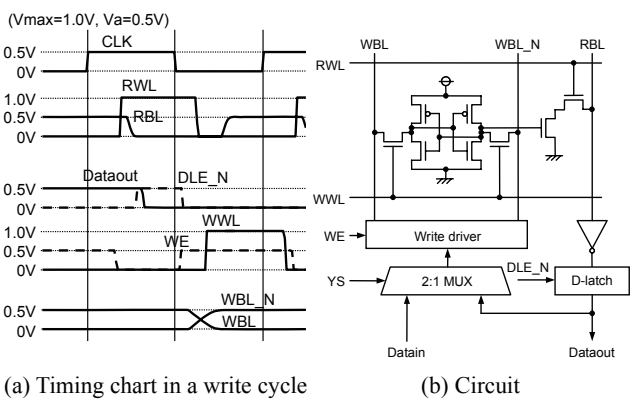


Fig. 5. Write-back scheme.

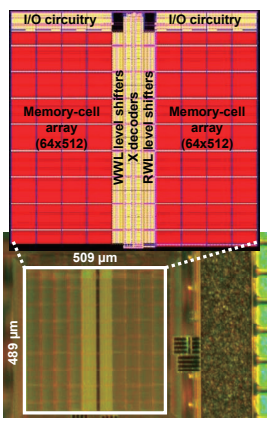


Fig. 6. A micrograph of the test chip and its layout.

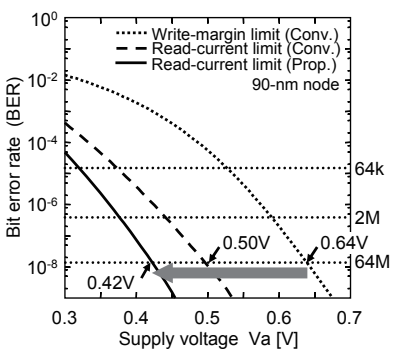


Fig. 7. BER improvement by the voltage-control scheme.