A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Clock Power Reduction

Hiroshi Kawaguchi and Takayasu Sakurai

Institute of Industrial Science, University of Tokyo
7-22-1, Roppongi, Minato-ku, Tokyo, 106 Japan
E-mail: kawapy@cc.iis.u-tokyo.ac.jp and tsakurai@iis.u-tokyo.ac.jp

Abstract

A Reduced Clock-Swing Flip-Flop (RCSFF) is proposed, which can reduce the clocking system power of an VLSI down to 1/3 compared to the conventional F/F. The area and the delay of the RCSFF can also be reduced by a factor of about 20%.

Introduction

In recent VLSI's, a clocking system, including clock interconnections and Flip-Flops,(F/F), consumes 20% to 45% of the total chip power[1]. This is partially because the activation ratio of a clock system is unity. In this clocking system power, 90% is consumed by the last branches of the clock distribution network which drive directly F/Fs and the F/Fs themselves. In order to achieve low-power VLSI's, it is important to reduce the clocking system power.

One idea is to reduce clock voltage swing, which was pursued by Ref. [4] but it required four clock lines, which will increase clock interconnection capacitance. Moreover, routing four clock lines is disadvantageous in area and the phase adjustment is difficult.

This paper describes a new small-swing clocking scheme which requires only one reduce-swing clock line.

Description of RCSFF

Figure 1 shows circuit diagrams of the RCSFF and the conventional F/F. The RCSFF is composed of a current-latch sense amplifier and cross-coupled NAND gates which act as a slave latch[2,3]. The salient feature of the RCSFF is to accept a reduced voltage swing clock. The voltage swing, Vclk, can be as low as 1V. By lowering the clock swing, the power of the clock distribution network is decreased as proportional to either $Vclk^1$ or $Vclk^2$, depending on the clock driver configuration shown in Fig. 2. When a clock driver Type A is used, power improvement is proportional to $Vclk^1$, while it is $Vclk^2$ if Type B driver is used. Type A is easy to implement but less efficient. Type B needs either an external Vclk supply or a DC-DC converter. Typical operation waveforms with Type A1 clock driver are shown in Fig. 3.

Only three MOSFET's, P1, P2 and N1 are clocked, which is beneficial to decrease capacitance of a clock network. P1 and P2 can be small because they may precharge slowly while the clock is low.

The issue of the RCSFF is that when a clock is high to Vclk, P1 and P2 do not switch off completely, leaving leak current flowing through either P1 or P2. The power consumption by this leak current turns out to be permissible for some cases (see next section), further power improvement is possible by reducing the leak current. One way is to apply backgate bias to P1 and P2 and increase the threshold voltage, which is studied in this paper. The other way is to increase the Vth of P1 and P2 by ion-implant, which needs process modification and is usually prohibitive. Thus this case has not been considered here.

When the clock is to be stopped, it should be stopped at V_{SS}. Then there is no leak current.

Performance comparison

A. Area

Transistor count of the RCSFF is 20 including an inverter for generating $\bar{D}$, while that of the conventional F/F is 24. The area of the RCSFF is 16% smaller than the conventional F/F as seen from Fig. 4 even when the well for the precharge PMOS is separated.

B. Delay

SPICE analysis is carried out assuming typical parameters of a generic 0.5μm double metal CMOS process. Figure 5 shows Clock-to-Q delay simulation results. The delay depends on Wclk (Wclk is defined in Fig.1). Since delay improvement is saturated at Wclk = 10μm, this value of Wclk is used in the area and power estimation. Clock-to-Q delay is improved by a factor of 20% over the conventional F/F even when Vclk = 2.2V, which can be easily realized by a clock driver of the Type A1.

Data setup time and hold time in reference to clock are 0.04ns and 0ns, respectively being independent from Vclk, compared to 0.1ns and 0ns for the conventional F/F.

C. Power

Simulated power consumption of the RCSFF is shown in Fig. 6. The power in the figure includes clock system power per F/F and the power of a F/F itself. The power consumption is reduced to about 1/2~1/3 compared to the conventional F/F depending on the type of the clock driver and V_{WELL}. In the best case studied here, 63% power reduction is observed. TABLE 1 summarizes typical performance improvement.

Application to reduced swing bus

For the RCSFF, the D and $\bar{D}$ input can also be small voltage swing signals. Using this characteristics, the RCSFF can be used to speed up RC delay of long buses. By placing the RCSFF at the end of a long bus and by sense-amplifying the slowly changing D input, RC delay can be reduced to 1/3 compared to the conventional F/F case (see Fig.7).

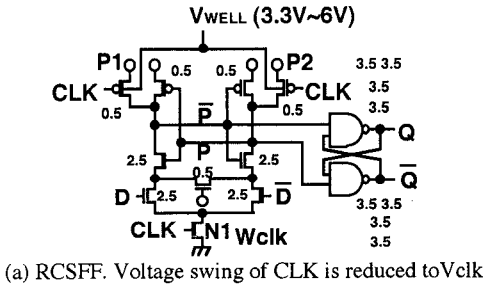
References

[1] T.Sakurai & K.Kuroda, "Low-Power Circuit Design for Multimedia CMOS VLSI's," SASIMI, pp.3-10, Nov. 1996.

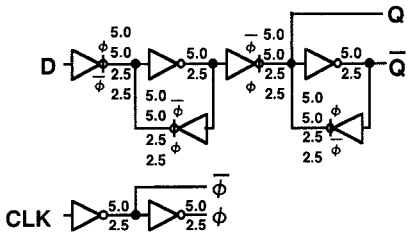
[2] M.Matsui et al., "200MHz Video Compression Macrocells Using Low-Swing Differential Logic," ISSCC, pp.76-77, Feb., 1994.

[3] J.Montanaro et al., "A 160-Mhz, 32-b, 0 5-W CMOS RISC Microprocessor," JSSC, vol. 31, pp. 1703-1714, Nov. 1996.

[4] H.Kojima et al., "Half-Swing Clocking Scheme for 75% Power Saving in Clocking Circuitry," VLSI Symp., pp.23-24, June 1994.



(a) RCSFF. Voltage swing of CLK is reduced toVclk



(b) Conventional F/F

Fig. 1 Circuit diagram of (a) the Reduced Clock Swing Flip-Flop (RCSFF) and (b) the conventional F/F. Numbers in the figure signify MOSFET gate width. Wclk is the gate width of N1

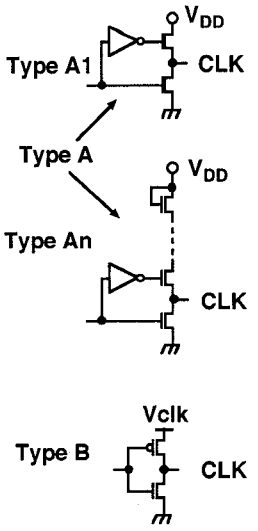
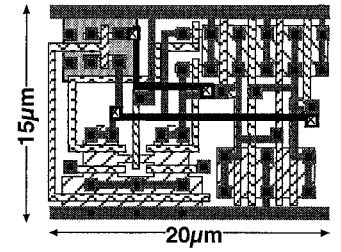
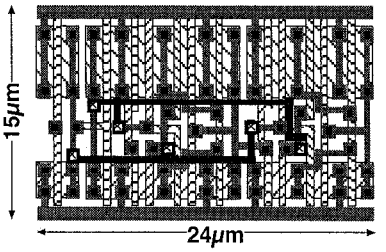


Fig. 2 Types of clock drivers. Type A1 and Type An are grouped as Type A. In Type B, Vclk is supplied by externally.



(a) RCSFF (N-well for P1 & P2 separated)



(b) Conventional F/F

Fig. 4 Layout of (a) the Reduced Clock Swing Flip-Flop (RCSFF) with Wclk being 10μm and (b) the conventional F/F.

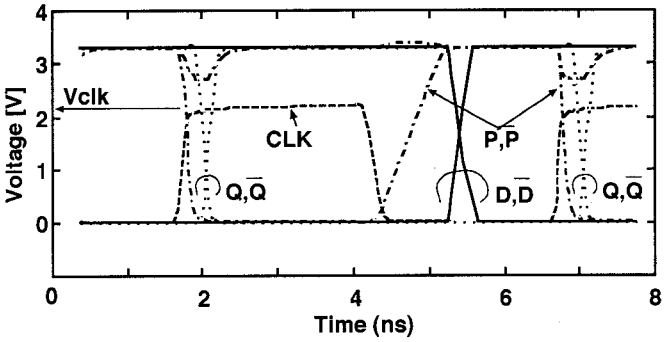


Fig 3. Operational waveforms of the RCSFF.

TABLE I Performance comparison of RCSFF and Conventional F/F

	Driver	Vclk[V]	Power	Delay	Area
Conventional		3.3	100%	100%	100%
RCSFF	Type A1	2.2	59%	82%	83%
V_{well}=6.6V	Type A2	1.3	48%	123%	83%
W_{clk}=10μm	Type B	2.2	48%	82%	83%
$f$clk=100MHz	Type B	1.3	37%	123%	83%

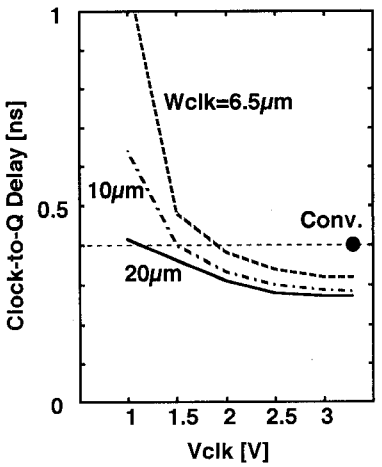


Fig. 5 Clock-to-Q delay dependence on Vclk. The delay is dependent on Wclk. See Fig.1 for explanation of Wclk.

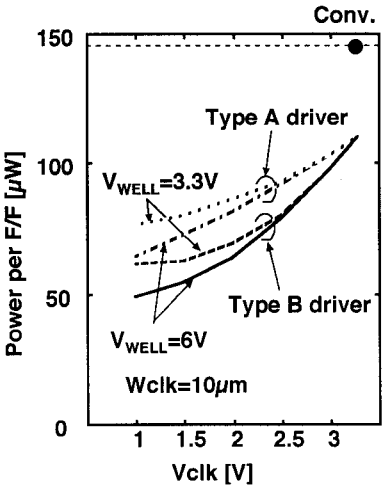


Fig 6. Power consumption for one F/F. Clock interconnection length per one F/F is assumed to be 200μm and data activation ratio is assumed to be 30%. $f$clk is 100MHz. By applying 6V well bias, the initial Vth of P1 and P2 (0.6 V) increases to 1.4V.

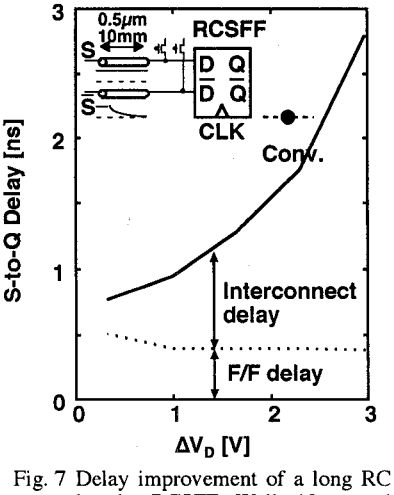


Fig. 7 Delay improvement of a long RC bus by RCSFF. Wclk=10μm and Type A1 clock driver is used. Bus is differential and precharged to VDD first and then CLK is asserted when the voltage difference of D and $\overline{D}$ becomes ΔVD.