Dynamic Leakage Cut-off Scheme for Low-Voltage SRAM's

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Introduction

The operation voltage of VLSI's is ever decreasing due to the strong needs for low-power consumption. In order to achieve low-voltage, high-speed operation, CMOS process tends to be optimized for low-voltage operation using thinner gate oxide and shorter effective channel length [1]. The low-voltage operation is also important in the future VLSI's, where scaled MOSFET's can be operated only in low V_{DD} environments with sufficient reliability.

Low-voltage, SRAM schemes have been proposed including source voltage driving [2] and dynamic boost of the supply voltage and word line [3]. However, in these schemes the gate voltage of MOSFET's go up to over 1.4V even though the V_{DD} is 0.8V, which give rise to reliability issues in cases.

In this paper, a sub-volt SRAM circuit scheme is presented which speeds up the conventional low-voltage SRAM by more than a factor of two without applying excessive voltage to gate oxide and with maintaining the subthreshold leakage current in a tolerable level.

Dynamic Leakage Cut-off Scheme

Figure 1 shows the proposed dynamic leakage cut-off (DLC) SRAM with operation waveforms. The salient feature of the scheme is that n- and p-well bias voltage are dynamically changed to V_{DD} and V_{SS} respectively for selected memory cells, while the well bias of the non-selected memory cells are kept V_{NWELL} (~ $2V_{DD}$) and V_{PWELL} (~ $-V_{DD}$). By doing so, the threshold voltage of the selected memory cells becomes relatively low and assures high drive current which in turn realizes fast operation. On the other hand, the threshold voltage of dormant memory cells is relatively high which achieves low subthreshold leakage.

This scheme is different from the Variable Threshold CMOS scheme (VTCMOS [4]), in that the well bias is synchronized with a word line signal in the DLC and not with a standby signal. It should be noted that a triple-well process technology is required to realize the DLC SRAM but the triple-well process is preferable for system LSI's where analog and memories are embedded in logic environments and electrical isolation is an issue.

Figure 2 shows a well bias driver circuit for n-well and the corresponding V_{GS}-V_{GD} trajectories of all MOSFET's in dynamic operation. It is seen from the figure that each MOSFET in the circuit does not feel voltage over V_{DD} across the gate oxide, which assures sufficient reliability. The absolute value of the well bias can be about V_{DD} without junction breakdown and reliability problem.

Design Considerations

Figure 3 and 4 show simulated delay and leakage characteristics of 1Mbit low-voltage SRAM in 0.35µm technology. V_{TH} of 0V is desirable from the delay point of view. The total subthreshold leak current of the dormant memory cells, I_{LEAK}, however, goes up to 200mA which should be compared with the active circuit current of 5mA at 100MHz. The subthreshold leakage current is dominant in SRAM's even in an active mode, since most of the memory cells are inactive. If more than 1Mbit is needed, the situation gets worse.

By using the DLC scheme, the V_{TH} can be shifted 0.14V at V_{DD} of 0.5V and 0.25V at V_{DD} of 1V. Hence, the bit line delay can be reduced by a factor of 2.5 in 0.5V V_{DD}.

The memory cell area overhead of the DLC scheme is 27% as is shown in Fig.5. Other than the memory cell, the DLC scheme has area overhead for well drivers. The overall area overhead is from 20% to 50% which is a function of the number of selected memory cells (Fig.6). The overhead can be reduced through the introduction of deep trench isolation by 10%.

The DLC SRAM can be built with an SOI technology. Compared with the dynamic threshold MOS (DTMOS) scheme where a gate and a body are tied and the body bias change is limited to 0.7V due to the forward bias of a junction, the DLC SRAM can allow more change in body voltage, for example 2V, resulting in the larger shift in V_{TH}, which in turn realizes higher speed with the same leakage current.

Measurement Results

Figure 7 shows a microphotograph of the chip fabricated with 0.35µm CMOS process. The threshold voltages for PMOS and NMOS are both 0.15V. Those values are not ideal from the speed and leakage point of view but we have carried out an important measurement which can not be simulated by a circuit simulator, that is, a disturb test. In the DLC SRAM, the well bias voltage is dynamically changed and an unexpected flip of the SRAM cell may occur. Figure 8 shows the results. No abnormal flip of memory cells was observed in the V_{DD} range from 0.5V through 1V and the well pulse height range from 0.5V through 2V.

Acknowledgments

Research support including chip fabrication from Toshiba and useful discussions with T.Kuroda and T.Furuyama are to be acknowledged.

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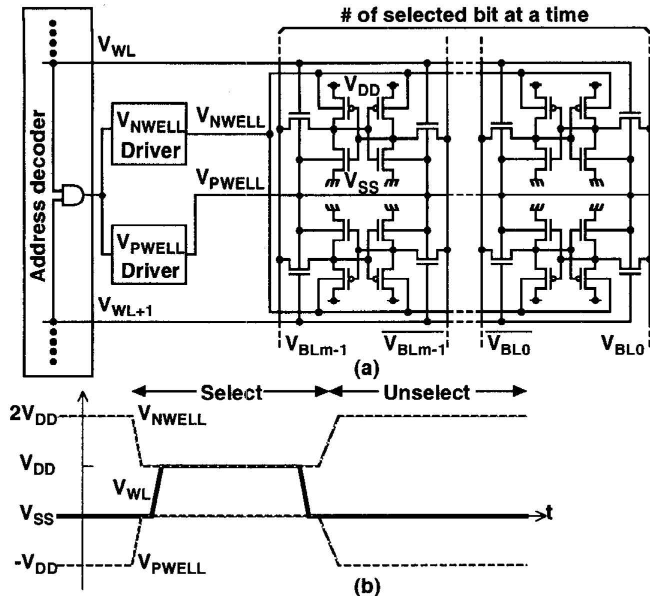


Fig. 1 (a) Circuit schematic of Dynamic Leakage Cut-off (DLC) SRAM, and (b) Operation waveforms

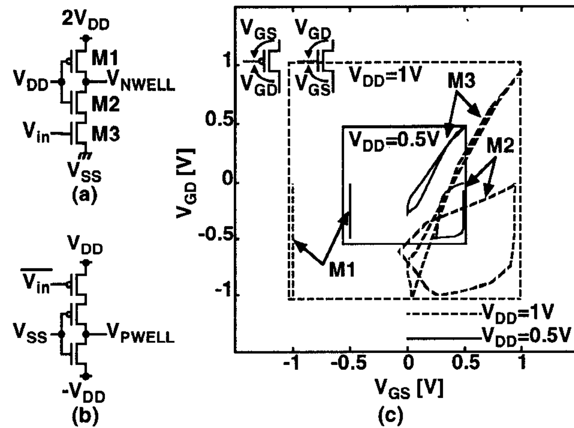


Fig. 2 (a) Well bias driver for N-well, (b) Well bias driver for P-well, (c) VGS-VGD trajectories of (a). No trajectories go beyond V_{DD}.

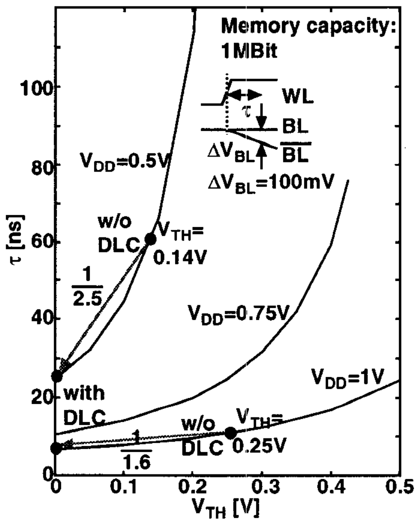


Fig. 3 Bit line delay characteristics of DLC SRAM

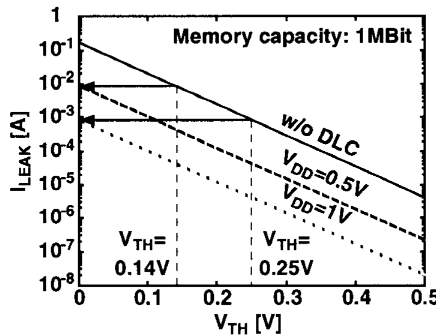


Fig. 4 Total subthreshold leak of 1Mbit SRAM. At 1V VDD, VTH of the dormant cell is 0.25V while that of the active cell is 0V, keeping the total leakage power at 0.9mW.

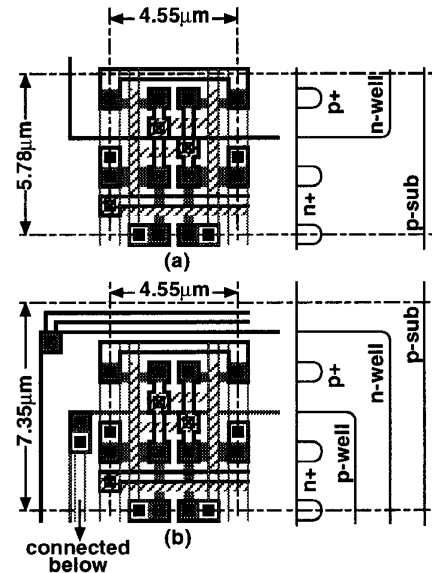


Fig. 5 (a) Layout of conventional memory cell
(b) Layout of DLC memory cell

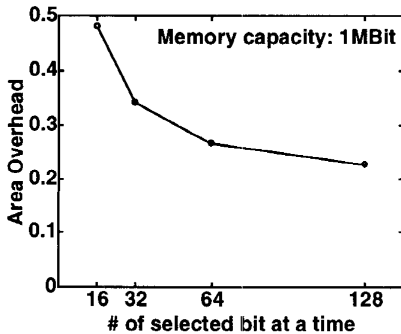


Fig. 6 Area overhead of DLC SRAM. Memory cell area occupancy is assumed to be 70% in the conventional SRAM.

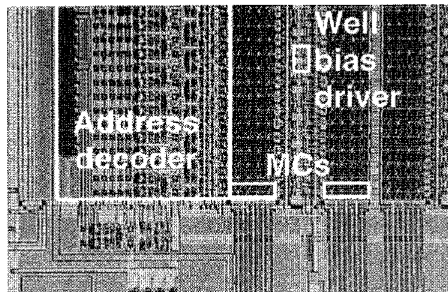
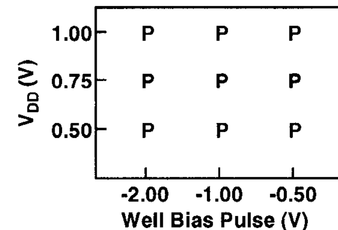


Fig. 7 Microphotograph of the fabricated chip. MCs signifies memory cells.



V_{DD} (V)	-2.00	-1.00	-0.50
1.00	P	P	P
0.75	P	P	P
0.50	P	P	P

Fig. 8 Disturb test results. Well bias pulse frequency is 100MHz. P means 'pass'.