A Wearable Healthcare System with a 13.7 μA Noise Tolerant ECG Processor

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***Abstract*— To prevent lifestyle diseases, wearable bio-signal monitoring systems for daily life monitoring have attracted attention. Wearable systems have strict size and weight constraints, which impose significant limitations of the battery capacity and the signal-to-noise ratio of bio-signals. This report describes an electrocardiograph (ECG) processor for use with a wearable healthcare system. It comprises an analog front end, a 12-bit ADC, a robust Instantaneous Heart Rate (IHR) monitor, a 32-bit Cortex-M0 core, and 64 Kbyte Ferroelectric Random Access Memory (FeRAM). The IHR monitor uses a short-term autocorrelation (STAC) algorithm to improve the heart-rate detection accuracy despite its use in noisy conditions. The ECG processor chip consumes 13.7 μA for heart rate logging application.**

***Index Terms*— Biomedical signal processing, Electrocardiography, Heart rate extraction, Microcontrollers, Mobile healthcare, Wearable sensors**

I. Introduction

BECAUSE of the advent of an aging society, mobile health plays an ever more prominent role [1]. Daily-life monitoring is especially important in preventing lifestyle diseases, which have rapidly increased the number of patients and elderly people requiring nursing care. Our goal is the monitoring and display of vital signals and physical activity in daily life to improve users' quality of life and realize a smart society.

We propose an Instantaneous Heart Rate (IHR) monitoring and electrocardiograph (ECG) processor for use in a wearable healthcare system. The IHR is an important bio-signal used for heart disease detection, heart rate variation analysis [2], and exercise intensity estimation [3].

Key factors affecting wearable system usability are miniaturization and weight reduction. However, a wearable ECG monitor is sensitive to extraneous noise because its electrodes are close together. The SNR of ECG signals will be especially degraded if a user is not at rest. Consequently, a sophisticated and costly analog front end is usually required. However, the feature and purpose of our approach is digital signal processing to reduce the performance requirements of the analog portion and to minimize the overall system power consumption. The battery weight is a dominant characteristic of the wearable system. Therefore, the battery capacity and power consumption must be limited as much as possible.

II. System Description and Architecture

Fig. 1 presents an overview of the wearable healthcare system, comprising the proposed ECG processor, Near Field Communication (NFC) tag IC, and accelerometer IC. The NFC is used for program loading, individual optimization, and logging data transfer from the ECG processor. Compared with Bluetooth Low Energy or ZigBee, the standby power of NFC is extremely small. The active communication energy is also consumed by a reader/writer side when using a passive NFC tag.

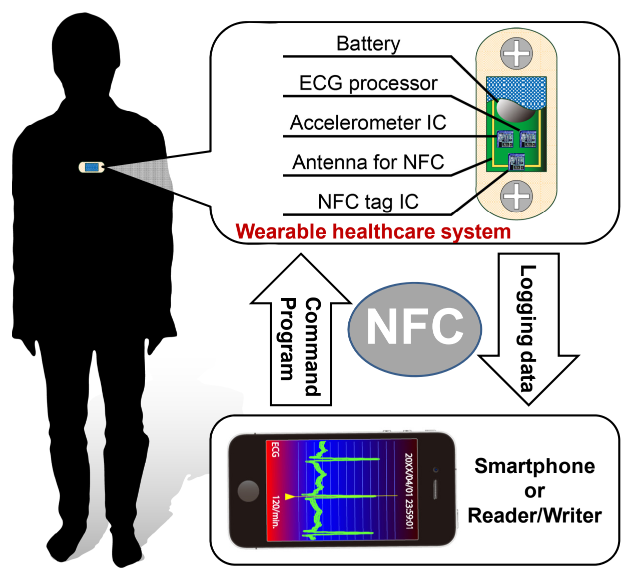

Fig. 1. Wearable healthcare system overview.

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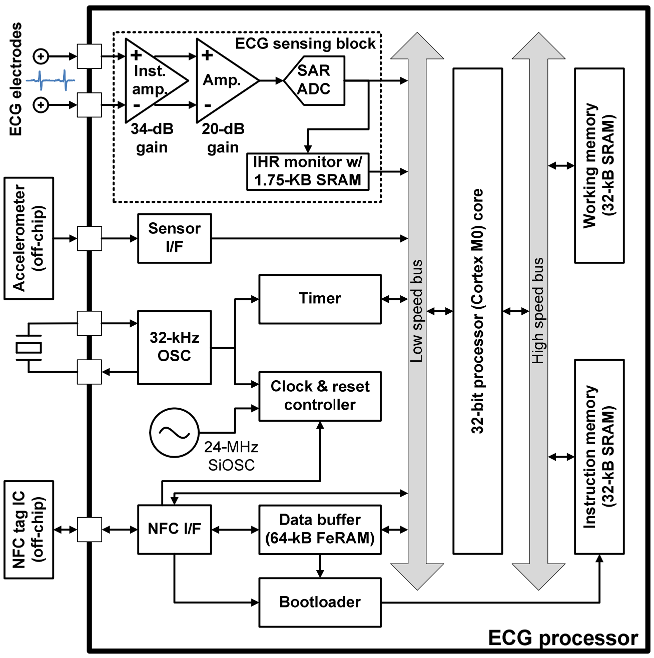


Fig. 2. Block diagram of ECG processor.

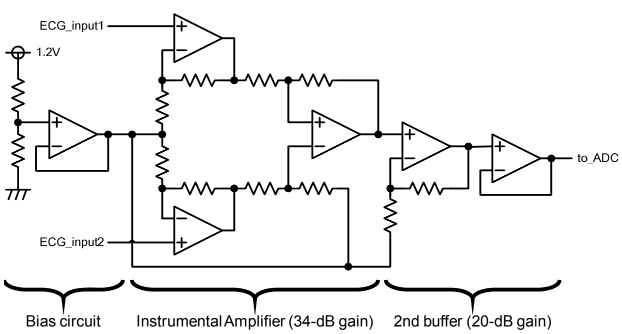


Fig. 3. Analog front-end circuits of ECG sensing block.

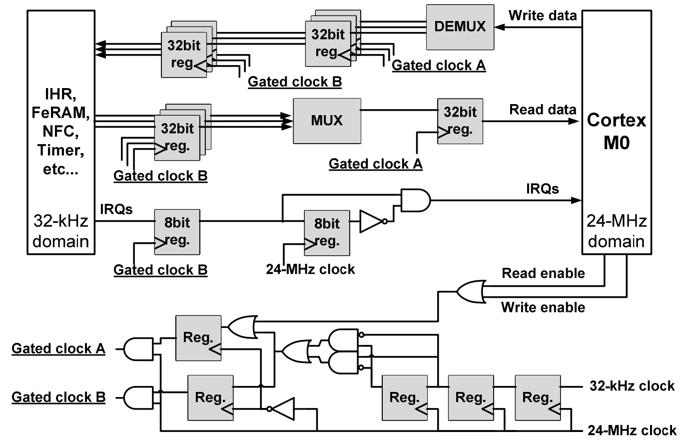


Fig. 4. Low speed bus and clock gating scheme for asynchronous clocks.

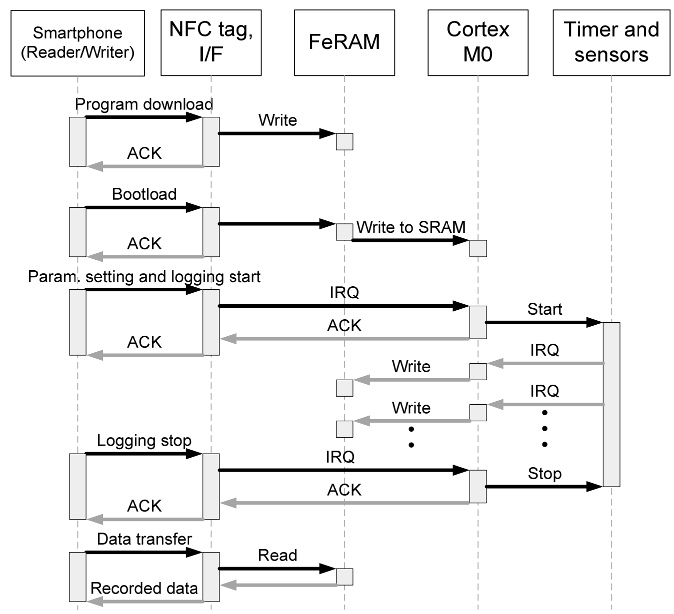


Fig. 5. Operation sequences of proposed sensor.

Therefore, the proposed system uses NFC to cooperate with a Smartphone (or reader/writer).

Fig. 2 presents a block diagram showing the proposed ECG processor, which consists of an ECG sensing block, Ferroelectric Random Access Memory (FeRAM), 32-bit Coretex-M0 core, and extra interfaces. Because the frequency range of vital signals is low (less than 1 kHz), both the standby power reduction and sleep time maximization are important to minimize the total power consumption. The 64-Kbyte FeRAM is integrated as a data buffer for daily life monitoring because the leakage current of the data buffer is dominant in the standby state.

The ECG sensing block has an analog front end (AFE), a 12-bit SAR ADC, and a robust IHR monitor. Although the IHR monitor using high-order eight-bit data of the ADC, 12-bit ADC output also directly connected to Cortex M0. The AFE includes a 34-dB gain instrumental amplifier and a 20-dB gain amplifier as shown in Fig. 3. The ADC sampling rate can be set to 1 kSamples/s for ECG processing mode and 128 Samples/s for IHR monitoring mode. The robust IHR monitor is the main contribution of this study.

The operating frequency of the Cortex M0 core, which is used for an on-node vital signal processing, is 24 MHz, whereas the operating frequency of other digital blocks is 32 kHz. The slow signals in the 32-kHz domain are synchronized at the low-speed bus to the 24-MHz domain as shown in Fig. 4. To minimize the power consumption of registers in the low-speed bus, the 24-MHz clock is gated using bus control signals. When the Cortex M0 core is in a deep sleep state, the on-chip 24-MHz oscillator is also stopped.

Fig. 5 shows the sequence diagram of the proposed system for the data logging application. When the system starts, only the 32-kHz real time clock and NFC interface circuits for RF signal detection are activated. If the NFC reader/writer starts communication in the transmission range, then the NFC interface and sequencer of the ECG processor are kicked by the NFC tag IC.

First, a program binary for the Cortex M0 is transferred from the reader/writer side. Then the program is stored directly in FeRAM. When the ECG processor receives the "bootloading" packet, the program is transferred from FeRAM to instruction SRAM. The program will be running. Before starting a data logging service or any other service, the NFC reader/writer communicates with Cortex M0 core for parameter

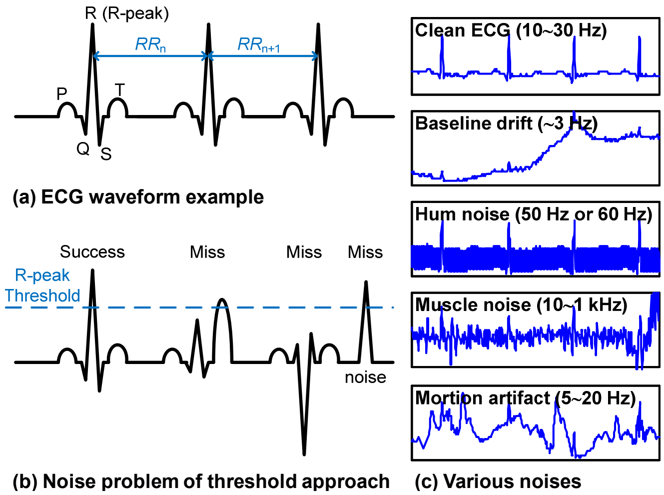


Fig. 6. Threshold based R-wave detection and its noise problems in wearable healthcare systems.

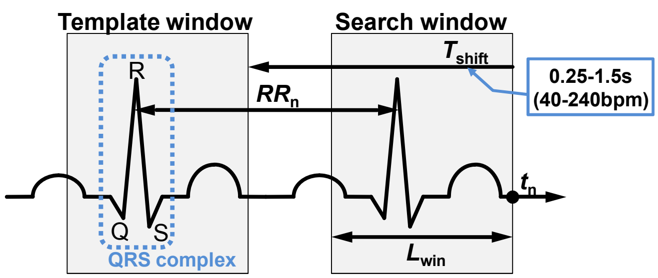


Fig. 7. IHR extraction with short-term autocorrelation (STAC).

configuration, time synchronization, and checking results of the self-test. When a packet to Cortex M0 core is received, the core is awakened by an interrupt request (IRQ) because it is normally in a deep sleep state. The payload of the received packet is accessible through the data bus. A "logging start" packet and a "logging stop" packet use the same procedure.

During the data logging operation, a timer circuit periodically wakes up the Cortex M0 core using the IRQ. Then the measured or calculated data are stored to FeRAM through the data bus. Therefore, the FeRAM is used both as a program ROM and a data buffer. The logging data in the FeRAM can be read out directly by the NFC interface circuit without the Cortex M0 core.

All application layer functions are defined using the payload in the transport protocol frame of NFC.

III. Robust Instantaneous Heart Rate Monitor

Ultra-low-power ADCs, which have sub-μW power consumption and a limited sample rate, have been developed for biomedical applications [4]. Furthermore, according to Moore's law, the power of digital components increases with the progress of process technology. However, the power consumption of analog circuits will not decrease similarly. Therefore, the features and purposes of our approach are the use of digital signal processing to reduce the performance requirements of analog components including electrode and to minimize the system's overall power consumption. In this work, a noise tolerant algorithm is implemented in dedicated hardware to achieve both noise tolerance and low-power consumption.

A. Heart rate extraction algorithms

Extracting R-waves (see Fig. 6(a)) with threshold determination is a general approach. Recently, various statistical approaches have been proposed for noise-tolerant threshold calculation.

The Pan–Tompkins (PT) algorithm [5] is most commonly used for beat detection. This algorithm uses band-pass filtering, differentiation, squaring, and moving window integration. The SQRS [6] and WQRS [7] algorithms can respectively detect QRS based on ECG slope and length transform. The SQRS uses band pass filtering for noise reduction, which uses only the integer coefficient. The WQRS also uses a low-pass filter to remove baseline wander. The Discrete Wavelet Transform (DWT) [8–10] uses a wavelet transform with quadratic spline wavelet (QSWT). The threshold is calculated using the root mean square value of the wavelet transform. This algorithm has been used in robust ECG monitoring LSIs [10–12]. The Quad Level Vector (QLV) algorithm [13] is implemented in dedicated hardware for ECG monitoring LSI [14, 15]. The QLV is generated using DWT and the adaptive threshold. Then, the threshold is determined by the maximum mean deviation (MD) of the previous heartbeats. The Continuous Wavelet Transform (CWT) algorithm [16–18] employs a Mexican hat wavelet in the frequency interval of 15–18 Hz. The R-peak can be extracted using the adaptive threshold, which is calculated using the modulus maxima of the CWT. This algorithm is also implemented in [15].

However, as depicted in Fig. 6, both misdetection and false detection are increased in the wearable healthcare system by noise from various sources such as myoelectric signals from muscle and electrode movement because the power consumption and electrode distance of the wearable sensor are strictly limited to reduce its size and weight.

Autocorrelation [19, 20] and template matching [21] are more robust approaches to prevent incorrect detection because these algorithms use the similarity of QRS complex waveforms and have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system [20]. However, the method necessitates numerous computations because it calculates the average heart-rate over a long duration (30 s). In our previous work, a short-term autocorrelation (STAC) technique was proposed for IHR detection [22].

Fig. 7 portrays IHR extraction using STAC. As depicted in Fig. 7 and (1–5), the IHR at time t_n (IHR_n) is obtained as a window shift length (T_{shift}) that maximizes the correlation coefficient between the template window and the search window (CC_n).

$$CC_n\left[T_{shift}\right] = w_1 \cdot \sum_{i=0}^{L_{win}-1} Q_w\left[t_n - i\right]\cdot Q_w\left[\left(t_n - T_{shift}\right) - i\right] \tag{1}$$

$$RR_n = \underset{0.25\times F_s \le T_{shift} \le 1.5\times F_s}{\arg_{T_{shift}} \max} \left\{CC_n\left[T_{shift}\right]\right\} \tag{2}$$

$$L_{win} = 1.5\times F_s \tag{3}$$

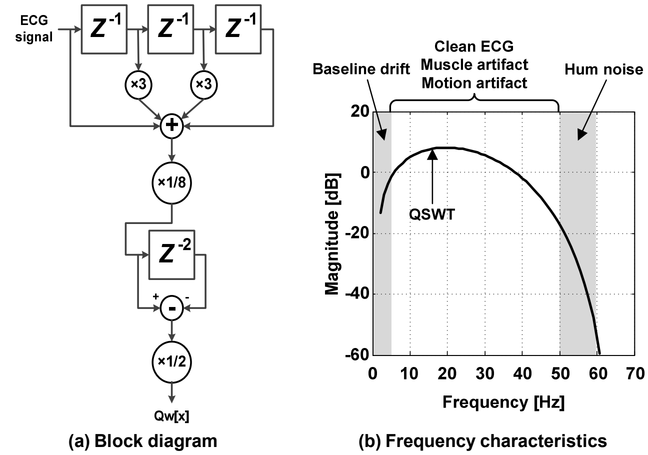


Fig. 8. Block diagram and frequency characteristics of QSWT.

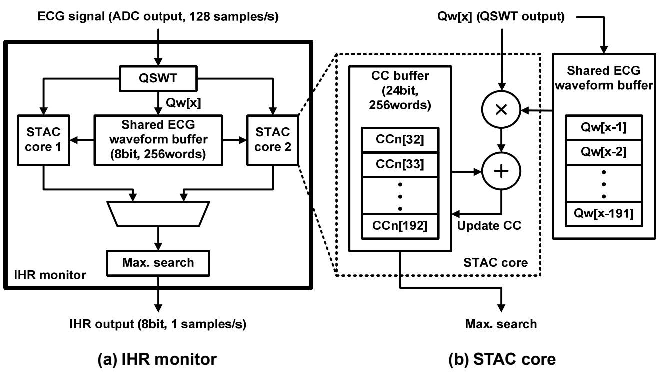


Fig. 9. Block diagram of robust IHR monitor.

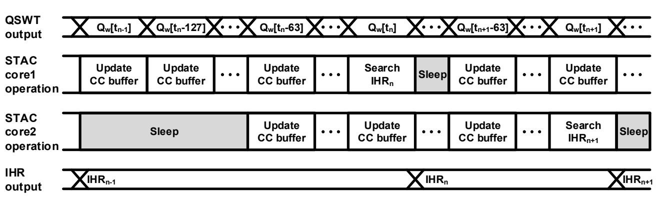


Fig. 10. Timing chart of IHR extraction.

$$w_1 = \begin{cases} 1 & \left(T_{\text{shift}} \le 0.546 \times F_s\right) \\ 0.75 & \left(0.546 \times F_s < T_{\text{shift}} \le 0.983 \times F_s\right) \\ 0.5 & \left(0.983 \times F_s < T_{\text{shift}}\right) \end{cases} \tag{4}$$

$$IHR_n = \frac{60}{RR_n} \tag{5}$$

In the equations presented above, F_s, L_{win}, and w_1 respectively denote the sampling rate (samples/s), the window length, and the weight coefficient. The value of T_{shift} is set as 0.25 s to 1.5 s because the heart rate of a healthy subject is 40 bpm to 240 bpm. The L_{win} is updated according to the estimated IHR to reduce the computational amount and to improve the IHR estimation accuracy. Then, the range of L_{win} and w_1 is determined by the maximum rate of the beat-to-beat variation, which is generally 20% in a healthy subject [23].

B. Hardware implementation of the heart rate monitor

In this work, we introduce a robust IHR monitor, which employs two-step noise reduction technique. In the first stage, the QSWT filter is used to mitigate the baseline wander and hum noise. Fig. 8 presents a block diagram and frequency characteristics of the QSWT with 128-Hz sampling rate. The QSWT requires few calculations and low hardware cost because it can be implemented using only adders and shift operators. The base-line wander and hum noise can be removed easily using QSWT. Unfortunately, it is difficult to remove the myoelectric noise and electrode motion artifacts only using QSWT because these frequency ranges are similar to the desired ECG signal.

Therefore, in the second stage, the IHR is extracted using the STAC method. The STAC is also implemented as dedicated hardware to minimize the power overhead. Fig. 9 presents the block diagram of the IHR monitor and STAC processing core. Each STAC core has CC buffer to store the intermediate value of $CC_n[T_{shift}]$ in (1). The CC buffer is updated in synchronization with ADC output (see Fig. 10). Since the L_{win} is 1.5 s and because IHR is updated every second, two STAC cores alternately calculate IHR with 0.5 s overlap.

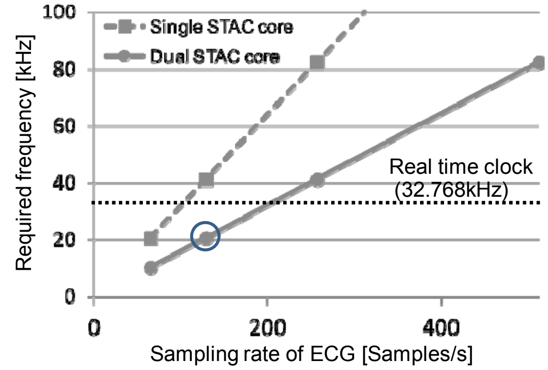


Fig. 11. Required operating frequency for real time IHR extraction.

The dual STAC core architecture also contributes to reduction of the operating frequency. Fig. 11 shows the required operating frequency to realize the real-time STAC calculation. Because the sampling rate target is set to 128 Samples/s in this study, the required frequency is lower than 32 kHz when applying dual core architecture. Therefore, this STAC hardware can operate only using 32.768-kHz real-time clocks. Note that the real-time clock, which has low power consumption, is a necessary component of a wearable monitoring system.

The gate level simulation result shows the IHR monitor block, which contains QSWT, two STAC cores, and SRAMs, consumes 1.21 μA in 130-nm CMOS process. The digital logic and SRAMs respectively consume 0.26 μA and 0.95 μA, which include 0.4-μA leakage current.

C. Performance evaluation of heart rate extraction

To evaluate the heart rate extraction algorithms, we implemented the conventional and our proposed algorithms, which combined STAC with QSWT filter, using MATLAB. First, we investigated the successful rate of heart rate extraction using 23 records from the MIT-BIH arrhythmia database [24]. Table I shows that no significant difference was found among the successful rates in clean waveforms, although they include arrhythmia.

TABLE I
PERFORMANCE COMPARISON OF IHR EXTRACTION SUCCESS RATE [%] WITH MIT-BIH ARRYTHMIA DATABASE [24]

Record #	PT	SQRS	WQRS	DWT	QLV	CWT	**Prop.**
100	99.9	99.8	99.8	99.9	99.9	99.8	99.9
101	99.8	99.7	99.3	99.7	99.4	99.6	99.7
102	99.9	99.9	99.9	99.8	98.2	99.7	99.8
103	100.0	99.9	99.9	100.0	99.9	100.0	99.8
104	95.6	96.5	95.5	97.0	95.3	92.2	99.5
105	70.7	94.1	92.8	95.2	93.5	98.0	97.7
106	84.6	89.7	96.4	95.2	87.9	93.4	96.7
107	96.8	99.3	94.8	99.6	94.6	99.1	97.8
108	86.9	80.9	84.7	74.1	70.5	99.1	98.5
109	99.6	98.1	99.4	99.6	99.6	99.6	99.0
111	99.3	99.4	99.8	97.4	17.0	99.8	99.7
112	99.9	99.7	99.8	99.4	99.9	100.0	99.2
113	99.8	99.4	97.2	99.8	99.6	99.6	99.9
114	99.8	99.7	99.3	99.9	99.6	99.8	98.4
115	99.9	99.5	99.1	99.7	99.7	99.8	99.9
116	95.4	98.6	98.1	99.6	98.3	99.2	95.6
117	100.0	99.9	99.9	99.7	99.1	100.0	99.9
118	99.9	97.9	99.1	99.7	96.2	99.4	99.2
119	99.8	98.5	96.1	95.9	99.1	97.4	96.8
121	99.9	99.4	99.7	99.2	91.1	99.9	99.8
122	100.0	99.9	99.9	99.9	97.2	100.0	99.8
123	100.0	99.2	98.6	99.7	99.4	99.4	99.6
124	98.4	99.4	99.3	99.5	96.7	98.2	99.7
average	96.8	97.8	97.8	97.8	92.7	98.8	99.0

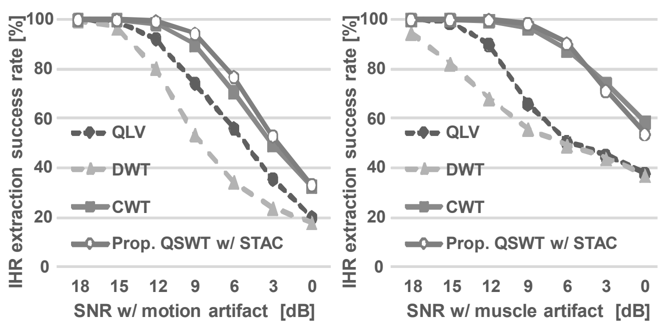


Fig. 12. Performance comparison of noise stress test using record #100 with muscle and motion artifact noises.

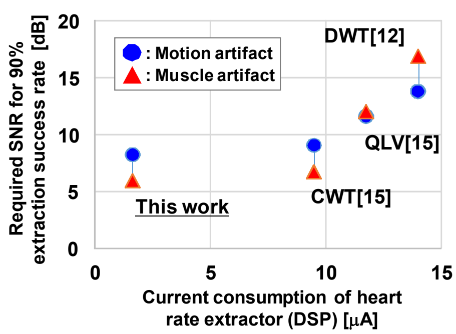


Fig. 13. Performance comparison of hardware implemented IHR monitors.

Next, we evaluated the noise tolerance using the MIT-BIH noise stress test database [25]. Fig. 12 shows the relation between the intensity of noise and the success rate of IHR detection. The MIT-BIH record #100 is used to evaluate the effect of noise contamination and to eliminate the effect of arrhythmia because this record contains a small number of arrhythmia beats. A muscle artifact and motion artifact records are used because these noises have critical frequency characteristics, as presented in Fig. 6. Then, the signal-to-noise ratio (SNR) is defined as shown below.

$$SNR = 10\log\frac{S}{N \times a^2} \tag{6}$$

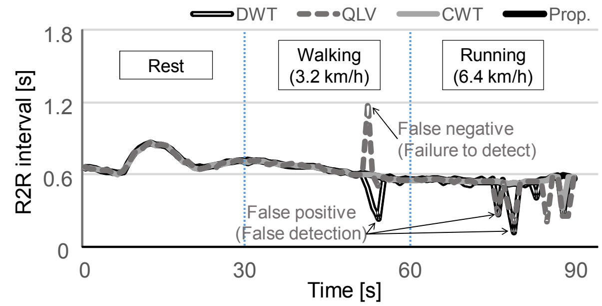


Fig. 14. Extracted IHR comparison example of subject #1 in rest, walking, and running condition using measured ADC output of proposed SoC.

TABLE II
PERFORMANCE COMPARISON OF IHR EXTRACTION SUCCESS RATE [%] WITH MEASURED DATA

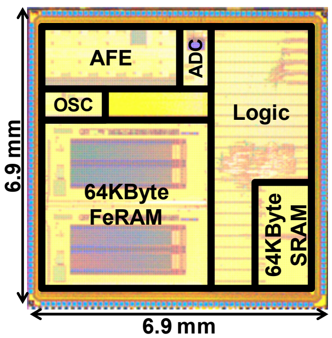
		DWT	QLV	CWT	Prop.
Subject #1	Rest	100.0	100.0	100.0	100.0
	Walking	90.0	96.7	100.0	100.0
	Running	83.3	80.0	96.7	100.0
	Total	91.1	92.2	98.9	100.0
Subject #2	Rest	100.0	100.0	100.0	100.0
	Walking	93.3	100.0	100.0	100.0
	Running	93.3	90.0	100.0	96.7
	Total	95.6	96.7	100.0	98.9
Subject #3	Rest	100.0	100.0	96.7	100.0
	Walking	96.7	96.7	96.7	100.0
	Running	96.7	93.3	96.7	100.0
	Total	97.8	96.7	96.7	100.0
Subject #4	Rest	100.0	100.0	100.0	100.0
	Walking	100.0	100.0	100.0	100.0
	Running	93.3	96.7	100.0	100.0
	Total	97.8	98.9	100.0	100.0
Subject #5	Rest	96.7	93.3	96.7	100.0
	Walking	100.0	93.3	96.7	96.7
	Running	96.7	90.0	96.7	96.7
	Total	97.8	92.2	96.7	97.8
Average	Rest	99.3	98.7	98.7	100.0
	Walking	96.0	97.3	98.7	99.3
	Running	92.7	90.0	98.0	98.7
	Total	96.0	95.3	98.4	99.3

Here, S, N, and a respectively denote the signal power, frequency-weighted noise power, and scale factor. Simulation results show that the proposed algorithm has better noise tolerance in each condition. As shown in Fig. 13, the proposed IHR monitor has higher noise tolerance and minimum current consumption compared with previous studies of hardware implemented heart rate extractor.

Finally, we evaluated the heart rate extraction success rate using the measured ADC output data of proposed SoC. To evaluate the noise tolerance, the ADC output data with the rest, walking, and running condition are used (see Fig. 14). The duration of each condition is 30s. Table II shows the performance comparison of heart rate extraction success rate with healthy five subjects, from 22 to 29 year-old man. As shown in Table II, the proposed method still has better performance in real data.

IV. Implementation Result

The test chip is fabricated using 130-nm CMOS technology. Fig. 15 presents a chip photograph and a performance summary. The operating voltage is 1.2 V for AFE, ADC, SRAM, 24-MHz oscillator, and digital blocks. The FeRAM, 32-KHz oscillator, and IO circuits are operated with 3.0 V supply voltage.



Technology		130-nm CMOS
Supply voltage		1.2V (Digital, SRAM, ADC, AFE)
		3.0V (FeRAM, 32kHz OSC, I/O)
Chip area		6.9 mm × 6.9 mm
Frequency		24 MHz (for MCU)
		32 kHz (for other blocks)
MCU		32-bit Cortex M0
On chip memory		64-KB FeRAM (for logging data)
		64-KB SRAM (for MCU)
		1.75-KB SRAM (for IHR monitor)
ADC	Resolution	12 bit (IHR monitor uses high-order 8-bit)
	Current	0.5 μA@128 S/s, 1.4 μA@1 kS/s
AFE	Gain	54 dB
	Bandwidth	0-100 Hz
	CMRR	73 dB
	Current	3.4 μA

Fig. 15. Chip photograph and chip specifications.

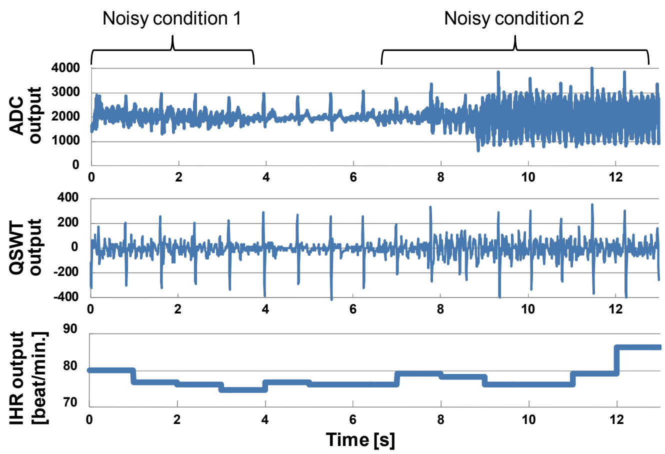


Fig. 16. Measured waveform of IHR monitor in a noisy condition.

To demonstrate the test chip performance, we implemented a heart rate logging application. In this experiment, an Android[TM] smartphone is used for program loading and logging data retrieval. As portrayed in Fig. 16, the IHR is extracted correctly in a noisy condition.

Fig. 17 portrays the current consumption with a heart rate logging application. In this experiment, the ADC sampling rate and the logging interval of IHR are set respectively to 128 Samples/s and 1 Sample/s. Then the AFE, 32-kHz OSC, and Timer block are always activated. The measurement results show that the test chip consumes 13.7 μA on average for the heart rate logging application. The peak current, which is consumed when the Cortex and FeRAM are activated to store the logging IHR data every second, is less than 1 mA.

As presented in Fig. 18, the IHR monitor and FeRAM respectively contribute to active ratio reduction and sleep power reduction. Table III presents a performance comparison of the ECG processor. Compared with earlier ECG processors [12, 26-28], the proposed processor has lower power and grater memory capacity for daily-life monitoring.

Fig. 19 portrays the application board of the proposed wearable sensor system. The board is 39.5 mm × 42.0 mm, with maximum thickness of 5 mm. The proposed system weighs 5.5 g including 1.0 g battery. We employed a 35mAh battery in this system. The total current consumption is less than 60 μA, which includes the Accelerometer IC, NFC tag IC, linear regulator, 32.768 kHz crystal oscillator, and the proposed ECG

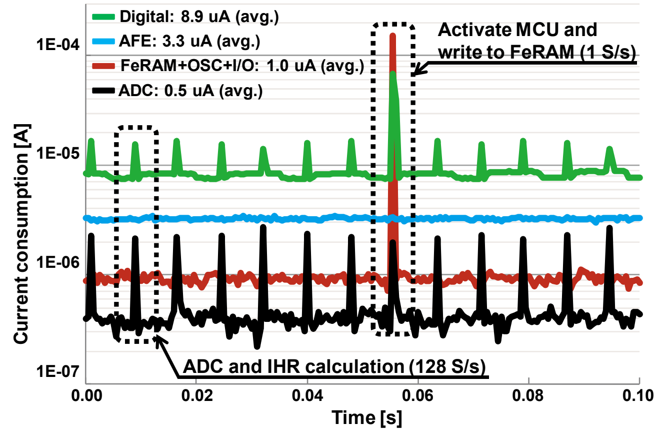


Fig. 17. Measurement result of current consumption with a heart rate logging application.

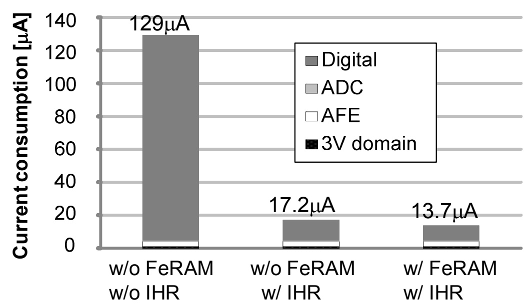


Fig. 18. Contribution of dedicated IHR monitor and FeRAM.

TABLE III
PERFORMANCE COMPARISON WITH PREVIOUS STUDIES

	VLSI'11 [26]	ISSCC'12 [27]	ISSCC'13 [28]	VLSI'13 [12]	This work
Technology	0.18μm	0.13μm	0.18μm	0.13μm	0.13μm
Supply voltage	1.2V	0.3-0.7V	1.8/3.2V	0.5-1.0V	1.2V/3.0V
Frequency	1MHz	1.7MHz-2kHz	20kHz	8-32kHz, 24/40MHz	32kHz, 24MHz
MCU	n/a	8b RISC	n/a	32b Andes N9	32b Cotex M0
On chip memory	46kB	5.5kB	n/a	20.5kB	129.75kB
Total power for IHR logging	31.1μW	19μW	18.7μW	16.1μW	18.24μW
Total current for IHR logging	25.9μA	>27μA	10.41μA	>16.1μA	13.7μA

processor. Consequently, the lifetime of the proposed system is about 24 days.

To evaluate the IHR accuracy, extracted results of the proposed sensor are compared with those of the reference sensor (CamNtech Actiwave Cardio [29]). The proposed sensor and reference sensor simultaneously record the ECG signal and IHR as depicted in Fig. 20. The distance between electrodes of the reference sensor is 14 cm.

Fig. 21 shows the measurement results of ECG waveforms obtained using the proposed sensor. As described in Section III, the limited distance of electrodes and limited performance of the analog front end affect the SNR degradation. Measurement results show that the gain of QRS complex is diminished according to the electrode distance. It is difficult to extract IHR using only a threshold approach from the ECG waveform with 5-cm electrode distance, especially not at rest.

In Fig. 22, the IHR output of the proposed sensor is

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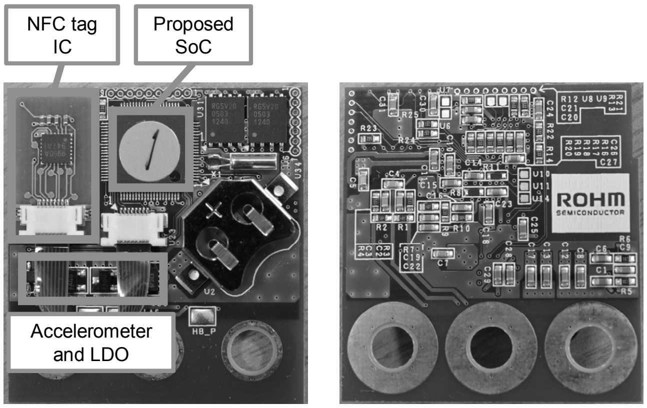

Fig. 19. Application board for the proposed sensor.

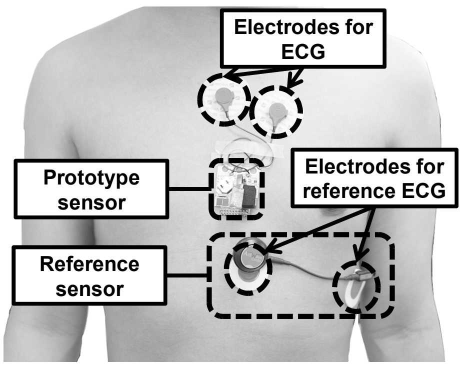

Fig. 20. Experimental set up for electrode distance test.

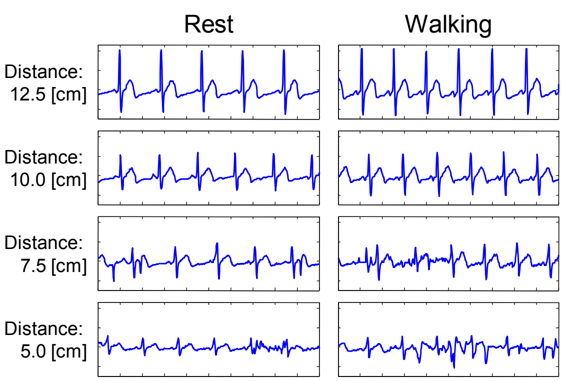

Fig. 21. Measured ECG waveform in rest and walking condition with 5.0 cm, 7.5 cm, 10.0 cm, and 12.5 cm electrode distance.

compared with the reference sensor. Then, the electrode distance of proposed sensor is set to 5 cm. Then, the root mean square error is 1.893. This result demonstrates that the proposed system can extract IHR correctly, but the electrode distance and the SNR of ECG signal are limited. It is noteworthy that, although the output of reference sensor is updated in every R-peak detected, the output of the proposed IHR monitor is updated every second, as depicted in Fig. 22.

Finally, we evaluated long-term data logging with a healthy subject, a 24-year-old man, in daily life. The upper part of Fig. 23 shows the heart rates calculated from the obtained IHR. The bottom side shows the obtained acceleration value. Results show that the IHR is extracted correctly, although the subject is not at rest. Fig. 24 shows the result of heart rate variability (HRV) analysis [2, 30] using the extracted IHR of daily life

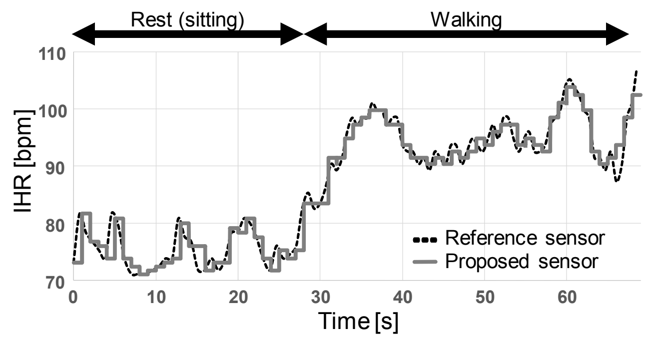

Fig. 22. Comparison of measured IHR of proposed sensor with 5.0 cm electrode distance and reference sensor (CamNtech Actiwave Cardio [29]).

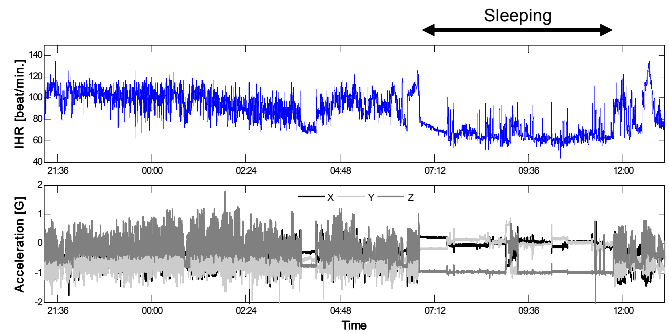

Fig. 23. Measurement results of daily life monitoring.

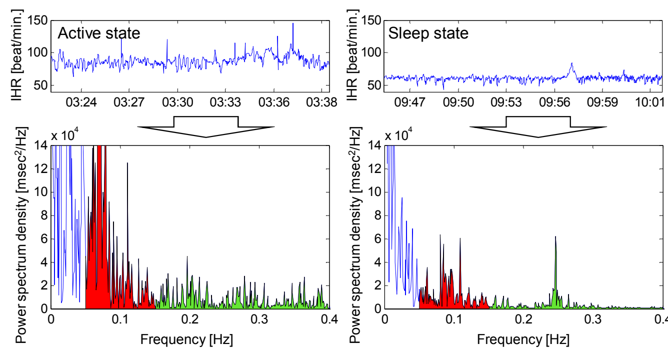

Fig. 24. Comparison of active and sleep state in daily life monitoring using heart rate variability (HRV) analysis.

monitoring. The HRV analysis result in the sleep state clearly indicates the parasympathetic nervous tone. In contrast, the sympathetic nervous tone can be observed in the active state.

V. Conclusion

As described in this paper, we proposed a low-power ECG processor with a robust heart rate monitor. The robust heart rate monitor can correctly extract a heart rate from noisy environments using the STAC algorithm. The measured total current consumption is 13.7 μA at 1.2V and 3.0V power supply for the heart rate logging application.

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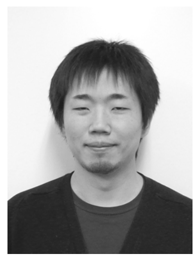

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