A Wearable Healthcare System with a 13.7 \( \mu \text{A} \) Noise Tolerant ECG Processor

Shintaro Izumi, Member, IEEE, Ken Yamashita, Student Member, IEEE, Masanao Nakano, Student Member, IEEE, Hiroshi Kawaguchi, Member, IEEE, Hiromitsu Kimura, Member, IEEE, Kyoji Marumoto, Takaaki Fuchikami, Yoshikazu Fujimori, Member, IEEE, Hiroshi Nakajima, Member, IEEE, Toshikazu Shiga, and Masahiko Yoshimoto, Member, IEEE

Abstract—To prevent lifestyle diseases, wearable bio-signal monitoring systems for daily life monitoring have attracted attention. Wearable systems have strict size and weight constraints, which impose significant limitations of the battery capacity and the signal-to-noise ratio of bio-signals. This report describes an electrocardiograph (ECG) processor for use with a wearable healthcare system. It comprises an analog front end, a 12-bit ADC, a robust Instantaneous Heart Rate (IHR) monitor, a 32-bit Cortex-M0 core, and 64 Kbyte Ferroelectric Random Access Memory (FeRAM). The IHR monitor uses a short-term autocorrelation (STAC) algorithm to improve the heart-rate detection accuracy despite its use in noisy conditions. The ECG processor chip consumes 13.7 \( \mu \text{A} \) for heart rate logging application.

Index Terms—Biomedical signal processing, Electrocardiography, Heart rate extraction, Microcontrollers, Mobile healthcare, Wearable sensors

I. INTRODUCTION

Because of the advent of an aging society, mobile health plays an ever more prominent role [1]. Daily-life monitoring is especially important in preventing lifestyle diseases, which have rapidly increased the number of patients and elderly people requiring nursing care. Our goal is the monitoring and display of vital signals and physical activity in daily life to improve users’ quality of life and realize a smart society.

We propose an Instantaneous Heart Rate (IHR) monitoring and electrocardiograph (ECG) processor for use in a wearable healthcare system. The IHR is an important bio-signal used for heart disease detection, heart rate variation analysis [2], and exercise intensity estimation [3].

Key factors affecting wearable system usability are miniaturization and weight reduction. However, a wearable ECG monitor is sensitive to extraneous noise because its electrodes are close together. The SNR of ECG signals will be especially degraded if a user is not at rest. Consequently, a sophisticated and costly analog front end is usually required. However, the feature and purpose of our approach is digital signal processing to reduce the performance requirements of the analog portion and to minimize the overall system power consumption. The battery weight is a dominant characteristic of the wearable system. Therefore, the battery capacity and power consumption must be limited as much as possible.

II. SYSTEM DESCRIPTION AND ARCHITECTURE

Fig. 1 presents an overview of the wearable healthcare system, comprising the proposed ECG processor, Near Field Communication (NFC) tag IC, and accelerometer IC. The NFC is used for program loading, individual optimization, and logging data transfer from the ECG processor. Compared with Bluetooth Low Energy or ZigBee, the standby power of NFC is extremely small. The active communication energy is also consumed by a reader/writer side when using a passive NFC tag.

![Fig. 1. Wearable healthcare system overview.](image-url)
Therefore, the proposed system uses NFC to cooperate with a Smartphone (or reader/writer).

Fig. 2 presents a block diagram showing the proposed ECG processor, which consists of an ECG sensing block, Ferroelectric Random Access Memory (FeRAM), 32-bit Cortex-M0 core, and extra interfaces. Because the frequency range of vital signals is low (less than 1 kHz), both the standby power reduction and sleep time maximization are important to minimize the total power consumption. The 64-Kbyte FeRAM is integrated as a data buffer for daily life monitoring because the leakage current of the data buffer is dominant in the standby state.

The ECG sensing block has an analog front end (AFE), a 12-bit SAR ADC, and a robust IHR monitor. Although the IHR monitor using high-order eight-bit data of the ADC, 12-bit ADC output also directly connected to Cortex M0. The AFE includes a 34-dB gain instrumental amplifier and a 20-dB gain amplifier as shown in Fig. 3. The ADC sampling rate can be set to 1 kSamples/s for ECG processing mode and 128 Samples/s for IHR monitoring mode. The robust IHR monitor is the main contribution of this study.

The operating frequency of the Cortex M0 core, which is used for an on-node vital signal processing, is 24 MHz, whereas the operating frequency of other digital blocks is 32 kHz. The slow signals in the 32-kHz domain are synchronized at the low-speed bus to the 24-MHz domain as shown in Fig. 4. To minimize the power consumption of registers in the low-speed bus, the 24-MHz clock is gated using bus control signals. When the Cortex M0 core is in a deep sleep state, the on-chip 24-MHz oscillator is also stopped.

Fig. 5 shows the sequence diagram of the proposed system for the data logging application. When the system starts, only the 32-kHz real time clock and NFC interface circuits for RF signal detection are activated. If the NFC reader/writer starts communication in the transmission range, then the NFC interface and sequencer of the ECG processor are kicked by the NFC tag IC.

First, a program binary for the Cortex M0 is transferred from the reader/writer side. Then the program is stored directly in FeRAM. When the ECG processor receives the "bootloading" packet, the program is transferred from FeRAM to instruction SRAM. The program will be running. Before starting a data logging service or any other service, the NFC reader/writer communicates with Cortex M0 core for parameter
A noise tolerant algorithm is implemented in dedicated hardware to achieve both noise tolerance and low-power consumption.

A. Heart rate extraction algorithms

Extracting R-waves (see Fig. 6(a)) with threshold determination is a general approach. Recently, various statistical approaches have been proposed for noise-tolerant threshold calculation.

The Pan–Tomkins (PT) algorithm [5] is most commonly used for beat detection. This algorithm uses band-pass filtering, differentiation, squaring, and moving window integration. The SQRS [6] and WQRS [7] algorithms can respectively detect QRS based on ECG slope and length transform. The SQRS uses band pass filtering for noise reduction, which uses only the integer coefficient. The WQRS also uses a low-pass filter to remove baseline wander. The Discrete Wavelet Transform (DWT) [8–10] uses a wavelet transform with quadratic spline wavelet (QSWT). The threshold is calculated using the root mean square value of the wavelet transform. This algorithm has been used in robust ECG monitoring LSIs [10–12]. The Quad Level Vector (QLV) algorithm [13] is implemented in dedicated hardware for ECG monitoring LSI [14, 15]. The QLV is generated using DWT and the adaptive threshold. Then, the threshold is determined by the maximum mean deviation (MD) of the previous heartbeats. The Continuous Wavelet Transform (CWT) algorithm [16–18] employs a Mexican hat wavelet in the frequency interval of 15–18 Hz. The R-peak can be extracted using the adaptive threshold, which is calculated using the modulus maxima of the CWT. This algorithm is also implemented in [15].

However, as depicted in Fig. 6, both misdetection and false detection are increased in the wearable healthcare system by noise from various sources such as myoelectric signals from muscle and electrode movement because the power consumption and electrode distance of the wearable sensor are strictly limited to reduce its size and weight.

Autocorrelation [19, 20] and template matching [21] are more robust approaches to prevent incorrect detection because these algorithms use the similarity of QRS complex waveforms and have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system [20]. However, the method necessitates numerous computations because it calculates the average heart-rate over a long duration (30 s). In our previous work, a short-term autocorrelation (STAC) technique was proposed for IHR detection [22].

Fig. 7 portrays IHR extraction using STAC. As depicted in Fig. 7 and (1–5), the IHR at time $t_n$ ($\text{IHR}_{t_n}$) is obtained as a window shift length ($T_{\text{shift}}$) that maximizes the correlation coefficient between the template window and the search window ($C_{t_n}$).

$$C_{t_n}[T_{\text{shift}}] = w_l \cdot \sum_{i=0}^{L} Q_{e}[t_n - i] \cdot Q_{w}[t_n - T_{\text{shift}} - i]$$

$$RR_{\text{n}} = \arg_{T_{\text{shift}}} \max_{0.25 \times F_s \leq T_{\text{shift}} \leq 1.5 \times F_s} [C_{t_n}[T_{\text{shift}}]]$$

$$L_{\text{win}} = 1.5 \times F_s$$

### III. ROBUST INSTANTANEOUS HEART RATE MONITOR

Ultra-low-power ADCs, which have sub-μW power consumption and a limited sample rate, have been developed for biomedical applications [4]. Furthermore, according to Moore's law, the power of digital components increases with the progress of process technology. However, the power consumption of analog circuits will not decrease similarly. Therefore, the features and purposes of our approach are the use of digital signal processing to reduce the performance requirements of analog components including electrode and to minimize the system's overall power consumption. In this work, a noise tolerant algorithm is implemented in dedicated configuration, time synchronization, and checking results of the self-test. When a packet to Cortex M0 core is received, the core is awakened by an interrupt request (IRQ) because it is normally in a deep sleep state. The payload of the received packet is accessible through the data bus. A "logging start" packet and a "logging stop" packet use the same procedure.

During the data logging operation, a timer circuit periodically wakes up the Cortex M0 core using the IRQ. Then the measured or calculated data are stored to FeRAM through the data bus. Therefore, the FeRAM is used both as a program ROM and a data buffer. The logging data in the FeRAM can be read out directly by the NFC interface circuit without the Cortex M0 core.

All application layer functions are defined using the payload in the transport protocol frame of NFC.
Fig. 11. Required operating frequency for real time IHR extraction.

In the equations presented above, $F_s$, $L_{\text{win}}$ and $w_1$ respectively denote the sampling rate (samples/s), the window length, and the weight coefficient. The value of $T_{\text{shift}}$ is set as 0.25 s to 1.5 s because the heart rate of a healthy subject is 40 bpm to 240 bpm. The $L_{\text{win}}$ is updated according to the estimated IHR to reduce the computational amount and to improve the IHR estimation accuracy. Then, the range of $L_{\text{win}}$ and $w_1$ is determined by the maximum rate of the beat-to-beat variation, which is generally 20% in a healthy subject [23].

In this work, we introduce a robust IHR monitor, which employs two-step noise reduction technique. In the first stage, the QSWT filter is used to mitigate the baseline wander and hum noise. Fig. 8 presents a block diagram and frequency characteristics of the QSWT with 128-Hz sampling rate. The QSWT requires few calculations and low hardware cost because it can be implemented using only adders and shift operators. The base-line wander and hum noise can be removed easily using QSWT. Unfortunately, it is difficult to remove the myoelectric noise and electrode motion artifacts only using QSWT because these frequency ranges are similar to the desired ECG signal.

Therefore, in the second stage, the IHR is extracted using the STAC method. The STAC is also implemented as dedicated hardware to minimize the power overhead. Fig. 9 presents the block diagram of the IHR monitor and STAC processing core. Each STAC core has CC buffer to store the intermediate value of $CC_n[T_{\text{shift}}]$ in (1). The CC buffer is updated in synchronization with ADC output (see Fig. 10). Since the $L_{\text{win}}$ is 1.5 s and because IHR is updated every second, two STAC cores alternately calculate IHR with 0.5 s overlap.

The dual STAC core architecture also contributes to reduction of the operating frequency. Fig. 11 shows the required operating frequency to realize the real-time STAC calculation. Because the sampling rate target is set to 128 Samples/s in this study, the required frequency is lower than 32 kHz when applying dual core architecture. Therefore, this STAC hardware can operate only using 32.768-kHz real-time clocks. Note that the real-time clock, which has low power consumption, is a necessary component of a wearable monitoring system.

The gate level simulation result shows the IHR monitor block, which contains QSWT, two STAC cores, and SRAMs, consumes 1.21 $\mu$A in 130-nm CMOS process. The digital logic and SRAMs respectively consume 0.26 $\mu$A and 0.95 $\mu$A, which include 0.4-$\mu$A leakage current.

C. Performance evaluation of heart rate extraction

To evaluate the heart rate extraction algorithms, we implemented the conventional and our proposed algorithms, which combined STAC with QSWT filter, using MATLAB. First, we investigated the successful rate of heart rate extraction using 23 records from the MIT-BIH arrhythmia database [24]. Table I shows that no significant difference was found among the successful rates in clean waveforms, although they include arrhythmia.
The effect of noise contamination and to eliminate the effect of detection. The MIT-BIH record #100 is used to evaluate the ratio (SNR) is defined as shown below.

\[ \text{SNR} = 10 \log \frac{S}{N \times \alpha^2} \]  \hspace{1cm} (6)

Here, \( S \), \( N \), and \( \alpha \) respectively denote the signal power, frequency-weighted noise power, and scale factor. Simulation results show that the proposed algorithm has better noise tolerance in each condition. As shown in Fig. 13, the proposed IHR monitor has higher noise tolerance and minimum current consumption compared with previous studies of hardware implemented heart rate extractor.

Finally, we evaluated the heart rate extraction success rate using the measured ADC output data of proposed SoC. To evaluate the noise tolerance, the ADC output data with the rest, walking, and running condition are used (see Fig. 14). The duration of each condition is 30s. Table II shows the performance comparison of heart rate extraction success rate with healthy five subjects, from 22 to 29 year-old man. As shown in Table II, the proposed method still has better performance in real data.

IV. IMPLEMENTATION RESULT

The test chip is fabricated using 130-nm CMOS technology. Fig. 15 presents a chip photograph and a performance summary. The operating voltage is 1.2 V for AFE, ADC, SRAM, 24-MHz oscillator, and digital blocks. The FeRAM, 32-KHz oscillator, and IO circuits are operated with 3.0 V supply voltage.
To demonstrate the test chip performance, we implemented a heart rate logging application. In this experiment, an Android™ smartphone is used for program loading and logging data retrieval. As portrayed in Fig. 16, the IHR is extracted correctly in a noisy condition.

Fig. 17 portrays the current consumption with a heart rate logging application. In this experiment, the ADC sampling rate and the logging interval of IHR are set respectively to 128 Samples/s and 1 Sample/s. Then the AFE, 32-kHz OSC, and Timer block are always activated. The measurement results show that the test chip consumes 13.7 μA on average for the heart rate logging application. The peak current, which is consumed when the Cortex and FeRAM are activated to store the logging IHR data every second, is less than 1 mA.

As presented in Fig. 18, the IHR monitor and FeRAM respectively contribute to active ratio reduction and sleep power reduction. Table III presents a performance comparison of the previous studies. Compared with earlier ECG processors [12, 26-28], the proposed processor has lower power and greater memory capacity for daily-life monitoring.

Fig. 19 portrays the application board of the proposed wearable sensor system. The board is 39.5 mm × 42.0 mm, with maximum thickness of 5 mm. The proposed system weighs 5.5 g including 1.0 g battery. We employed a 35mAh battery in this system. The total current consumption is less than 60 μA, which includes the Accelerometer IC, NFC tag IC, linear regulator, 32.768 kHz crystal oscillator, and the proposed ECG processor. Consequently, the lifetime of the proposed system is about 24 days.

To evaluate the IHR accuracy, extracted results of the proposed sensor are compared with those of the reference sensor (CamNtech Actiwave Cardio [29]). The proposed sensor and reference sensor simultaneously record the ECG signal and IHR as depicted in Fig. 20. The distance between electrodes of the reference sensor is 14 cm.

Fig. 21 shows the measurement results of ECG waveforms obtained using the proposed sensor. As described in Section III, the limited distance of electrodes and limited performance of the analog front end affect the SNR degradation. Measurement results show that the gain of QRS complex is diminished according to the electrode distance. It is difficult to extract IHR using only a threshold approach from the ECG waveform with 5-cm electrode distance, especially not at rest.

In Fig. 22, the IHR output of the proposed sensor is
compared with the reference sensor. Then, the electrode
distance of proposed sensor is set to 5 cm. Then, the root mean
square error is 1.893. This result demonstrates that the proposed
system can extract IHR correctly, but the electrode distance and
the SNR of ECG signal are limited. It is noteworthy that,
although the output of reference sensor is updated in every
R-peak detected, the output of the proposed IHR monitor is
updated every second, as depicted in Fig. 22.

Finally, we evaluated long-term data logging with a healthy
subject, a 24-year-old man, in daily life. The upper part of Fig.
23 shows the heart rates calculated from the obtained IHR. The
bottom side shows the obtained acceleration value. Results
show that the IHR is extracted correctly, although the subject is
not at rest. Fig. 24 shows the result of heart rate variability
(HRV) analysis [2, 30] using the extracted IHR of daily life
monitoring. The HRV analysis result in the sleep state clearly
indicates the parasympathetic nervous tone. In contrast, the
sympathetic nervous tone can be observed in the active state.

V. CONCLUSION

As described in this paper, we proposed a low-power ECG
processor with a robust heart rate monitor. The robust heart rate
monitor can correctly extract a heart rate from noisy
environments using the STAC algorithm. The measured total
current consumption is 13.7 \( \mu A \) at 1.2V and 3.0V power supply
for the heart rate logging application.

ACKNOWLEDGMENT

The authors would like to thank Y. Kawamoto, Y. Tanaka, T.
Fuji, and Y. Nakai with the Graduate School of System
Informatics, Kobe University, for assistance in the data logging
experiment.
REFERENCES


Shintaro Izumi (S’09–M’12) respectively received his B.Eng. and M.Eng. degrees in Computer Science and Systems Engineering from Kobe University, Hyogo, Japan, in 2007 and 2008. He received his Ph.D. degree in Engineering from Kobe University in 2011. He was a JSPS research fellow at Kobe University from 2009 to 2011. Since 2011, he has been an Assistant Professor in the Organization of Advanced Science and Technology at Kobe University. He has served as a Program Committee Member for IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips) and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences.

His current research interests include biomedical signal processing, communication protocols, low-power VLSI design, and sensor networks.

Ken Yamashita (S’13) received his B.Eng. degree in Informatics from Sizouka University, Sizouka, Japan, in 2012, and M.Eng. degree in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2014. His current research is related to wearable health-care systems.
Masanao Nakano (S’12) respectively received his B.Eng. and M.Eng. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2012 and 2014. His current research is related to wearable health-care systems.

Hiroshi Kawaguchi (M’98) received B.Eng. and M.Eng. degrees in electronic engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and earned a Ph.D. degree in Engineering from The University of Tokyo, Tokyo, Japan, in 2006.

He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to The Institute of Industrial Science, The University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with The Department of Information Science at that university. He is also a Collaborative Researcher with The Institute of Industrial Science, The University of Tokyo. His current research interests include low-voltage SRAM, RF circuits, and ubiquitous sensor networks.

Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Program Committee Member for IEEE Custom Integrated Circuits Conference (CICC) and IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM).

Hiromitsu Kimura (M’99) received the B.E. degree in Electrical Engineering from Tohoku University, Sendai, Japan, in 1998 and the Master of Information Science and Doctor of Information Science degrees in Computer and Mathematical Sciences from Tohoku University in 2000 and 2003, respectively.

He is currently a Senior Engineer of ROHM Co. Ltd., Japan. His main interests and activities are in the areas of Ferroelectric random access memory (FeRAM) and non-volatile logic LSI.

Dr. Kimura received the Judge’s Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002 and the Grand Award at IEEE International Meeting for Future of Electron Devices, Kansai in 2006. Dr. Kimura is a member of the IEEE.

Kyoji Marumoto has been working on ROHM Co., Ltd., Kyoto, Japan.

Takaaki Fuchikami has been working on LSI Product Development Headquarters Core Technology Development Division, ROHM Co., Ltd., Kyoto, Japan.

Yoshikazu Fujimori received the B.E. and M.E. degrees in electronics engineering from Kyoto University, Kyoto, Japan. In 1996, he joined ROHM Co. Ltd., Kyoto, Japan, where he has been working on device and process development of Ferroelectric Random Access Memory (FeRAM). He received the degree of Doctor of Engineering from Kyoto University in 2005. His research interests include low power and functional applications of non-volatile ferroelectric devices and piezoelectric devices.

Hiroshi Nakajima (M’97) received the B.Eng. degree in System Engineering from Kobe University, Japan, in 1985, and Ph.D. degree in Systems Information Science from Kumamoto University, Japan, in 2004. He is currently Chief Specialist of Technology at Omron Corporation. Besides long term career at industry, he also has some academic careers such as visiting professor at Kyushu Institute of Technology. He has focused on the general solution for improvement of health in humans, machines, and energy consumptions by applying sensory inspection and computational intelligence. He received the best paper award from Interaction’99 in 1999, the best author award from Information Processing Society of Japan in 2000, the Industrial Outstanding Application Award from International Fuzzy Systems Association in 2007, the best paper award from Japan Society for Fuzzy Theory and Intelligent Informatics in 2009, and Biomedical Wellness Award from SPIE in 2011.
Toshikazu Shiga received the B.S. degree in 1982 from Yamaguchi University, Yamaguchi Japan in electrical engineering, the M.S. degree in 1986 from Hokkaido University, Hokkaido Japan, and Ph.D. degree in 1998 from Hokkaido University, Hokkaido Japan, both in biomedical engineering. In April 1986, he was joined the research and development division of Omron Healthcare Co, ltd. His areas of research interest are the measurement of biological signal and all biomedical engineering.

Masahiko Yoshimoto (M’98) joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in 1977. From 1978 to 1983 he had been engaged in the design of NMOS and CMOS static RAM. Since 1984 he had been involved in the research and development of multimedia ULSI systems. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. Since 2000, he had been a professor of Dept. of Electrical & Electronic System Engineering in Kanazawa University, Japan. Since 2004, he has been a professor of Dept. of Computer and Systems Engineering in Kobe University, Japan. His current activity is focused on the research and development of an ultra low power multimedia and ubiquitous media VLSI systems and a dependable SRAM circuit. He holds on 70 registered patents. He has served on the program committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. Also he served as Guest Editor for special issues on Low-Power System LSI, IP and Related Technologies of IEICE Transactions in 2004. He was a chair of IEEE SSCS (Solid State Circuits Society) Kansai Chapter from 2009 to 2010. He is also a chair of The IEICE Electronics Society Technical Committee on Integrated Circuits and Devices from 2011-2012. He received the R&D100 awards from the R&D magazine for the development of the DISP and the development of the realtime MPEG2 video encoder chipset in 1990 and 1996, respectively. He also received 21th TELECOM System Technology Award in 2006.