Normally Off ECG SoC with Non-Volatile MCU and Noise Tolerant Heartbeat Detector

Shintaro Izumi, *Member, IEEE*, Ken Yamashita, Masanao Nakano, Shusuke Yoshimoto, *Member, IEEE,* Tomoki Nakagawa, Yozaburo Nakai, Hiroshi Kawaguchi, *Member, IEEE*, Hiromitsu Kimura, *Member, IEEE*, Kyoji Marumoto, Takaaki Fuchikami, Yoshikazu Fujimori, *Member, IEEE*, Hiroshi Nakajima, *Member, IEEE*, Toshikazu Shiga, and Masahiko Yoshimoto, *Member, IEEE*

***Abstract*— This paper describes an electrocardiograph (ECG) monitoring SoC using a non-volatile MCU (NVMCU) and a noise-tolerant instantaneous heartbeat detector. The novelty of this work is the combination of the non-volatile MCU for normally off computing and a noise-tolerant-QRS (heartbeat) detector to achieve both low-power and noise tolerance. To minimize the stand-by current of MCU, a non-volatile flip-flop and a 6T-4C NVRAM are used. Proposed plate-line charge-share and bit-line non-precharge techniques also contribute to mitigate the active power overhead of 6T-4C NVRAM. The proposed accurate heartbeat detector uses coarse-fine autocorrelation and a template matching technique. Accurate heartbeat detection also contributes system-level power reduction because the active ratio of ADC and digital block can be reduced using heartbeat prediction. Measurement results show that the fully integrated ECG-SoC consumes 6.14 μA including 1.28-μA non-volatile MCU and 0.7-μA heartbeat detector.**

***Index Terms*— Biomedical signal processing, Electrocardiography, Heartbeat detection, Microcontrollers, Mobile healthcare, Non-volatile memory, Wearable sensors**

I. Introduction

MOBILE health is expected to play an increasingly prominent role in health provision with the advent of an aging society [1]. Daily life monitoring is especially important to prevent lifestyle diseases, which raise the numbers of patients and elderly people requiring care. Key factors affecting wearable system usability are miniaturization and weight reduction. Battery weight is a dominant characteristic of a wearable system. Therefore, battery capacity and power consumption must be limited.

This report specifically describes an electrocardiograph (ECG) monitoring SoC for use in a wearable healthcare system. Table 1 shows specifications of the proposed system using ECG monitoring SoC. The proposed SoC, which uses normally off computing using non-volatile MCU (NVMCU) and a dedicated heartbeat detector, can minimize the active ratio and the stand-by power dissipation of the sensor system. This heart beat detector has superior noise tolerance and low power consumption.

A preliminary version of this work has been reported in the literature [2]. This paper presents additional details of implementation and performance evaluation results. Section II of this report explains the architecture of the proposed ECG SoC and the non-volatile MCU. The noise-tolerant heartbeat detection algorithm and its dedicated hardware implementation

TABLE I
SPECIFICATIONS OF PROPOSED SYSTEM

Size	28.5mm × 22.5mm (w/o electrodes)
Weight	3.9g (w/ battery)
Sensor	ECG and heart rate
Processing unit	32-bit Cortex M0 (24-MHz operation)
Memory	16kByte NVRAM
Communication	Near Field Communication (passive mode)
Battery capacity	35mAh (CR1220 Lithium battery)
Current consumption	6.14μA

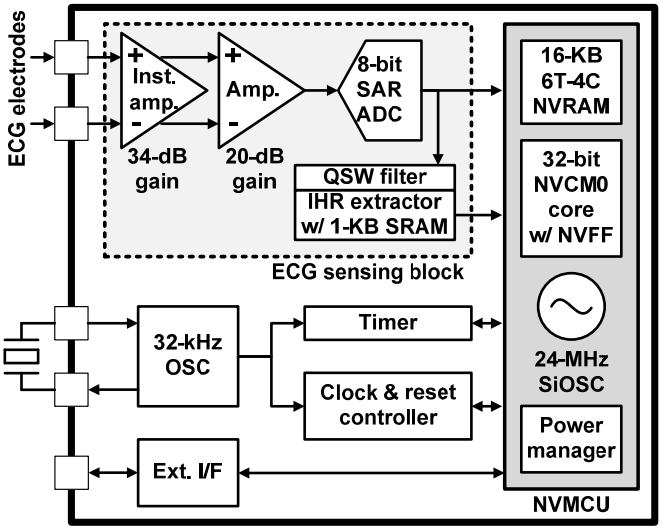


Fig. 1. Block diagram of normally off ECG-SoC.

This research was partially supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy an Industrial Technology Development Organization (NEDO) and a grant from Tateishi Science and Technology Foundation.

S. Izumi, K. Yamashita, M. Nakano, T. Nakagawa, Y. Nakai H. Kawaguchi, and M. Yoshimoto are with the Graduate School of System Informatics, Kobe University, 1-1 Rokkodai, Nada, Kobe, Hyogo 657-8501 Japan (e-mail: shin@cs28.cs.kobe-u.ac.jp).

S. Yoshimoto is with the Institute of Scientific and Industrial Research, Osaka University, 8-1 Mihogaoka, Ibaraki, Osaka 567-0047 Japan.

H. Kimura, K. Marumoto, T. Fuchikami, and Y. Fujimori are with Rohm Co. Ltd., 21 Saiin Mizosaki-cho, Ukyo-ku, Kyoto 615-8585 Japan.

H. Nakajima is with Omron Corporation, Horikawa Higashiiru, Shiokoji-Dori, Shimogyo-Ku, Kyoto 600-8530 Japan.

T. Shiga is with Omron Healthcare Co., Ltd., 53 Kunotsubo, Terado-cho, Muko, Kyoto 617-0002 Japan.

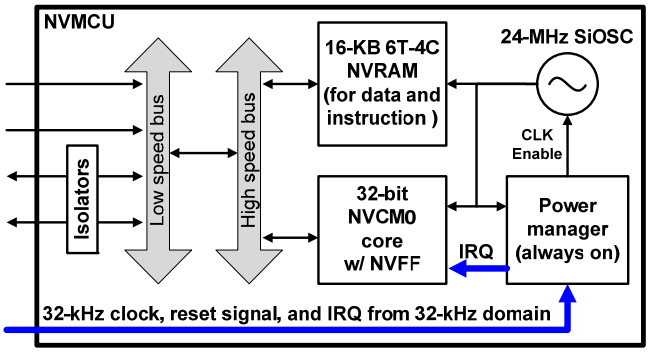


Fig. 2. Block diagram of non-volatile MCU (NVMCU).

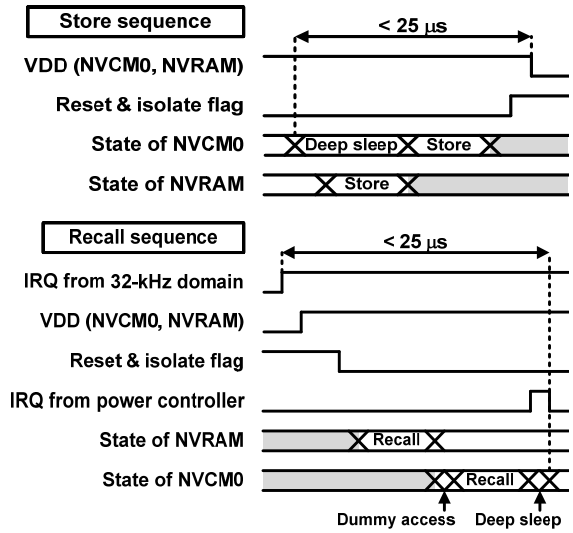


Fig. 3. Timing diagram of store/recall sequence in NVMCU.

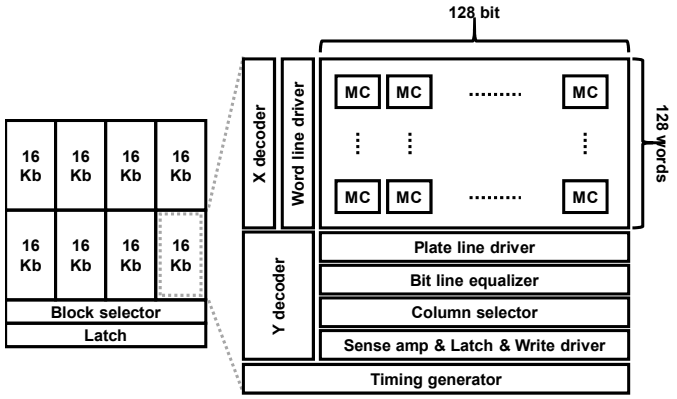


Fig. 4. Block diagram of 16 Kbyte non-volatile memory (NVRAM).

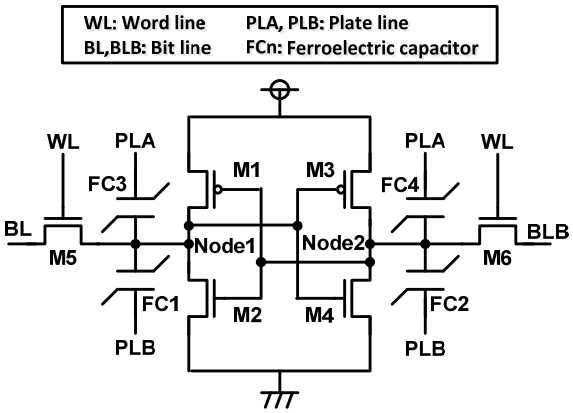


Fig. 5. 6T-4C memory cell circuit.

are described in Section III. Section IV presents test chip implementation and performance evaluation results. Finally, conclusions are presented in Section V.

II. Normally Off ECG-SoC Architecture

Fig. 1 presents a block diagram showing the proposed ECG-SoC, which consists of an ECG sensing block, NVMCU, and extra interfaces. The ECG sensing block has an analog front end (AFE), an 8-bit SAR ADC, and a robust heartbeat detector. The ADC output is connected to the heatbeat detector and the NVMCU block. The operating frequency of the NVMCU, which is used for on-node vital signal processing, is 24 MHz, the operating frequency of other digital blocks is 32 kHz. The AFE includes a 34-dB gain instrumental amplifier and a 20-dB gain amplifier. The ADC sampling rate is set to 128 samples/s for the proposed heartbeat detector.

A. Non-volatile MCU

The NVMCU (see Fig. 2) includes a Cortex M0 (CM0) core with ferroelectric-based nonvolatile flip-flops (NVFF) [3, 4], a 16-Kbyte 6T-4C NVRAM for instruction and data memory, and peripherals. Because the frequency range of vital signals is low, both the standby power reduction and sleep time maximization are important for system level power reduction. Therefore, the NVMCU is normally in a deep sleep state in our application. As presented in Fig. 2, the NVMCU is awakened only by an interrupt request (IRQ) from the 32-kHz always-on domain.

Slow signals from the 32-kHz always-on domain are synchronized at the low-speed bus to the 24-MHz normally off NVMCU domain. To minimize the active power consumption of registers in the low-speed bus, the 24-MHz clock is gated using bus control signals.

Standby current of the entire 24 MHz domain including an on-chip 24-MHz oscillator can be cut when the state of CM0 core transits to a deep sleep state. Fig. 3 shows the shut-down and wake-up sequence of NVMCU. Then the data in the NVRAM and register values of CM0 core in the NVFF are stored sequentially to ferroelectric capacitors. The data and register values of NVMCU will be recalled if the interrupt occurs from the 32-kHz domain. Although the store and recall operation for NVRAM and NVFF dissipate up to 25 μs overhead, that figure is sufficiently small in our application.

B. Non-volatile Memory

Fig. 4 portrays a block diagram of the 16-Kbyte 6T-4C NVRAM. It comprises eight macro blocks, each consisting of 2-Kbyte memory cell arrays, which has 128 columns and 128 rows. We used a 6T-4C memory cell (see Fig. 5) for the NVRAM because it presents the benefit of non-volatility and fast access time [5]. However, it has active power dissipation from the large ferroelectric capacitor, which is connected directly to plate-lines and internal nodes. Therefore, this work presents plate-line charge-share and bit-line non-precharge

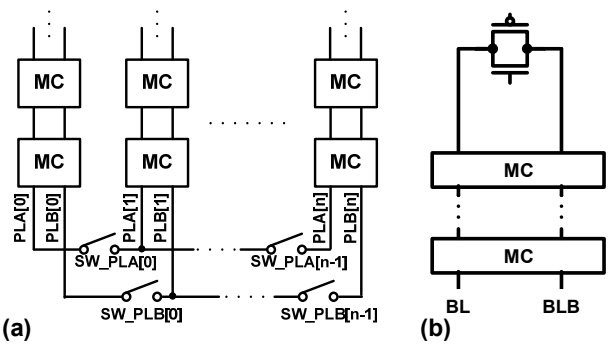


Fig. 6. (a) Plate-line charge sharing switch and (b) bit-line equalizer.

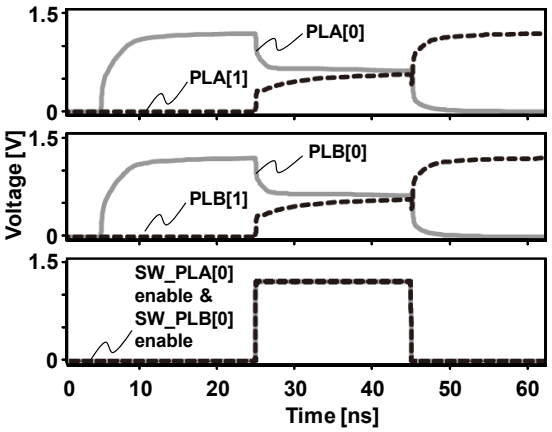


Fig. 7. Store operation with plate-line charge share.

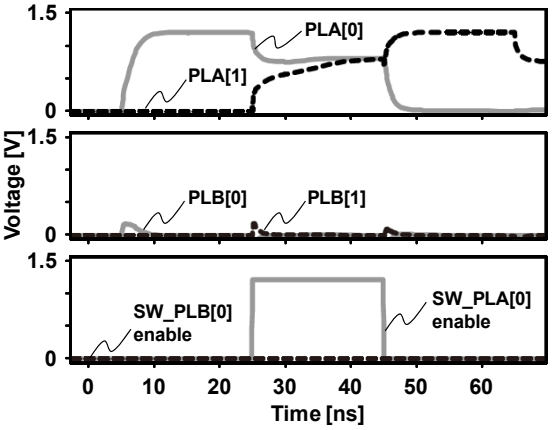


Fig. 8. Recall operation with plate-line charge share.

techniques to reduce the power overhead.

The 6T-4C memory requires store and recall operations before power gating and power on. The plate-lines (PLA and PLB in Fig. 5) are charged by a plate line driver in these operations. However, driving of the plate lines requires large power dissipation because large ferroelectric capacitors are connected to the plate lines. Therefore, plate-line charge-share is introduced to reduce the power consumption in store and recall operation. As depicted in Fig. 6(a), additional switches between plate lines are used to share the charge used for store and recall operations. The charge is transported sequentially from one plate line to the next one.

Fig 7 depicts the waveform of store operation with plate-line charge share. SW_PLA[0] and SW_PLB[0] are connected after

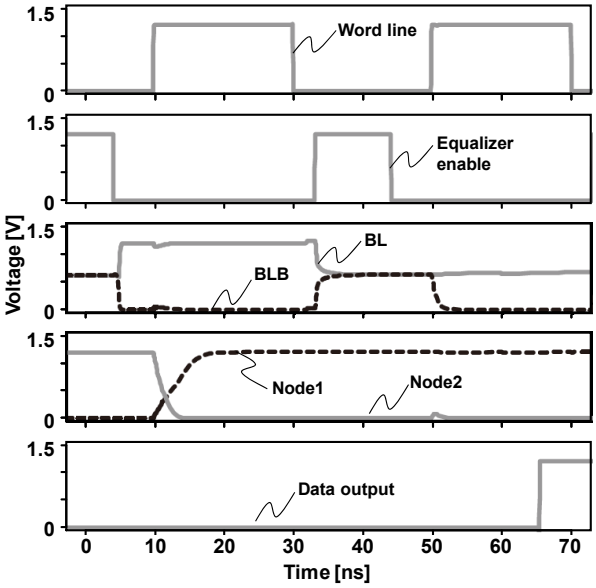


Fig. 9. Write and read operations with bit-line non-precharge.

PLA[0] and PLB[0] are charged. Then, the charging of PLA[0] and PLB[0] is shared with the PLA[1] and PLB[1]. Finally, PLA[1] and PLB[1] are charged after cutting off the SW_PLA[0]. Other plate-lines PLA[n] and PLB[n] are charged sequentially in the same manner. Fig. 8 depicts the waveform of the recall operation with the plate-line charge sharing. Only PLA[n] should be drive in this operation. As presented in Fig. 8, the charge of PLA[n] is shared in the same manner as the store operation. Consequently, in both store and recall operation, the plate-line driver need not charge plate lines from 0 V to VDD.

Next, bit-line non-precharge is introduced to reduce the power consumption in read and write operations. The conventional 6T-4C memory charges the bit-line before charging the word line to prepare read operations and to stabilize the status of the half-selected cell. The half-selected cell is selected by the X decoder, although it is not selected by the Y decoder during read and write operations. Because 128 memory cells are connected to each bit line in this design, the pre-charging power is dominant in the read and write operations. However, the bit-line precharge can be omitted. Only equalizing is used in this design. The large ferroelectric capacitors are also connected to the internal nodes of the memory cell. Therefore, the 6T-4C cell is sufficiently tolerant to the half-select problem.

Fig. 9 shows the waveform of read and write operations with bit-line non-precharge. First, bit-lines are equalized to force the same voltage by a bit-line equalizer (see Fig. 6(b)), they are not charged to VDD. During read and write operations, the bit line equalizer is disabled. Finally, the bit lines are equalized again when the operation is finished. Therefore the pre-charging power can be omitted from write and read operations.

Store and recall operations are executed sequentially in each macro block. Consequently, these operations require 128 cycles with 24-MHz operating frequency for the entire 16-Kbyte NVRAM.

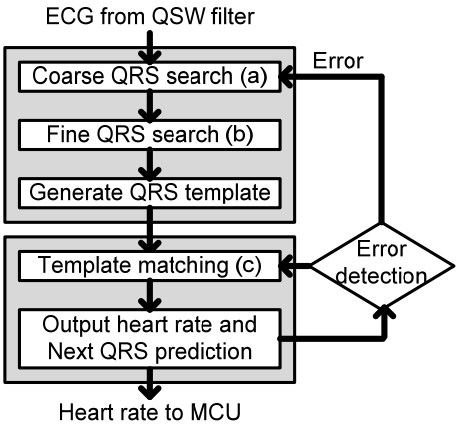


Fig. 10. Flow chart of heart beat detection algorithm.

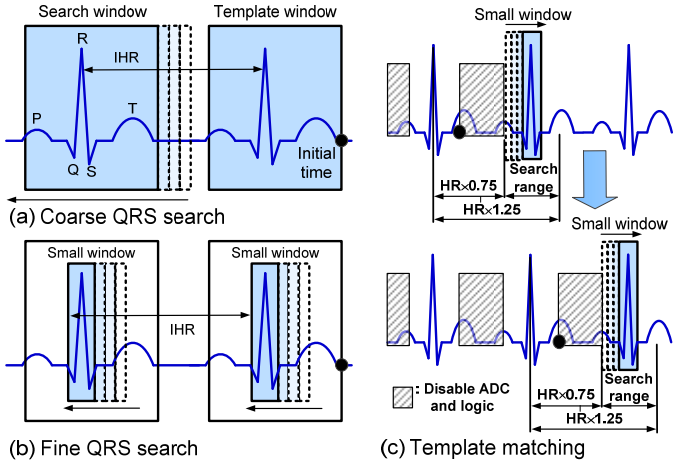


Fig. 11. Algorithm overview of coarse-fine QRS template generation and template matching with QRS prediction.

III. Noise-Tolerant Heartbeat Detector

The ECG signal in wearable systems is sensitive to various noises because the electrode distance, size, and the battery capacity are strictly limited. The SNR will be especially degraded if a user is not at rest. Therefore, our approach uses digital signal processing to mitigate the performance requirements for the analog portion and to minimize the overall system power consumption. For this work, we propose a noise-tolerant algorithm using a combination of short-term autocorrelation and the template matching approach. The proposed method is implemented in dedicated hardware to achieve both noise tolerance and low power consumption.

A. Heartbeat detection algorithms

Extracting R-waves with threshold determination is a general approach. Recently, various statistical approaches have been proposed for noise-tolerant threshold calculation [6–15]. However, both misdetection and false detection are increased in wearable healthcare systems by noise from various sources such as myoelectric signals from muscle and electrode movements because the power consumption and electrode distance of the wearable sensor are strictly limited to reduce its size and weight.

More robust approaches to prevent incorrect detection are autocorrelation [16, 17] and template matching [18] because these algorithms use the similarity of QRS complex waveforms and because they have no threshold calculation process. Autocorrelation has been used in a non-invasive monitoring system [17], but the method necessitates numerous computations to calculate the average heart rate over a long duration (30 s). A short-term autocorrelation (STAC) technique was proposed for heart rate detection in our previous work [19].

For this work, we implemented the combination algorithm of quadratic spline wavelet (QSW) filter [9–11] and two-stage STAC based heartbeat detection [20]. The QSW is commonly used as the low-power noise reduction method for ECG [11]. The hum-noise and baseline wander are well suppressed using QSW. Nevertheless, it is difficult to remove these noises solely by using QSW because it has a similar frequency range of the QRS complex. Therefore, in the next step, we used a noise-tolerant heartbeat detection algorithm.

Figs. 10 and 11 present the heartbeat detection algorithm. In the first stage, the template data of QRS complex are generated autonomously using the extended version of STAC. Following equations (1–4) express the coarse QRS search, as presented in Fig. 11 (a). The correlation coefficient (CC_{CS}) between the template window and the search window is calculated as presented below.

$$CC_{\mathrm{CS}}[n] = W_1^2 \cdot \sum_{i=0}^{L_{\mathrm{w}}} W_2 \cdot d[t_n - i] \cdot d[t_n - i - T_{\mathrm{shift}}] \tag{1}$$

$$W_1 = \begin{cases} 1 & (T_{\mathrm{shift}} \le 0.54) \\ 0.75 & (0.54 < T_{\mathrm{shift}} \le 0.98) \\ 0.5 & (T_{\mathrm{shift}} < 0.98) \end{cases} \tag{2}$$

$$W_2 = \begin{cases} 1 & (i \le 0.25 \cdot L_w) \\ 0.75 & (0.25 \cdot L_{\mathrm{w}} < i \le 0.5 \cdot L_{\mathrm{w}}) \\ 0.5 & (0.5 \cdot L_{\mathrm{w}} < i) \end{cases} \tag{3}$$

Here, $d[t_{\mathrm{n}}]$ denotes the nth sampled ECG data. W_1 and W_2 are the weight coefficients to avoid the detection error caused by multiple heart beats in search range. L_{w} is the search window and the template window length, which is set to 1.5 s for this study. Then, the window shift length T_{shift} with the maximum value of the correlation coefficient (4) shows the heart rate at time t_n ($IHR[n]$).

$$IHR[n] = \underset{0.27 \le T_{\mathrm{shift}} \le 1.5}{\arg_{T_{\mathrm{shift}}} \max} \{CC_{\mathrm{CS}}[n]\} \tag{4}$$

Equations (5) and (6) show the coarse QRS search, as presented in Fig. 11(b).

$$CC_{\mathrm{FS}}[n] = \sum_{i=0}^{L_{\mathrm{sw}}} d[t_n - i - T'_{\mathrm{shift}}] \cdot d[t_n - i - T'_{\mathrm{shift}} - IHR[n]] \tag{5}$$

$$t_{\mathrm{QRS}}[n] = t_n - \underset{0 \le T'_{\mathrm{shift}} \le L_w}{\arg_{T'_{\mathrm{shift}}} \max} \{CC_{\mathrm{FS}}[n]\} \tag{6}$$

Then, the QRS is detected by a small window with window length L_{SW}, set to 0.1 s. When the window shift length T_{shift} is set to $IHR[n]$ in (4), the QRSs exist at the same distance from the edge of the search window. The template window as presented in Fig. 11(b). Therefore, as shown in (5) and (6), the time of the nearest QRS complex (t_{QRX}) from t_n is calculable from the small window shift length (T'_{shift}) and the correlation coefficient between small windows ($CC_{FS}[n]$). Then, the initial QRS complex template TM_{init} is set as presented below.

$$TM_{\text{init}}[i] = d[t_{\text{QRS}}[n] + i] \quad (-\frac{L_{\text{sw}}}{2} \le i \le \frac{L_{\text{sw}}}{2}) \tag{7}$$

Next, template matching is conducted to extract QRS complexes as presented in Fig. 11(c). Then, the time at which the next QRS complex occurs is predicted from the beat-to-beat variation to minimize the search range. We assumed that the maximum rate of the beat-to-beat variation is 25% in this implementation, although it is generally 20% in healthy subjects [21]. The prediction result is used to maximize the sleep time of the ADC and heartbeat detector. Even in cases where misdetection or false detection occurs because of arrhythmia or intense noise, the heartbeat detector can awaken and recover from the error because the coefficient of autocorrelation will decrease rapidly if such an error occurs. Whenever the QRS complex is detected at t_{QRS}, the QRS complex template (TM) is updated by adding the detected QRS complex to the previous template (TM_{prev}) as shown below.

$$TM[i] = \frac{7 \cdot TM_{\text{prev}}[i] + d[t_{\text{QRS}}[n] + i]}{8} \quad (-\frac{L_{sw}}{2} \le i \le \frac{L_{sw}}{2}) \tag{8}$$

B. Performance evaluation of heartbeat detection

First, we investigated the success rate of heart rate extraction using 48 records from the MIT-BIH arrhythmia database [22]. The proposed method is modeled using MATLAB. Table 2 presents the simulation results. Here, the definition of sensitivity (Se) is TP / (TP + FN). The definition of positive predictivity (+P) is TP / (TP + FP). Then, TP, FN, and FP respectively denote the number of correct QRS complex detection, the number of failures to detect the true QRS complex, and the number of false detections. The success rate denotes the heart rate extraction success rate every second. Then the recent beat-to-beat interval is compared with a database every second.

Comparison with the conventional algorithms [6–15] showed no significant difference in the simulation result with most records. Table 3 shows the success rate comparison with proposed method and conventional algorithms of QSW and CWT [13–15]. However, the success rate was degraded for several records because a certain type of arrhythmia, which has irregular heartbeat waveform (e.g. premature ventricular contraction), increases misdetection. Table 4 shows that, although the proposed method shows equivalent or better performance in most cases, it is degraded by such arrhythmia because the algorithm uses similarity of the QRS waveform.

Next, we evaluated the noise tolerance using the MIT-BIH noise stress test database [23]. To evaluate the heartbeat extraction performance in noisy conditions, the proposed method and the conventional QSW, Quad Level Vector (QLV) [12], Continuous Wavelet Transform (CWT) [13–15], and STAC [19] are modeled using MATLAB. The QSW has been used in robust ECG monitoring LSIs [11, 24, 25]. The threshold is calculated using the root mean square value of the wavelet transform. The QLV is implemented in dedicated hardware for ECG monitoring LSI [26, 27]. The QLV is generated using

TABLE II
QRS DETECTION PERFORMANCE AND HEART RATE EXTRACTION SUCCESS RATE (SR) OF PROPOSED HEARTBEAT DETECTOR WITH 48 CLEAN ECG RECORDS

Record	Se [%]	+P [%]	SR [%]	Record	Se [%]	+P [%]	SR [%]
100	99.8	100.0	100.0	202	91.6	99.4	95.3
101	99.7	99.9	99.7	203	69.4	98.5	70.7
102	93.0	93.4	93.0	205	84.2	100.0	82.0
103	99.8	100.0	100.0	207	84.1	93.2	88.3
104	97.1	99.4	98.6	208	74.2	89.8	55.1
105	97.0	99.3	97.3	209	99.7	100.0	100.0
106	77.7	98.9	92.6	210	86.9	99.9	91.8
107	97.5	99.1	97.5	212	99.9	100.0	100.0
108	94.9	95.9	80.4	213	87.8	99.4	83.5
109	99.0	100.0	99.0	214	91.8	99.6	96.9
111	99.7	99.9	96.3	215	91.5	100.0	92.4
112	99.9	100.0	100.0	217	98.8	99.7	92.4
113	99.6	100.0	99.9	219	92.8	97.6	94.6
114	98.1	99.8	97.8	220	98.1	100.0	99.1
115	99.9	100.0	100.0	221	76.1	99.6	85.1
116	99.0	98.1	97.0	222	84.3	99.2	89.9
117	99.9	100.0	95.2	223	85.7	100.0	84.0
118	99.6	100.0	99.4	228	86.8	98.3	96.3
119	78.0	99.0	96.8	230	99.9	100.0	99.9
121	99.6	99.6	99.6	231	87.1	79.4	74.8
122	99.8	100.0	100.0	232	90.1	77.4	61.3
123	99.3	99.6	99.4	233	76.6	99.9	67.2
124	99.1	100.0	99.7	234	78.6	100.0	73.0
200	76.9	99.8	64.2	Avg.	91.8	98.1	90.9
201	87.4	95.5	88.2				

TABLE III
COMPARISON OF HEART RATE EXTRACTION SUCCESS RATE

Record	Success rate [%]			Record	Success rate [%]		
	QSW	CWT	Prop.		QSW	CWT	Prop.
100	96.9	98.8	100.0	202	98.5	95.4	95.3
101	96.1	98.4	99.7	203	59.4	81.1	70.7
102	87.9	95.5	93.0	205	98.7	98.9	82.0
103	99.4	98.9	100.0	207	80.2	86.7	88.3
104	55.5	80.5	98.6	208	62.4	35.3	55.1
105	92.1	97.1	97.3	209	95.7	98.5	100.0
106	85.1	88.3	92.6	210	91.0	86.3	91.8
107	77.8	97.7	97.5	212	96.4	99.2	100.0
108	48.3	86.4	80.4	213	92.3	92.6	83.5
109	96.8	98.1	99.0	214	95.3	96.7	96.9
111	65.6	96.6	96.3	215	95.8	93.8	92.4
112	98.1	98.7	100.0	217	68.6	87.1	92.4
113	99.3	98.2	99.9	219	94.8	92.9	94.6
114	95.2	99.2	97.8	220	99.1	98.8	99.1
115	98.6	98.3	100.0	221	97.0	84.4	85.1
116	96.4	97.8	97.0	222	77.2	87.8	89.9
117	94.8	68.6	95.2	223	97.1	83.7	84.0
118	90.1	97.8	99.4	228	67.5	69.7	96.3
119	80.2	94.0	96.8	230	98.3	98.4	99.9
121	96.3	99.2	99.6	231	71.8	98.6	74.8
122	99.3	99.0	100.0	232	95.4	89.5	61.3
123	99.2	98.5	99.4	233	68.1	86.5	67.2
124	56.5	96.5	99.7	234	99.3	98.7	73.0
200	88.7	96.0	64.2	Avg.	86.9	91.6	90.9
201	77.1	79.7	88.2				

TABLE IV
SUCCESS RATE AND ARRHYTHMIA TYPE IN 48 RECORDS

Type of arrhythmia	# of beats	Success rate [%]		
		QSW	CWT	Prop.
Normal beat	52927	93.18	96.16	94.86
Left bundle branch block beat	6372	82.42	97.65	98.40
Right bundle branch block beat	6366	74.55	96.26	94.49
Atrial premature beat	2588	92.31	93.59	82.88
Aberrated atrial premature beat	258	58.53	33.72	38.76
Nodal (junctional) premature beat	64	68.75	95.31	98.44
Premature ventricular contraction	9847	62.96	63.18	42.77
Fusion of ventricular and normal beat	715	84.90	92.31	80.84
Atrial escape beat	21	100.00	90.48	95.24
Nodal (junctional) escape beat	252	82.94	92.46	90.87
Ventricular escape beat	108	87.96	92.59	93.52
Paced beat	5880	71.04	92.45	96.46
Fusion of paced and normal beat	854	56.91	76.93	88.52
Unclassifiable beat	35	8.57	57.14	71.43
Ventricular flutter wave	147	14.29	26.53	38.10

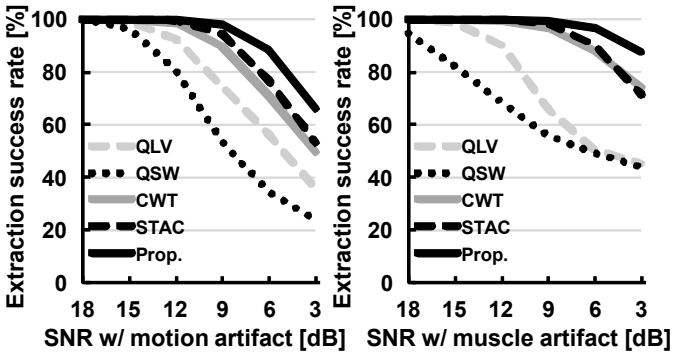


Fig. 12. Noise stress test (MIT-BIH record #100).

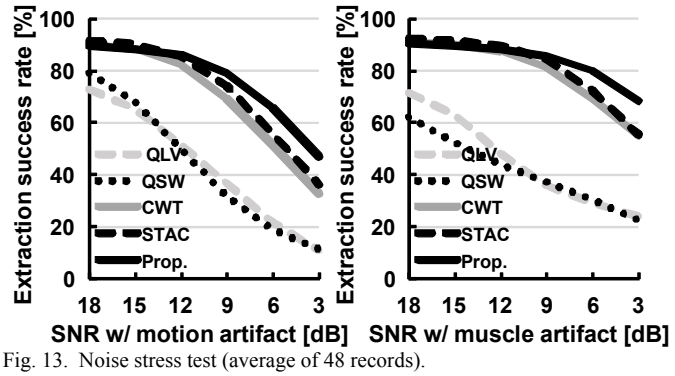


Fig. 13. Noise stress test (average of 48 records).

DWT and the adaptive threshold. Then, the threshold is ascertained from the maximum mean deviation (MD) of the previous heartbeats. The CWT employs a Mexican hat wavelet in the frequency interval of 15–18 Hz. The R-peak can be extracted using the adaptive threshold, which is calculated using the modulus maxima of the CWT. This algorithm was implemented in an earlier study [27].

Figs. 12 and 13 portray the relation between the noise intensity and the heart rate detection success rate. A muscle artifact and motion artifact records are used because these noises have critical frequency characteristics. We used the muscle artifact and the motion artifact databases from MIT-BIH noise stress test database [23]. Then, the signal-to-noise ratio (SNR) is defined as shown below.

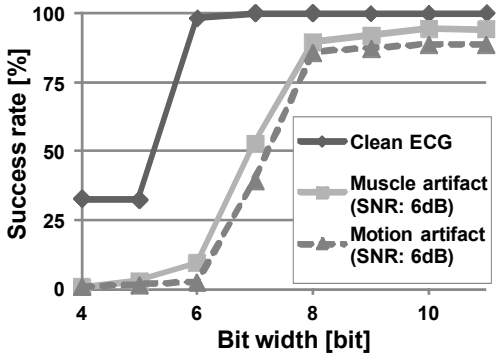


Fig. 14. Bit width of ECG signal versus extraction success rate from record #100 with and without 6-dB noises. The sampling rate is set to 128 samples/s.

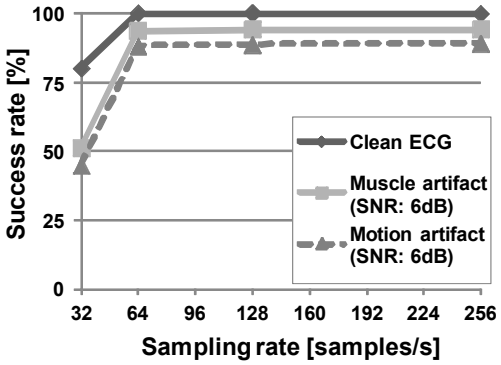


Fig. 15. Sampling rate of ECG signal versus extraction success rate from record #100 with and without 6-dB noises. The bit width is set to eight bits.

$$SNR = 10\log\frac{S}{N \times a^2} \tag{9}$$

Here, S, N, and a respectively denote the signal power, frequency-weighted noise power, and scale factor. Simulation results show that the proposed algorithm has better noise tolerance in each condition.

In Fig. 12, MIT-BIH record #100 is used to evaluate the effect of noise contamination and to eliminate the effect of arrhythmia because this record includes a few arrhythmic beats. In Fig. 13, all 48 records from MIT-BIH are used. These results show that proposed method can improve the noise tolerance compared with conventional algorithms when the ECG is contaminated by both a muscle artifact and a motion artifact.

Finally, we evaluate the required resolution of the ECG signal to minimize the computational amount and the hardware overhead because the battery capacity is strictly limited in our target application. The bit width and the sampling rate of ECG signal directly affect the overhead. Fig. 14 presents the effect of bit width with record #100 with and without 6-dB noises. Then, the sampling rate of the ECG signal is fixed to 128 samples/s. The simulation result shows that the success rate is degraded when the bit width is less than eight in noisy conditions. Fig. 15 portrays the effects of sampling rate differences. The bit width is fixed to eight bits in this simulation. Simulation results show that a 64 samples/s or more sampling rate is needed for heart rate extraction without degradation.

C. Hardware implementation of the heartbeat detector

The proposed method is implemented as dedicated hardware

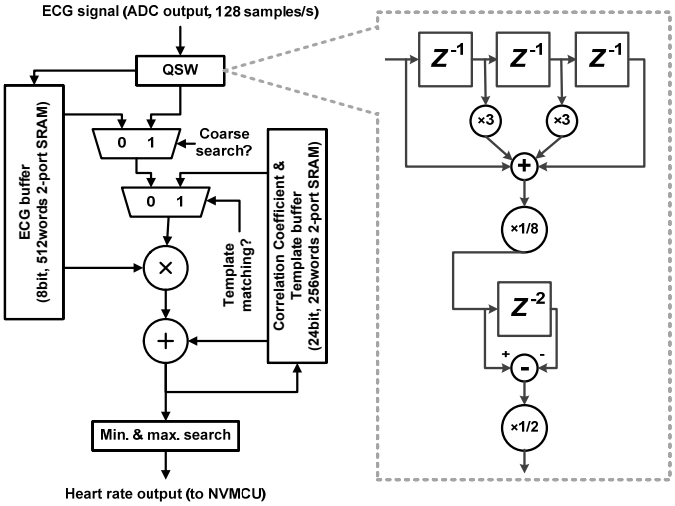


Fig. 16. Block diagram of heartbeat detector.

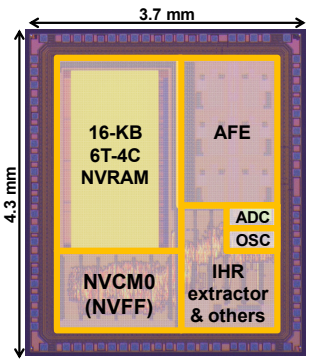
to minimize the power overhead. Fig. 16 presents a block diagram of the heartbeat detector, which consists of dual port SRAMs, registers, and accumulators. As presented in Fig. 16, the hardware resources are shared in both the coarse-fine QRS search state and the template matching state. Therefore, the capacity and the stand-by current of SRAMs can be minimized. The bit-width reduction according to the simulation result of Fig. 14 also reduces hardware overhead.

The required operating frequency to realize the real-time heartbeat detection is less than 32 kHz when applying the 128-samples/s sampling rate according to the evaluation result of Fig. 15. Therefore, this heartbeat detection block can operate using only 32.768-kHz real-time clocks. The real-time clock is a necessary component of a wearable monitoring system and it has low power consumption.

IV. Implementation Result

The 3.7 × 4.3 mm^2 test chip is fabricated using 0.13 µm CMOS technology. Fig. 17 depicts the chip micrograph and a performance summary. The operating voltage is 1.2 V for the AFE, the ADC, the 24-MHz oscillator, the heartbeat detector, NVMCU, and other digital blocks. Only the 32-kHz oscillator and IO circuits are operated with 3.0V supply voltage.

First, we evaluated the performance of NVRAM and NVMCU. As presented in Fig. 18, the energy consumption of the 6T-4C NVRAM in store, recall, write, and read operations are reduced respectively by 22%, 11%, 74%, and 77% by virtue of the charge sharing and pre-charge-less techniques. In bit-line equalization, some power dissipation overhead exists in the memory cell power supply. Nevertheless, the total power consumption of read and write operations can be reduced. The power during plate-line equalization can be negligible because the plate-lines are connected only to ferroelectric capacitors. The plate-line driver is isolated from plate-lines during equalization. The measurement results show that the operating frequency of read and write operations is 47 MHz at maximum. However, the store and recall operations require at least 40-ns cycle time, as presented in Fig. 19. Therefore, the maximum operating frequency of NVRAM is 24 MHz, which complies



Technology		0.13 µm CMOS
Supply voltage		1.2 V (AFE, ADC, Logic, Memory)
		3.0 V (32.768-kHz OSC and I/O)
Chip area		3.7×4.3 mm^2
Frequency		24 MHz (for processor)
		32 kHz (for other blocks)
Processor		32-bit Cortex M0 (with NVFF)
On chip memory		16-KByte 6T-4C NVRAM
AFE	Gain	54 dB
	Bandwidth	700 Hz
	CMRR	73 dB
ADC	Resolution	8 bit
	Current	0.23 µA@128 S/s, 1.0 µA@1 kS/s

Fig. 17. Chip micrograph and chip specifications.

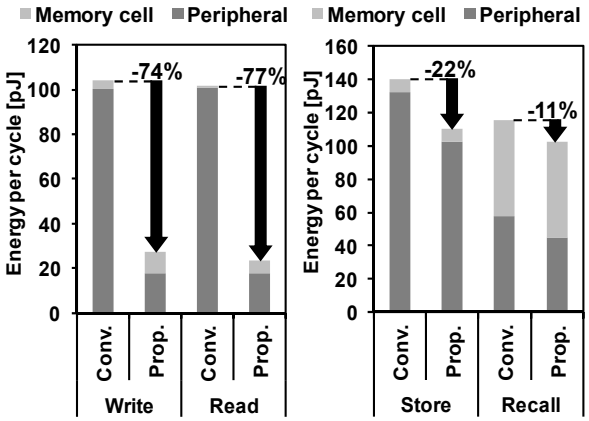


Fig. 18. Measured energy consumption of 6T-4C NVRAM with and without proposed methods.

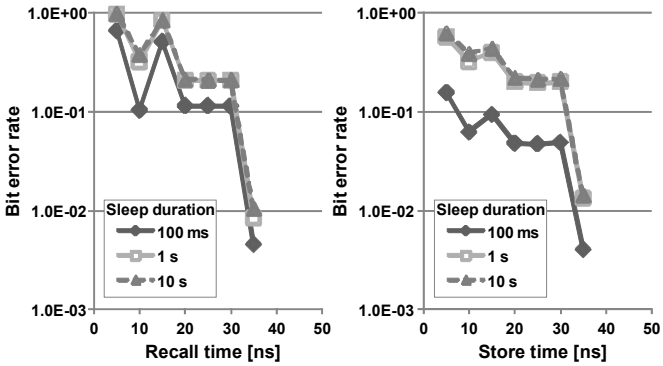


Fig. 19. Measured bit error rate of 16-Kbyte NVRAM.

with the NVMCU operating frequency.

Next, to demonstrate the test chip performance, we implemented a heart rate logging application. Fig. 20 shows the measured waveforms of the heart rate extraction. The measurement results show that the heart rate is extracted correctly even in a noisy condition, and especially not at rest.

Fig. 21 shows the summary of current consumptions in each block with heart rate logging application. Then, the ADC sampling rate is set to 128 Hz. The heartbeat detector output is stored to data memory every second. The AFE, 32-kHz OSC, and timer block are always activated. The total current consumption is 6.14 µA on average, including 1.28-µA non-volatile MCU and 0.7-µA heartbeat detector. As presented in Fig. 22, the proposed heart rate extractor has higher noise tolerance and minimum power overhead compared with previous studies of hardware implemented heartbeat detector

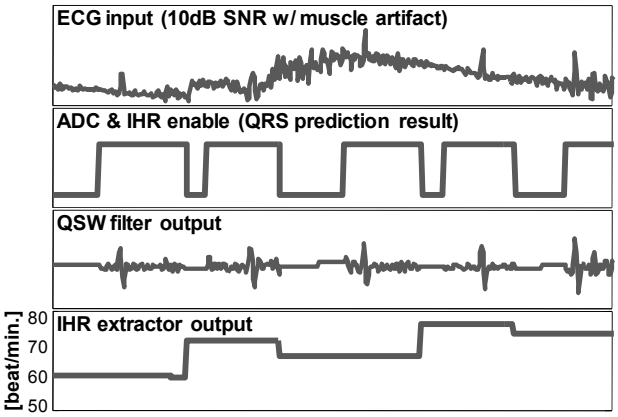


Fig. 20. Input ECG waveform and measurement results of QRS prediction, filter output and extracted IHR.

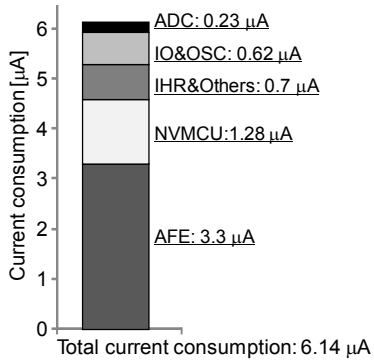


Fig. 21. Total current consumption for heart rate logging application.

[25, 27, 28]

Table 5 presents a comparison with other recently published ECG monitoring SoCs [25, 28–31]. The proposed SoC has the lower power consumption in fully integrated (with AFE, ADC, digital filter, non-volatile MCU, OSC, and communication I/F) ECG sensors for daily life monitoring.

Fig. 23 portrays the application board of the proposed wearable sensor system. The board size is 22.5 mm × 28.5 mm. A near field communication (NFC) Tag IC is used to communicate with a smartphone. The proposed system weighs 3.9 g including the NFC tag IC, linear regulator, 32.768-kHz crystal oscillator, and a 1.0 g battery, which has 35mAh capacity.

To evaluate the accuracy of extracted heartbeats, measurement results obtained using the proposed sensor are compared with those of the reference sensor (CamNtech Actiwave Cardio [32]). The proposed sensor and reference sensor record the ECG signal and heart rate simultaneously as depicted in Fig. 24.

In Fig. 25, the heart rate output of the proposed sensor is compared with the reference sensor. This result demonstrates that the proposed system can extract the heart rate correctly, although the electrode distance and the SNR of ECG are limited.

V. Conclusion

We proposed the ECG-SoC using the noise-tolerant heartbeat detector and NVMCU in 0.13 μm CMOS. The heartbeat detector uses short-term autocorrelation and a template matching algorithm for noisy conditions in wearable systems. The NVMCU consists of 16-Kbyte 6T-4C NVRAM and Cortex M0 core with ferroelectric-based nonvolatile FFs. The 3.7 × 4.3 mm^2 ASIC consumes 6.14 μA for heart rate extraction and logging application. The proposed heartbeat detector achieves state-of-the-art noise tolerance and power consumption. This result demonstrates that it accommodates the performance requirements for analog front end and electrodes.

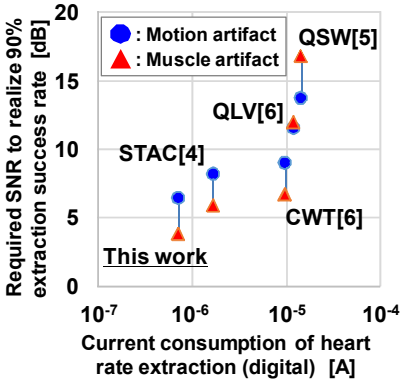


Fig. 22. Performance comparison of heart beat detector with previous studies.

TABLE V
Performance Comparison of ECG SoC

	This work	VLSI'14 [29]	A-SSCC'13 [30]	ESSCIRC'13 [28]	VLSI'13 [25]	ISSCC'13 [31]
Technology	0.13 μm	0.13 μm	0.35 μm	0.13 μm	0.13 μm	0.18 μm
Supply voltage	1.2 V / 3.0 V	1.0 V	2.4-3.0 V	1.2V / 3.0 V	0.5-1.0 V	1.8 V / 3.2 V
Frequency	32.768 kHz, 24 MHz	200 kHz, 48 MHz	32.768 kHz	32.768 kHz, 24 MHz	8-32 kHz, 24 / 40 MHz	20 kHz
MCU	32b NVCM0	MSP430L092 (off chip)	n/a	32b CM0	32b Andes N9	n/a
On-chip memory	16 kB NVRAM	n/a	n/a	129.75 kB	20.5 kB	n/a
Total power for HR logging	8.47 μW	95 μW	9.6-12 μW	18.24 μW	16.1 μW	18.7 μW
Total current for HR logging	6.14 μA	95 μA	4.0 μA	13.7 μA	>16.1 μA	10.41 μA

References

[1] H. Nakajima, T. Shiga, and Y. Hata, "Systems Health Care," *Proc. of IEEE SMC*, pp. 1167–1172, Oct. 2011.

[2] S. Izumi, K. Yamashita, M. Nakano, T. Nakagawa, Y. Kitahara, K. Yanagida, S. Yoshimoto, H. Kawaguchi, H. Kimura, K. Marumoto, T. Fuchikami, Y. Fujimori, H. Nakajima, T. Shiga, and M. Yoshimoto, "A 6.14μA Normally-Off ECG-SoC with Noise Tolerant Heart Rate Extractor for Wearable Healthcare Systems," *Proc. of IEEE BioCAS*, pp. 280–283, Oct. 2014.

[3] H. Kimura, Z. Zhong, Y. Mizuochi, N. Kinouchi, Y. Ichida, and Y. Fujimori, "Highly reliable non-volatile logic circuit technology and its application," *Proc. of IEEE ISMVL*, pp. 212–218, May 2013.

[4] H. Kimura, T. Fuchikami, K. Marumoto, Y. Fujimori, S. Izumi, H. Kawaguchi, and M. Yoshimoto, "A 2.4 pJ Ferroelectric-Based Non-Volatile Flip-Flop with 10-Year Data Retention Capability," *Proc. of IEEE A-SSCC*, Nov. 2014.

[5] S. Masui, W. Yokozeki, M. Oura, T. Ninomiya, K. Mukaida, Y. Takayama, and T. Teramoto, "Design and applications of ferroelectric nonvolatile SRAM and Flip-FF with unlimited read, program cycles and stable recall," *Proc. of IEEE CICC*, pp. 403–406, 2003.

[6] J. Pan, W. J. Tompkins, "A Real-Time QRS Detection Algorithm," *IEEE Trans. Biomed. Eng.*, vol. BME-32, no. 3, pp. 230–236, Mar. 1985.

[7] PhysioNet WFDB Applications, sqrs, "http://www.physionet.org/physiotools/wag/sqrs-1.htm"

[8] PhysioNet WFDB Applications, wqrs, "http://www.physionet.org/physiotools/wag/wqrs-1.htm"

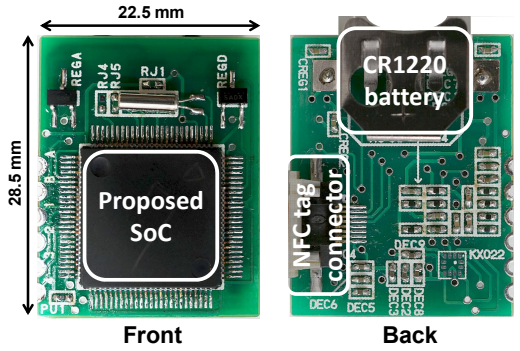


Fig. 23. Application board for the proposed sensor.

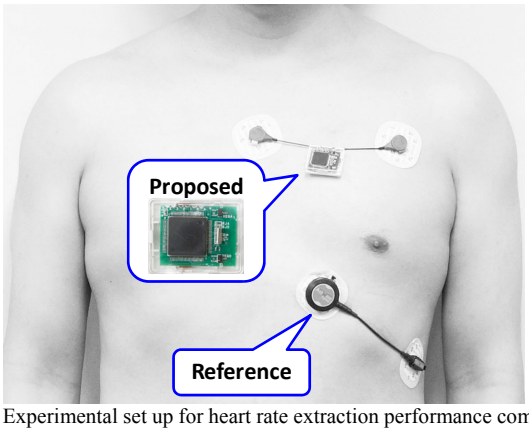


Fig. 24. Experimental set up for heart rate extraction performance comparison.

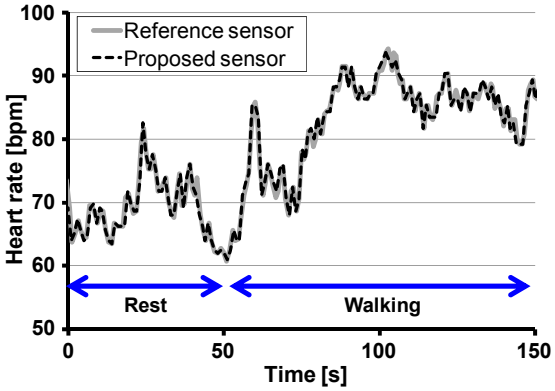


Fig. 25. Comparison of measured heart beat using proposed sensor and reference sensor [32].

[9] C. Li, C. Zheng, C. Tai, "Detection of ECG characteristic points using wavelet transforms," *IEEE Trans. Biomed. Eng.*, vol. 42, no. 1, pp. 21–28, Jan. 1995.

[10] J. P. Martinez, R. Almeida, S. Olmos, A. P. Rocha, and P. Laguna, "A wavelet-based ECG delineator: evaluation on standard databases," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 4, pp. 570–581, Apr. 2004.

[11] S. Y. Hsu, Y. L. Chen, P. Y. Chang, J. Y. Yu, T. F. Yang, R. J. Chen, and C. Y. Lee, "A micropower biomedical signal processor for mobile healthcare applications," *Proc. of IEEE A-SSCC*, pp. 301–304, Nov. 2011.

[12] H. Kim, R. F. Yazicioglu, P. Merken, C. V. Hoof, and H. J. Yoo, "ECG Signal Compression and Classification Algorithm With Quad Level Vector for ECG Holter System," *IEEE Trans. Information Technology in Biomedicine*, vol. 14, no. 1, pp. 93–100, Jan. 2010.

[13] I. Romero, P. S. Addison, M. J. Reed, N. Grubb, G. R. Clegg, C. E. Robertson, and J. N. Watson, "Continuous Wavelet Transform Modulus Maxima Analysis of the Electrocardiogram: Beat Characterisation and Beat-to-Beat Measurement," *Int. J. Wavelets Multiresolut Inf. Process 3*, no. 1, pp. 19–42, 2005.

[14] I. Romero, B. Grundlehner, J. Penders, "Robust beat detector for ambulatory cardiac monitoring," *Proc. of IEEE EMBC*. Annual International Conference, pp. 950–953, Sep. 2009.

[15] I. Romero, B. Grundlehner, J. Penders, J. Huisken, and Y. H. Yassin, "Low-power robust beat detection in ambulatory cardiac monitoring," *Proc. of IEEE BioCAS*, pp. 249–252, Nov. 2009.

[16] Y. Takeuchi, M. Hogaki, "An adaptive correlation rate meter: a new method for Doppler fetal heart rate measurements," *Ultrasonics*, pp. 127–137, May 1978.

[17] M. Sekine, K. Maeno, "Non-Contact Heart Rate Detection Using Periodic Variation in Doppler Frequency," *Proc. of IEEE SAS*, pp. 318–322, Feb. 2011.

[18] H. L. Chan, G. U. Chen, M. A. Lin, and S. C. Fang, "Heartbeat Detection Using Energy Thresholding and Template Match," *Proc. of IEEE EMBC*, pp. 6668–6670, Aug. 2005.

[19] M. Nakano, T. Konishi, S. Izumi, H. Kawaguchi, and M. Yoshimoto, "Instantaneous Heart Rate detection using short-time autocorrelation for wearable healthcare systems," *Proc. of IEEE EMBC*, pp. 6703–6706, Aug. 2012.

[20] Y. Nakai, S. Izumi, M. Nakano, K. Yamashita, T. Fujii, H. Kawaguchi, M. Yoshimoto, "Noise Tolerant QRS Detection using Template Matching with Short-Term Autocorrelation," *Proc. of IEEE EMBC*, pp. 34–37, Aug. 2014.

[21] M. Malik, "Heart Rate Variability; standards of Measurement, Physiological Interpretation, and Clinical Use," *Circulation*, 1996; 93: 1043–1065.

[22] MIT-BIH Arrhythmia Database(mitdb), "http://www.physionet.org/physiobank/database/mitdb/"

[23] MIT-BIH Noise Stress Test Database(nstdb), "http://www.physionet.org/physiobank/database/nstdb/"

[24] S. Y. Hsu, Y. Ho, Y. Tseng, T. Y. Lin, P. Y. Chang, J. W. Lee, J. H. Hsiao, S. M. Chuang, T. Z. Yang, P. C. Liu, T. F. Yang, R. J. Chen, C. Su, and C. Y. Lee, "A sub-100μW multi-functional cardiac signal processor for mobile healthcare applications," *IEEE Symp. VLSI Circuits*, pp. 156–157, Jun. 2012.

[25] S. Y. Hsu, Y. Ho, P. Y. Chang, P. Y. Hsu, C. Y. Yu, Y. Tseng, T. Z. Yang, T. F. Yang, R. J. Chen, C. Su, and C. Y. Lee, "A 48.6-to-105.2μW Machine-Learning Assisted Cardiac Sensor SoC for Mobile Healthcare Monitoring," *IEEE Symp. VLSI Circuits*, pp. 252–253, Jun. 2013.

[26] H. Kim, R. F. Yazicioglu, T. Torfs, P. Merken, H. J. Yoo, and C. V. Hoof, "A low power ECG signal processor for ambulatory arrhythmia monitoring system," *IEEE Symp. VLSI Circuits*, pp. 19–20, Jun. 2010.

[27] H. Kim, R. F. Yazicioglu, S. Kim, N. V. Helleputte, A. Artes, M. Konijnenburg, J. Huisken, J. Penders, and C. V. Hoof, "A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications," *IEEE Symp. VLSI Circuits*, pp. 142–143, Jun. 2011.

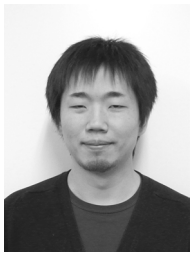
[28] S. Izumi, K. Yamashita, M. Nakano, H. Kawaguchi, H. Kimura, K. Marumoto, T. Fuchikami, Y. Fujimori, H. Nakajima, T. Shiga, and M. Yoshimoto, "A Wearable Healthcare System with a 13.7 μA Noise Tolerant ECG Processor," *IEEE Trans. BioCAS*, Nov. 2014. (to be published, DOI: 10.1109/TBCAS.2014.2362307)

[29] T. Morrison, J. Silver, and B. Otis, "A single-chip encrypted wireless 12-lead ECG smart shirt for continuous health monitoring," *IEEE Symp. VLSI Circuits*, pp. 1–2, June 2014.

[30] C.J. Deepu, X. Zhang, W.S. Liew, D.L.T. Wong, and Y. Lian, "An ECG-SoC with 535nW/channel lossless data compression for wearable sensors," *Proc. of IEEE A-SSCC*, pp. 145–148. Nov. 2013.

[31] S. Kim, L. Yan, S. Mitra, M. Osawa, Y. Harada, K. Tamiya, C. van Hoof, R. Yazicioglu, "A 20μW Intra-Cardiac Signal-Processing IC with 82dB Bio-Impedance Measurement Dynamic Range and Analog Feature Extraction for Ventricular Fibrillation Detection," *ISSCC Dig. Tech.Papers*, pp. 302–303, Feb. 2013.

[32] CamNtech Actiwave Cardio Overview, "http://www.camntech.com/products/actiwave-cardio/actiwave-cardio-overview"

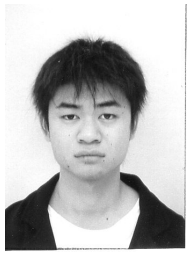


Shintaro Izumi (S'09–M'12) respectively received his B.Eng. and M.Eng. degrees in Computer Science and Systems Engineering from Kobe University, Hyogo, Japan, in 2007 and 2008. He received his Ph.D. degree in Engineering from Kobe University in 2011. He was a JSPS research fellow at Kobe University from 2009 to 2011. Since 2011, he has been an Assistant Professor in the Organization of Advanced Science and Technology at Kobe University. His current research interests include biomedical signal processing, communication protocols, low-power VLSI design, and sensor networks.
He has served as a Vice Chair of IEEE Kansai Section Young Professional Affinity Group, as a Student Activity Committee Member for IEEE Kansai Section, as a Program Committee Member for IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences. He was a recipient of 2010 IEEE SSCS Japan Chapter Young Researchers Award.

Ken Yamashita received his B.Eng. degree in Informatics from Sizuoka University, Sizuoka, Japan, in 2012, and M.Eng. degree in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2014. His current research is related to wearable health-care systems.

Masanao Nakano respectively received his B.Eng. and M.Eng. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2012 and 2014. His current research is related to wearable health-care systems.

Shusuke Yoshimoto (S'11–M'13) received B.E. and M.E. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2009 and 2011, respectively. He earned Ph.D. degree in Engineering from the university in 2013. He was a JSPS research fellow from 2013 to 2014. He worked in Department of Electrical Engineering at Stanford University as a postdoctoral from 2013 to 2015. Since 2015, he has been an Assistant Professor in The Institute of Scientific and Industrial Research at Osaka University. His current research interests include biomedical signal processing, flexible electronics, organic circuit design, nano-electronics, soft error, low-power and robust memory design. He was a recipient of 2011 and 2012 IEEE SSCS Japan Chapter Academic Research Awards, 2013 IEEE SSCS Kansai Chapter IMFEDK Student Paper Award, and 2013 Intel/Analog Devices/Catalyst Foundation/Cirrus Logic CICC Student Scholarship Award. He has served as a program committee student member in IEICE Integrated Circuit Design.



Tomoki Nakagawa respectively received his B.Eng. and M.Eng. degrees in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2013 and 2015. His current research is low-power FeRAM designs.

Yozaburo Nakai received his B.Eng. degree in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2014. Currently, he is a master course student at Kobe University. His current research is related to wearable health-care systems.

Hiroshi Kawaguchi (M'98) received B.Eng. and M.Eng. degrees in electronic engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and earned a Ph.D. degree in Engineering from The University of Tokyo, Tokyo, Japan, in 2006.

He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to The Institute of Industrial Science, The University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with The Department of Information Science at that university. He is also a Collaborative Researcher with The Institute of Industrial Science, The University of Tokyo. His current research interests include low-voltage SRAM, RF circuits, and ubiquitous sensor networks.

Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Program Committee Member for IEEE Custom Integrated Circuits Conference (CICC) and IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as a Guest Associate

Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM).

Hiromitsu Kimura (M'99) received the B.E. degree in Electrical Engineering from Tohoku University, Sendai, Japan, in 1998 and the Master of Information Science and Doctor of Information Science degrees in Computer and Mathematical Sciences from Tohoku University in 2000 and 2003, respectively.

He is currently a Senior Engineer of ROHM Co. Ltd., Japan. His main interests and activities are in the areas of Ferroelectric random access memory (FeRAM) and non-volatile logic LSI.

Dr. Kimura received the Judge's Special Award at the 9th LSI Design of the Year from the Semiconductor Industry News of Japan in 2002 and the Grand Award at IEEE International Meeting for Future of Electron Devices, Kansai in 2006. Dr. Kimura is a member of the IEEE.

Kyoji Marumoto has been working on ROHM Co., Ltd., Kyoto, Japan.

Takaaki Fuchikami has been working on LSI Product Development Headquarters Core Technology Development Division, ROHM Co., Ltd., Kyoto, Japan.

Yoshikazu Fujimori (M'03) received the B.E. and M.E. degrees in electronics engineering from Kyoto University, Kyoto, Japan. In 1996, he joined ROHM Co. Ltd., Kyoto, Japan, where he has been working on device and process development of Ferroelectric Random Access Memory (FeRAM). He received the degree of Doctor of Engineering from Kyoto University in 2005. His research interests include low power and functional applications of non-volatile ferroelectric devices and piezoelectric devices.

Hiroshi Nakajima (M'97) received the B.Eng. degree in System Engineering from Kobe University, Japan, in 1985, and Ph.D. degree in Systems Information Science from Kumamoto University, Japan, in 2004. He is currently Chief Specialist of Technology at Omron Corporation. Besides long term career at industry, he also has some academic careers such as visiting professor at Kyushu Institute of Technology. He has focused on the general solution for improvement of health in humans, machines, and energy consumptions by applying sensory inspection and computational intelligence. He received the best paper award from Interaction'99 in 1999, the best author award from Information Processing Society of Japan in 2000, the Industrial Outstanding Application Award from International Fuzzy Systems Association in 2007, the best paper award from Japan Society for Fuzzy Theory and Intelligent Informatics in 2009, and Biomedical Wellness Award from SPIE in 2011.

Toshikazu Shiga received the B.S. degree in 1982 from Yamaguchi University, Yamaguchi Japan in electrical engineering, the M.S. degree in 1986 from Hokkaido University, Hokkaido Japan, and Ph.D. degree in 1998 from Hokkaido University, Hokkaido Japan, both in biomedical engineering. In April 1986, he was joined the research and development division of Omron Healthcare Co, ltd. His areas of research interest are the measurement of biological signal and all biomedical engineering.

Masahiko Yoshimoto (M'98) joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in 1977. From 1978 to1983 he had been engaged in the design of NMOS and CMOS static RAM. Since 1984 he had been involved in the research and development of multimedia ULSI systems. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. Since 2000, he had been a professor of Dept. of Electrical & Electronic System Engineering in Kanazawa University, Japan. Since 2004, he has been a professor of Dept. of Computer and Systems Engineering in Kobe University, Japan. His current activity is focused on the research and development of an ultra low power multimedia and ubiquitous media VLSI systems and a dependable SRAM circuit. He holds on 70 registered patents.

He has served on the program committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. Also he served as Guest Editor for special issues on Low-Power System LSI, IP and Related Technologies of IEICE Transactions in 2004. He was a chair of IEEE SSCS (Solid State Circuits Society) Kansai Chapter from 2009 to 2010. He is also a chair of The IEICE Electronics Society Technical Committee on Integrated Circuits and Devices from 2011-2012. He received the R&D100 awards from the R&D magazine for the development of the DISP and the development of the realtime MPEG2 video encoder chipset in 1990 and 1996, respectively. He also received 21th TELECOM System Technology Award in 2006.