PAPER Special Section on Design Methodologies for System on a Chip

Low-Jitter Design for Second-Order Time-to-Digital Converter Using Frequency Shift Oscillators*

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SUMMARY We present a low-jitter design for a 10-bit second-order frequency shift oscillator time-to-digital converter (FSOTDC). As described herein, we analyze the relation between performance and FSOTDC parameters and provide insight to support the design of the FSOTDC. Results show that an oscillator jitter limits the FSOTDC resolution, particularly during the first stage. To estimate and design an FSOTDC, the frequency shift oscillator requires an inverter of a certain size. In a standard 65-nm CMOS process, an SNDR of 64 dB is achievable at an input signal frequency of 10 kHz and a sampling clock of 2 MHz. Measurements of the test chip confirmed that the measurements match the analyses.

key words: *TDC, FSO, jitter, design methodology*

1. Introduction

Time-to-digital converters (TDCs), which digitalize a time interval, are used in all-digital phase locked loops (ADPLLs) and analog-to-digital converters (ADCs). The time-domain ADC using the TDC can be configured using digital circuits. Therefore, they can be extended easily to advanced CMOS processes. The minimum time resolution of the state-of-the art TDC is 180 fs [2]. The TDC, which can be realized in a small area and at low cost, requires an external circuit to convert a signal (with analog voltage) to a time-domain signal, although voltage-to-time converters reportedly achieve good linearity [1]. The combination of the TDC and voltage-to-time converter can produce a high-performance ADC that uses a small area. To obtain the small area and high resolution, the proposed TDC consists of a pair of inverter rings as oscillators. The oscillators are called frequency-shift oscillators that output either low frequency or high frequency on demand [3]. The second-order frequency shift oscillator TDC (FSOTDC) achieves smaller area with simple architecture.

In the next section, to estimate an FSOTDC resolution, we describe analysis of the factors affecting the FSOTDC performance. Then, simulation results derived from the analyses and measurement results of a test chip are described in Sect. 3. The final section summarizes this paper.

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2. Analyses of Second-Order FSOTDC

Figure 1 portrays the architecture and the timing diagram of the second-order ΔΣ FSOTDC. The first-stage FSOTDC converts an input time at the N-th sample ($T_{IN1}[N]$) to a digital value ($D_1[N]$) using an FSO, which oscillates at a low frequency or high frequency (F_{A1} or F_{B1}) depending on $T_{IN1}[N]$ (F_{A1} when $T_{IN1}[N]$ = "High"; F_{B1} when $T_{IN1}[N]$ = "Low"). Consequently, $D_1[N]$ signifies the total oscillation count during a sampling period (T_{CK}). $J_{CK}[N]$ and $J_{TIN}[N]$ are jitters in a clock period and an input signal. $D_{B1}[N]$ is a digital value corresponding to $T_{CK} - T_{IN1}[N]$. $J_{A1\_X}[N]$ ($X = 1, 2, \ldots$) and $J_{B1\_X}[N]$ ($X = 1, 2, \ldots$) represent timing jitters at the respective oscillation frequencies of F_{A1} and F_{B1}

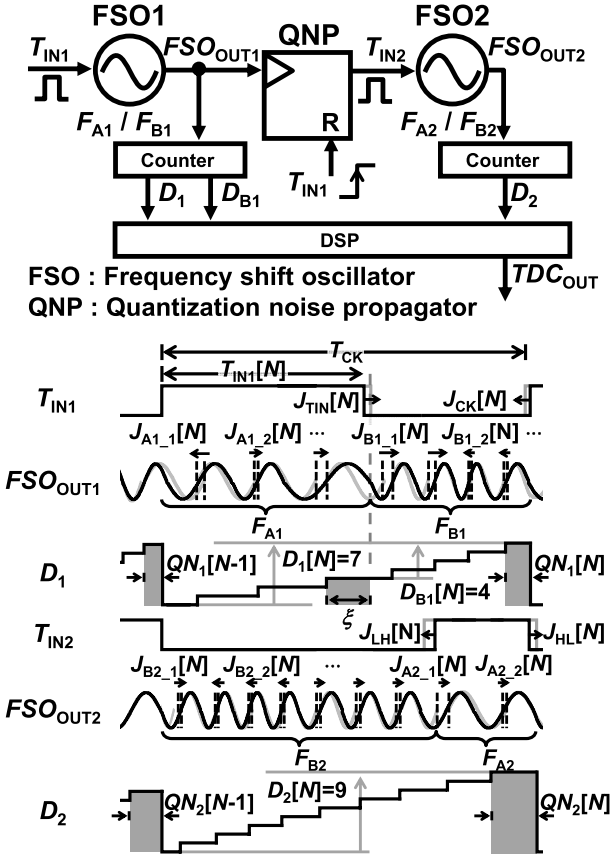

Fig. 1 FSOTDC architecture and timing diagrams.

at the N-th sample. $\Sigma J_{A1}[N]$ and $\Sigma J_{B1}[N]$ respectively denote the sums of $J_{A1\_X}[N]$ and $J_{B1\_X}[N]$. When the jitters are considered, $D_1[N]$ can be derived from [3] as

$$\begin{aligned} D_1[N] = (F_{A1}-F_{B1})\cdot T_{IN1}[N] - F_{B1}\cdot\Delta QN_1 + F_{B1}\cdot T_{CK} \\ + F_{A1}\cdot\sum J_{A1}[N] + F_{B1}\cdot\sum J_{B1}[N] \\ + J_{TIN}[N] + J_{CK}[N], \end{aligned} \tag{1}$$

where Δ is the difference from the previous amount, that is, ΔQN_1 is $QN_1[N]-QN_1[N-1]$. Actually, (1) shows that the first-stage FSOTDC indeed achieves first-order noise shaping if no jitter occurs. To extend it to the second-order TDC, the FSOTDC has a quantization noise propagator (QNP) between the first and second stages, which propagates a quantization noise. The QNP output ($T_{IN2}[N]$) is another input for the second-stage FSO, which includes $QN_1[N]$. $T_{IN2}[N]$, which has timing jitters $J_{LH}[N]$ and $J_{HL}[N]$, is defined as shown below.

$$T_{IN2}[N] = \frac{D_{B1}[N]-3}{F_{B1}} + QN_1[N] + J_{LH}[N] + J_{HL}[N]. \tag{2}$$

In the second stage, the second-stage FSO oscillates at F_{A2} or F_{B2}. $J_{A2\_X}[N]$ and $J_{B2\_x}[N]$ represent timing jitters as well. The second-stage digital output, D_2[N], is represented as

$$\begin{aligned} D_2[N] = (F_{A2}-F_{B2})\cdot T_{IN2}[N] - F_{A2}\cdot\Delta QN_2 + F_{B2}\cdot T_{CK} \\ + F_{A2}\cdot\sum J_{A2}[N] + F_{B2}\cdot\sum J_{B2}[N] \\ + J_{LH}[N] + J_{HL}[N]. \end{aligned} \tag{3}$$

Eventually, from (1), (2), and (3), the final output, $TDC_{OUT}[N]$, including the second-order noise shaping, can be expressed as shown below.

$$\begin{aligned} TDC_{OUT}[N] &= \frac{A_2}{F_{B1}}\cdot D_1[N] + \Delta\left(D_2[N] - \frac{A_2}{F_{B1}}\cdot D_{B1}[N]\right) \\ &= \frac{A_2}{F_{B1}}\Bigg(A_1\cdot T_{IN1}[N] + F_{A1}\cdot\sum J_{A1}[N] \\ &\quad + F_{B1}\cdot\sum J_{B1}[N] + J_{TIN}[N] + J_{CK}[N]) \\ &\quad + F_{B2}\cdot\sum\Delta J_{B2} + F_{A2}\cdot\sum\Delta J_{A2} \\ &\quad + A_2(\Delta J_{HL} + \Delta J_{LH} + T_{CK}) + F_{A2}\cdot\Delta^2 QN_2, \end{aligned} \tag{4}$$

Therein, A_1 and A_2 are constants. In this case, A_1 equals $F_{A1} - F_{B1}$. A_2 equals $F_{A2} - F_{B2}$. A frequency mismatch between the two FSOs can be canceled out using a first-order least mean squares (LMS) filter in the DSP [3].

Equation (4) shows that the timing jitters and the oscillator jitters at the first stage (ΣJ_{A1}, ΣJ_{B1}, J_{TIN} and J_{CK}) are not noise-shaped. They remain as noise sources. Therefore, they affect the resolution of the first- and second-order FSOTDCs directly. These jitters must be reduced for high resolution. Actually, ΔJ_{LH} and ΔJ_{HL} are noise-shaped, so they are cancelled out as noise sources.

2.1 Effect of FSO Jitters (ΣJ_{A1}, ΣJ_{B1})

In this subsection, we present discussion of the effects of the FSO jitters: J_{A1_X}, J_{B1_X}, J_{A2_X}, and J_{B2_X}. The jitters of the second-stage FSO (J_{A2_X} and J_{B2_X}) are first-order noise-shaped, as described above. Therefore, we exclude the effects of J_{A2_X} and J_{B2_X}. Then we define a relative jitter (RJ), which is a ratio of the jitter amount (J_{A1_X} and J_{B1_X}) to the oscillation period of the first-stage FSO ($1/F_{A1}$ and $1/F_{B1}$), and which is an important parameter affecting the TDC resolution. Actually, RJ is defined as the ratio of the oscillator cycle jitter's standard deviation to the cycle period. Figure 2 shows the TDC output spectra and the SNDR at a bandwidth of 20 kHz, obtained with MATLAB, for RJ amounts of 0.05%, 0.2%, and 0.8%. This paper utilizes the same MATLAB simulation which has been proposed in [3]. The simulation requires the FSO frequency and the RJ; we achieve these parameters from SPICE simulation. Because the jitters of the first-stage FSO are not first-order noise-shaped, the noise floor increases depending on RJ and decreases the SNDR. RJ is expected to be about 0.05% to achieve 10-bit resolution. In [4], the standard deviation of a ring oscillator's jitter (σ) model is

$$\sigma^2 = \frac{kT}{IF_0}\cdot\left(\frac{2}{V_{DD}-V_{TH}}(\gamma_N+\gamma_P) + \frac{2}{V_{DD}}\right), \tag{5}$$

where F_0 stands for the output frequency of the ring oscillator. k denotes the Boltzmann's constant. V_{TH} is a threshold voltage. In addition, T, V_{DD}, and I respectively represent the temperature, a supply voltage and a current for the oscillator. γ_N and γ_P are parameters of NMOS and PMOS. Therefore, RJ can be given as

$$RJ = F_0 * \sigma = \sqrt{\frac{kTF_0}{I}\cdot\left(\frac{2}{V_{DD}-V_{TH}}(\gamma_N+\gamma_P) + \frac{2}{V_{DD}}\right)}. \tag{6}$$

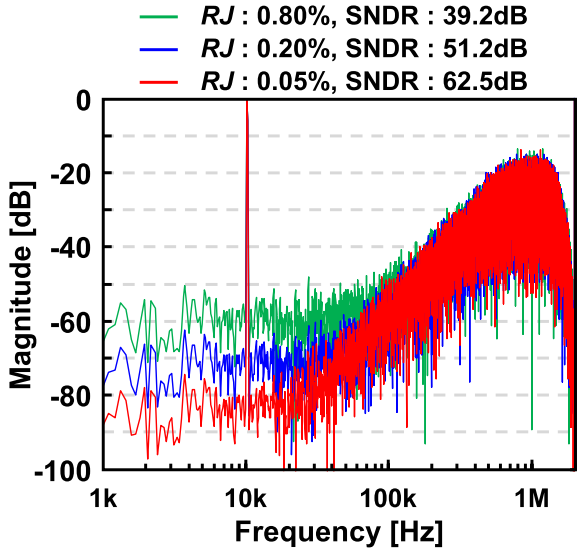

Fig. 2 Output spectra when RJ is varied.

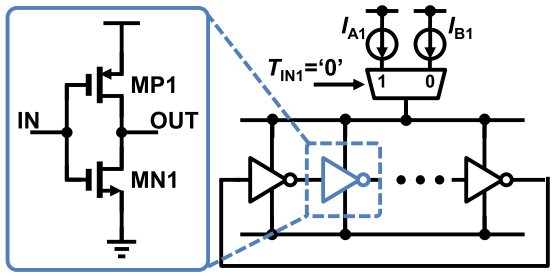

Fig. 3 Simulation model of an FSO.

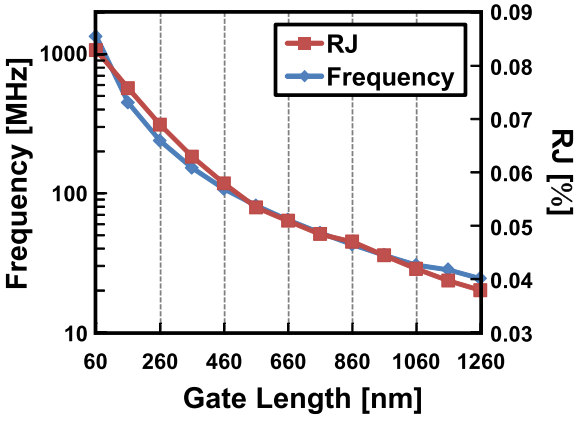

Fig. 4 Relative jitter (*RJ*) and oscillation frequency with sweeping gate length from 60 nm to 1260 nm.

From [4], F_0 is given as

$$F_0 \cong \frac{I}{MCV_{DD}}. \tag{7}$$

where C is a load capacitance of the inverter, and M is the number of oscillator stages. (6) is rewritten as

$$RJ \cong \sqrt{\frac{kT}{MCV_{DD}} \cdot \left(\frac{2}{V_{\mathrm{DD}} - V_{\mathrm{TH}}} (\gamma_{\mathrm{N}} + \gamma_{\mathrm{P}}) + \frac{2}{V_{\mathrm{DD}}} \right)}. \tag{8}$$

From (8), *RJ* is affected by C, M, V_{DD} and T. We conducted transient noise analyses in SPICE to examine the relation among *RJ*, the oscillation frequency, and the current amount with variation of the gate length of the oscillator. Figure 3 presents a simulation model of the FSO. In these simulations, the sampling rate (*SR*) is 2 MHz, the band-width (*BW*) is 20 kHz and the full-range input time interval is 250 ns.

2.1.1 Gate Length

In this simulation, the gate length of the inverters (MP1 and MN1) in the 17-stage ring oscillator is swept from 60 nm to 1260 nm. The simulation time is 200 times longer than the longest oscillator period. As presented in Fig. 4, *RJ* tends to be small for a low oscillation frequency. *RJ* with the large-gate length results in approximately 0.04%. Figure 5 shows that the lower *RJ* improves the SNDR. These simulations demonstrate that *RJ* is reduced under 0.055% and that 10-bit resolution is achievable at the slow oscillation frequency

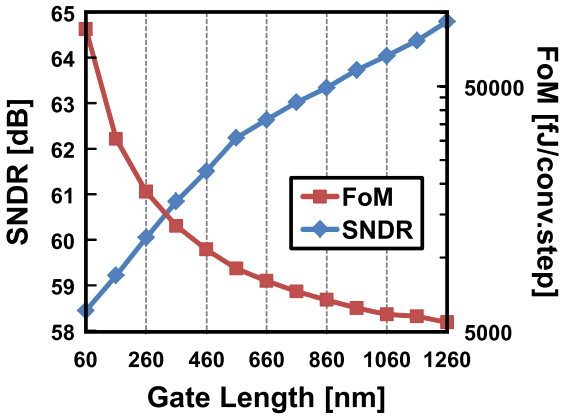

Fig. 5 SNDR and FoM with sweeping gate length from 60 nm to 1260 nm.

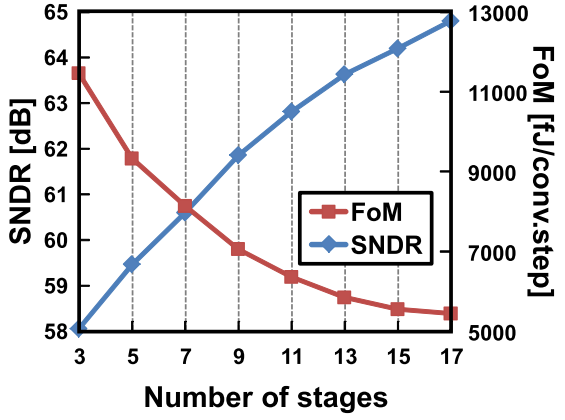

Fig. 6 SNDR and FoM with sweeping M from 3 to 17.

for 560 nm gate length. A figure-of-merit (FoM) is also depicted in Fig. 5. The FoM is improved by the large-gate inverter because the large capacitance.

2.1.2 Number of Oscillator Stages

F_0 is inversely proportional to M from (7). *RJ* is inversely proportional to the square root of M from (8). In this simulation, M is swept from 3 to 17. The gate length is 1260 nm, V_{DD} is 1.5 V, and T is 25°C. With more-stage FSO, *RJ* becomes lower. The SNDR becomes higher and the FoM are improved with more-stage FSO as presented in Fig. 6.

2.1.3 Supply Voltage

RJ is also inversely proportional to the square root of V_{DD}. In this simulation, V_{DD} in the ring oscillator is swept from 0.9 V to 1.5 V. The gate length is 1260 nm, M is 17, and T is 25°C. As higher V_{DD}, the oscillator achieves the higher frequency and the lower *RJ*. The SNDR becomes higher as V_{DD} becomes larger in Fig. 7. However the power consumption is increased at the higher V_{DD} and the FoM is worsen. There is a trade-off relationship between SNDR and FoM, when V_{DD} is swept.

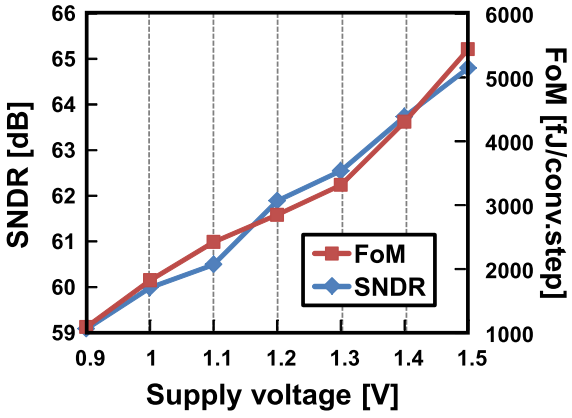

Fig. 7 SNDR and FoM with sweeping V_{DD} from 0.9 V to 1.5 V.

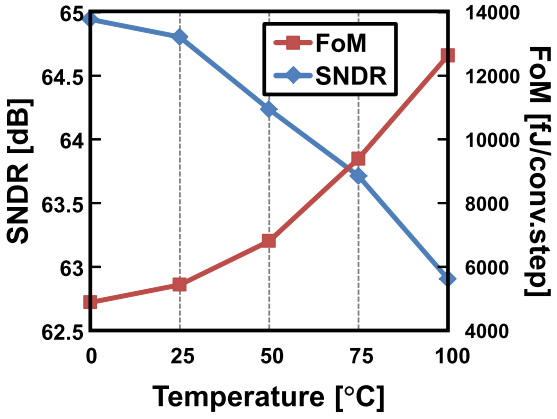

Fig. 8 SNDR and FoM with sweeping T from 0°C to 100°C.

2.1.4 Temperature

In this section, we discuss the effect of the temperature. *RJ* is inversely proportional to the square root of T. We sweep T from 0°C to 100°C. The gate length is 1260 nm, V_{DD} is 1.5 V, and M is 17. As presented in Fig. 8, at the lower temperature, the SNDR and the FoM is improved because the FSO achieves lower *RJ* and higher F_0.

2.2 Relation between FSO Frequency and Sampling Rate (F_{A1}, F_{B1}, F_{A2}, F_{B2}, and T_{CK})

When the FSO frequency becomes lower, its sampling rate in the FSOTDC must be decreased. This subsection presents discussion of the relation between the FSO frequency and its sampling rate. The FSOTDC needs at least one respective rising edge during T_{IN1} and $T_{CK} - T_{IN1}$.

QN_1 is propagated to the next stage by the QNP. Figures 9(a) and 9(b) respectively present a schematic and an example of the timing diagram in the QNP. The QNP consists of two dynamic d-type flipflops (DDFFs) and an NOR gate to avoid metastability [5]. To propagate QN_1, the QNP requires two rising edges or more in each sampling cycle. Figure 10 portrays a timing diagram with the minimum and

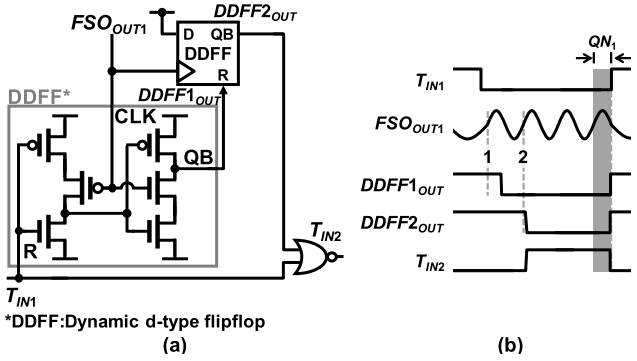

Fig. 9 (a) Schematic and (b) timing diagram of the quantization noise propagator (QNP).

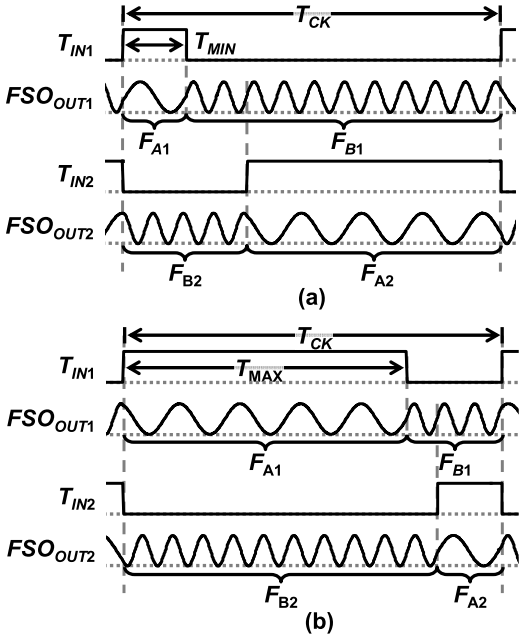

Fig. 10 Timing diagrams of (a) the minimum time interval (T_{MIN}) and (b) the maximum time interval (T_{MAX}).

the maximum T_{IN1} (T_{MIN} and T_{MAX}: $T_{MAX} - T_{MIN}$ is a dynamic range). T_{MIN} must be longer than $1/F_{A1}$. There should exist two rising edges in $T_{CK} - T_{MAX}$ and one rising edge in T_{IN2} at least. Therefore, the relation of FSO frequency and T_{MAX} is $T_{CK} - T_{MAX} > 1/F_{B1} + 1/F_{A2}$. Eventually, in the two-stage FSOTDC, the range of T_{IN1} is

$$\frac{1}{F_{A1}} < T_{IN1} < T_{CK} - \left(\frac{1}{F_{B1}} + \frac{1}{F_{A2}}\right). \tag{9}$$

2.3 Effect of Input and Clock Jitters (J_{TIN} and J_{CK})

Next, we discuss the clock jitter effect. Here, clock jitter includes T_{IN1} and T_{IN2} jitters. We define the ratio of the clock jitter's standard deviation to the T_{CK} as *RJT*. The T_{IN2} jitters (J_{LH} and J_{HL}) achieve first-order noise shaping. Therefore, we define that the *RTJ* equals J_{TIN}/T_{CK} and J_{CK}/T_{CK}. Figure 11 shows the SNDRs for *RJT* of 0.10%, 0.05%, and

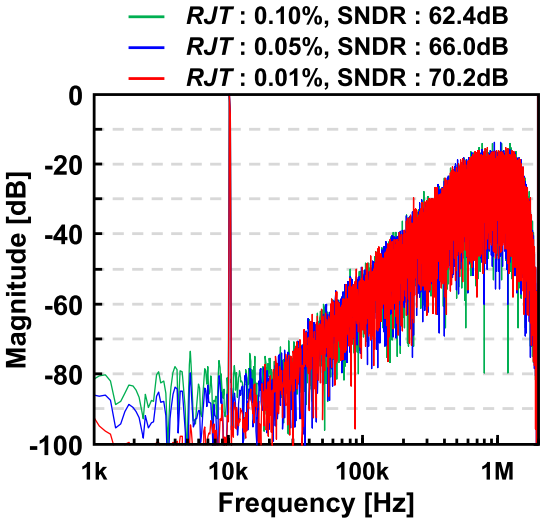

Fig. 11 Output spectra when CK jitter is varied.

0.01%. In this MATLAB simulation, *RJ* is 0% and T_{CK} is 500 ns. The noise floor increases depending on the clock jitter. Therefore, it decreases the SNDR. *RJT* should be reduced to 0.10% or less for 10-bit resolution.

3. Measurement Results of Low-Jitter FSOTDC Test Chip and Comparison to the Analyses

Based on the discussion presented in Sect. 2, we developed a low-noise FSO architecture to increase the resolution. To realize the small-area 10-bit TDC, we improve a low-noise 17-stage FSO with large-gate inverters. In SPICE simulation, the *RJ* of the ring oscillator is 0.038% considering current sources, $F_{A1,2}$ is 17 MHz, and $F_{B1,2}$ is 25 MHz.

To obtain a second-order noise shaping characteristic, the FSOTDC requires detection of the quantization noise. The FSO must oscillate sufficiently during the T_{IN1} pulse width for the QNP to operate correctly, as described in Sect. 2.2. Here, the sampling clock is 2 MHz. The full-range of the T_{IN1} is 250 ns. Figure 12 presents a MATLAB simulation result of the FSOTDC. The SNDR of 64.8 dB is achievable at a 20-kHz bandwidth. In this result, this FSOTDC achieves 10-bit resolution.

A test chip was fabricated using a 65-nm CMOS process (Fig. 13). The 1.5-V TDC core occupies 597 μm^2 as an active area. Figure 14 shows the spectra obtained from the simulated and measured output of the proposed TDC with the LMS filter. In the spectra, the input signal frequency is 10 kHz; the input width is 250 ns at a 2 MHz sampling rate. The SFDR is 75.4 dB. The SNDR is 64.5 dB, which is worse than that in the simulation because of the effect of the 1/f noise at low frequency. The test chip performance is presented in Table 1. The FSOs consume 218 μW. The QNP, peripheral buffers, and flip-flops consume 113 μW. In comparison with [3], this test chip has higher resolution because *RJ* is lower. However, the sampling rate is lower and the power consumption is increased. Therefore, the figure-of-merit (FoM) is worsened.

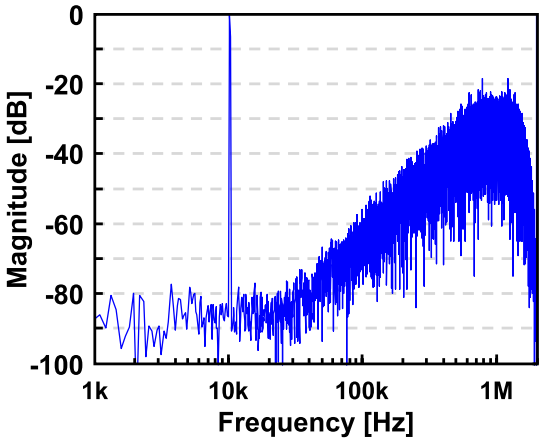

Fig. 12 Simulation result of low jitter second-order FSOTDC.

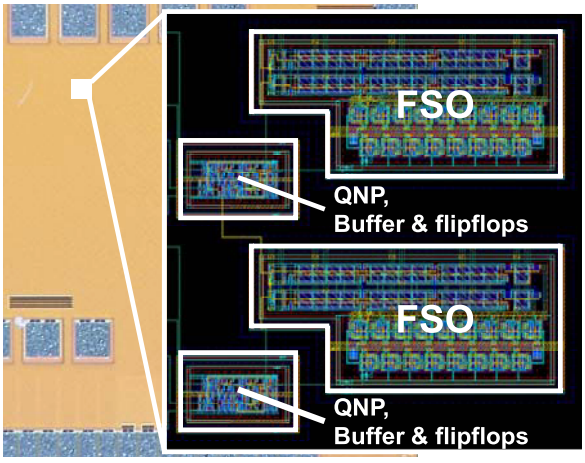

Fig. 13 Chip micrograph and layout of the 65 nm proposed FSOTDC.

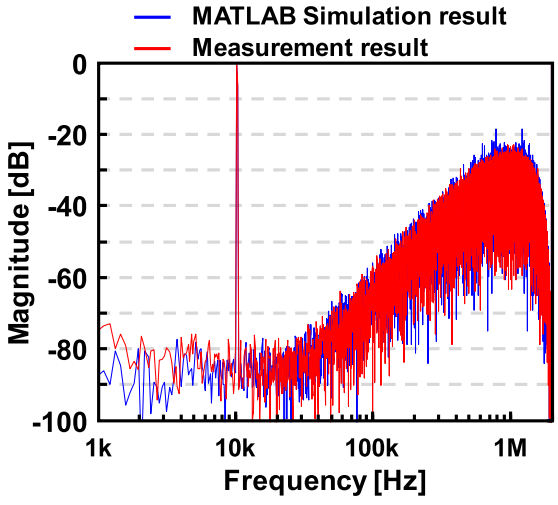

Fig. 14 Comparison of measured spectra and simulation results.

Figure 15 presents the performance of the FSOTDC using the simulation result in Sect. 2. In these simulations with

Table 1 Chip characteristics.

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Technology (nm)	65	65
Bandwidth (kHz)	500	20
Sampling rate (MS/s)	16	2
Power (mW)	0.282	0.332
SNDR (dB)	61	64.5
ENOB (bits)	9.8	10.4
Active area (mm^2)	0.0007	0.0006
FoM(fJ/conv.step)	308	6050

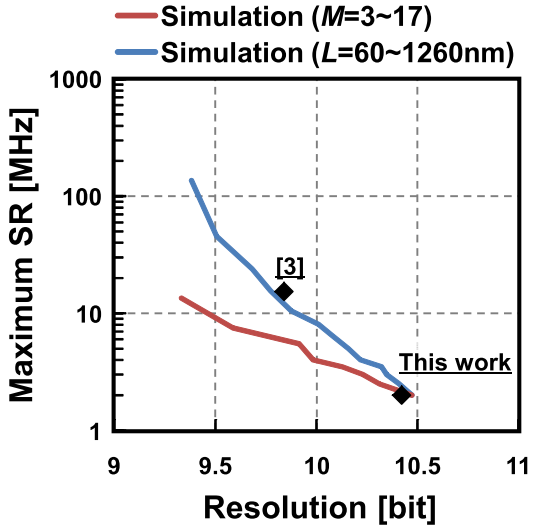

Fig. 15 Simulation and measurement results of FSO TDC performance.

sweeping gate length and M, the input width is a half of SR, SR is maximum frequency which is calculated with (9), and an oversampling rate (OSR) is 50. To achieve higher resolution the FSOTDC at the same sampling rate, one can increase the channel length and transistor width to decrease RJ.

FSOTDCs with large-gate and many-stages achieve the high ENOB. However the active area becomes larger. Figure 16 shows the relationship of the active area and the FoM at the maximum SR. And we compare the other state-of-the-art TDCs. The state-of-the-art TDCs have lower FoM, but they occupy large active area. The estimated area of the FSOTDC is calculated by using the active area. Based on these simulation results, the FoM of the FSOTDCs with the smaller-gate and fewer-stage FSOs tends to decrease. Because the FSO frequencies become higher, the maximum SR and the maximum BW are also higher. On the other hand, the ENOB at the maximum BW is increased by the large-gate inverters and many-stages FSOs. Therefore, there is a trade-off between ENOB and FoM.

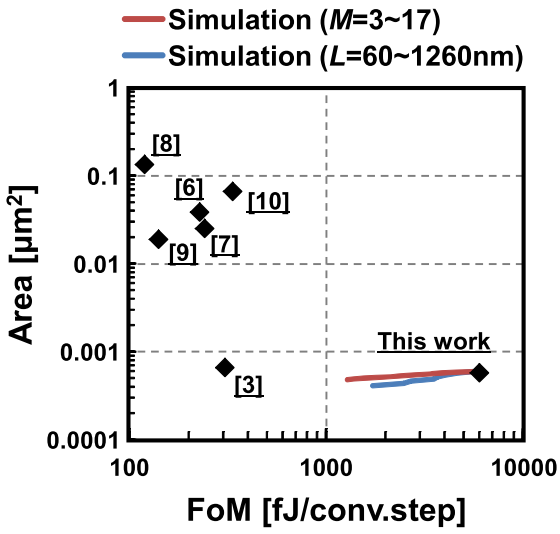

Fig. 16 Simulation results and comparison with other state-of-the-art TDCs.

4. Conclusion

By analyzing the second-order FSOTDC, we demonstrated that the noise floor of the TDC is determined by the oscillator timing jitters and that they occupy the TDC resolution. To implement lower-jitter FSO, we introduced large-gate inverter rings. In a standard 65-nm CMOS process, we designed a 10-bit FSOTDC using our design methodology. Results show that our design methodology is available for estimating FSOTDC performance by comparison to a test chip.

Acknowledgments

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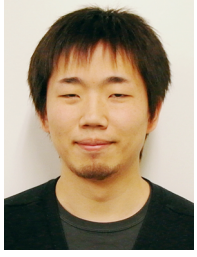

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