IEICE TRANS. FUNDAMENTALS, VOL.E98–A, NO.12 DECEMBER 2015

PAPER Special Section on VLSI Design and CAD Algorithms

A Fast Settling All Digital PLL Using Temperature Compensated Oscillator Tuning Word Estimation Algorithm*

Keisuke OKUNO[†a)], ***Student Member***, **Shintaro IZUMI**[†], ***Member***, **Kana MASAKI**[†], ***Nonmember***, **Hiroshi KAWAGUCHI**[†], ***and*** **Masahiko YOSHIMOTO**[†], ***Members***

SUMMARY This report describes an all-digital phase-locked loop (ADPLL) using a temperature compensated settling time reduction technique. The novelty of this work is autonomous oscillation control word estimation without a look-up table or memory circuits. The proposed ADPLL employs a multi-phase digitally controlled oscillator (DCO). In the proposed estimation method, the optimum oscillator tuning word (OTW) is estimated from the DCO frequency characteristic in the setup phase of ADPLL. The proposed ADPLL, which occupies $0.27 \times 0.36\,\mathrm{mm}^2$, is fabricated by a 65 nm CMOS process. The temperature compensation PLL controller (TCPC) is implemented using an FPGA. Although the proposed method has 20% area overhead, measurement results show that the 47% settling time is reduced. The average settling time at 25°C is 3 μs. The average reduction energy is at least 42% from 0°C to 100°C.

key words: *ADPLL, fast settling, digital calibration, timing error correction, temperature compensation*

1. Introduction

An all-digital phase-locked loop (ADPLL) has attracted attention in a lot of applications because of its low power consumption and small circuit area [1]–[10]. In this report, we specifically examine the settling time of the ADPLL.

In a modern wireless communication application such as sensor networks, the periodical wake-up technique is used to minimize the energy consumption [1], [2]. The average active ratio of wireless transceiver in the sensor node is less than 0.1% in ultra-low energy application such as environmental monitoring. Then, the communication power is mainly consumed by a carrier sense operation, although only several bits of preamble data are received. In such a case, the settling time of the ADPLL directly affects the system level power consumption, because the settling time is dominant in the active time. For example, when the data rate is 1 Mbps, preamble receiving time is only several μs. This duration is almost same or smaller than the settling time of the ADPLL. Unfortunately, the wireless transceiver has larger power consumption compared with other components of the sensor node.

Generally, a LC oscillator or a ring oscillator is employed in a digitally controlled oscillator (DCO) block of the ADPLL. Compared with LC oscillators, the advantages of the ring oscillator based ADPLL are small footprint and low power consumption at low frequency (less than 1 GHz). Furthermore, in recent study [11], a few-GHz ring oscillator achieves almost same or better power consumption compared with LC oscillator. Although it has larger jitter compared with the LC oscillator, the ring oscillator contributes to both the power reduction and the settling time reduction [4]. Therefore, we focused on the ring oscillator based ADPLL in this work.

The settling time of ADPLL is affected by process, voltage and temperature variations. Figure 1 shows the conventional settling-time reduction method using an oscillator tuning word (*OTW*) estimation and a gain shift of a digital loop filter. To estimate the optimum *OTW* at setup phase, the conventional method utilizes a frequency characteristic model of the DCO, which can be obtained by self-calibration in the fabrication stage to eliminate the process variation effect [6]. After the *OTW* estimation, the digital loop filter dynamically switches its filter gain coefficients according to the phase frequency detector output [2]. However, the DCO characteristic is also changed by the temperature variation. The settling time lengthens because it is difficult to reduce the effect of the temperature variation. Although the effect of the voltage variation can be reduced by a supply noise cancellation [7], [8], it is difficult to remove the temperature variation of ring oscillators. Thus, the target of this work is the temperature compensated settling time reduction.

In this paper, we propose a fast-settling ADPLL using digital calibration to compensate both the temperature and

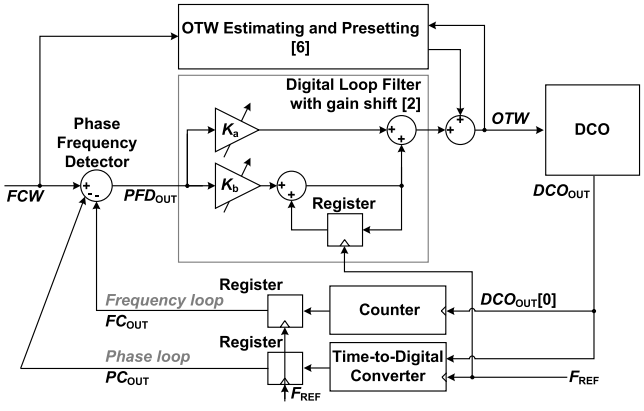


Fig. 1 Block diagram of conventional fast-settling ADPLL.

Manuscript received March 12, 2015.
Manuscript revised July 13, 2015.

[†]The authors are with the the Department of Computer Science and Systems Engineering, Kobe University, Kobe-shi, 657-8501 Japan.

*This is the extended version of the conference paper [18].

a) E-mail: okuno@cs28.cs.kobe-u.ac.jp

DOI: 10.1587/transfun.E98.A.2592

the process variation. The frequency characteristic model of the DCO for *OTW* estimation is extended to address the temperature variation. This paper is organized as follows: Section 2 describes the proposed ADPLL architecture using a digital error correction. The proposed temperature compensation scheme and its implementation are described in Sect. 3. Section 4 presents measurement results with a test chip. Finally, conclusions are drawn in Sect. 5.

2. ADPLL Architecture Using Digital Timing Error Correction

This section introduces the architecture of the fractional–N ADPLL, which has the digital timing error correction circuits and the *OTW* estimation block (see Fig. 2). The proposed ADPLL is based on a divider-less ADPLL architecture [9], [10]. The temperature compensation PLL controller (TCPC) is the *OTW* estimation block using the proposed algorithm. The detail of the TCPC and the digital loop filter are described in Sect. 3. The phase converter of the ADPLL consists of a latch and a decoder, instead of a time-to-digital converter (TDC). The phase converter can detect the fine frequency using the oscillator phases. The time resolutions of the counter and phase converter are about 417 ps and 35 ps, respectively.

A multi-phase output oscillator (MPOSC) is used to detect oscillator phase with phase couplers, because the phase couplers can improve the phase accuracy [11]. As presented in Fig. 3, the DCO consists of the MPOSC and a 16-bit resolution current source circuit. The current source is controlled with *OTW* and a bias voltage (*VBIAS*). The level shifters (LSs) which consist of the differential buffers contribute to improve the phase detection accuracy. The output signals of DCO (DCO_{OUT}) are connected to both the counter and the phase converter. The phase frequency detector compares a frequency control word (*FCW*) and the DCO frequency, which is calculated by a sum of the integral 10-bit counter output and the fractional 4-bit phase converter output. The decoded phase and frequency error (PFD_{OUT}) are filtered by the digital loop filter.

The digital loop filter and the phase frequency detector operate at the falling edge of the reference clock F_{REF}. In this report, the frequency of F_{REF} is set to 15 MHz. Then, the register in front of the DCO latches the *OTW* from the digital loop filter output at the rising edge of F_{REF}. Therefore the setup and hold errors in DFFs can be eliminated. Although the minimum timing constraint between DFFs is decreased to the half cycle of F_{REF}, the critical path in the feedback loop is sufficiently smaller than the minimum timing constraint.

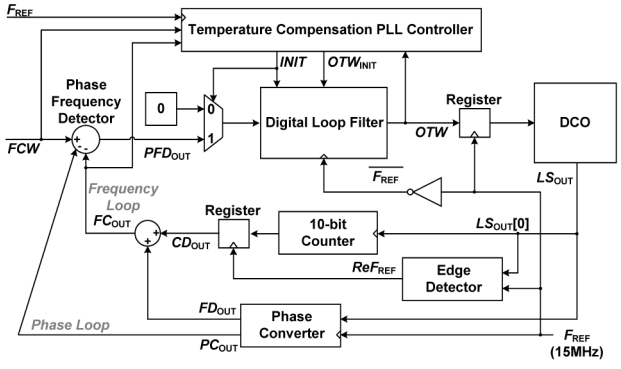


Fig. 2 Block diagram of proposed ADPLL.

2.1 Frequency Counter and Edge Detector

The coarse DCO frequency is detected by the counter. The counter has a strict timing constraint because the DCO output is connected directly. To prevent the timing error, an edge detector is implemented to generate a latch timing signal.

Figure 4 shows the block diagram and the timing diagram of the counter and the edge detector. The counter output is synchronized by $DCO_{OUT}[0]$ which has high frequency. Unfortunately, the $DCO_{OUT}[0]$ and F_{REF} are asynchronous. If the rising edge of F_{REF} is directly used in the counter, the timing error will be occurred when the rising edge of $DCO_{OUT}[0]$ is closed to the rising edge of F_{REF} (see Fig. 4(a)). To eliminate the error, the edge detector outputs the gated $DCO_{OUT}[0]$ clock (ReF_{REF}), which is kept away from the rising edge of F_{REF} as depicted in Fig. 4(b). Therefore, ReF_{REF} can be used to latch the counter value without metastability.

2.2 Phase Converter

The phase converter detects the fine frequency and the phase error by decoding the DCO_{OUT} to phase data. In other words, the phase converter operates as the TDC. As portrayed in Figs. 5 and 6, the phase converter output is used for the fine frequency tuning and the phase locking. All 12-phase DCO output signals are latched by DFFs at the rising edge of F_{REF}. Because the DCO outputs and F_{REF} are asynchronous, the phase latch output PL_{OUT} includes latch errors. PL_{OUT} is decoded to 4-bit signals (called *Phase* in

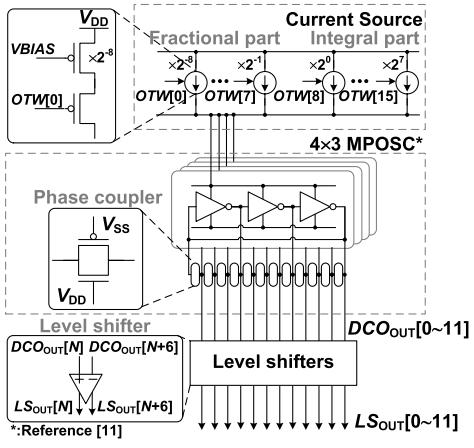


Fig. 3 Block diagram of level shifters and DCO with MPOSC.

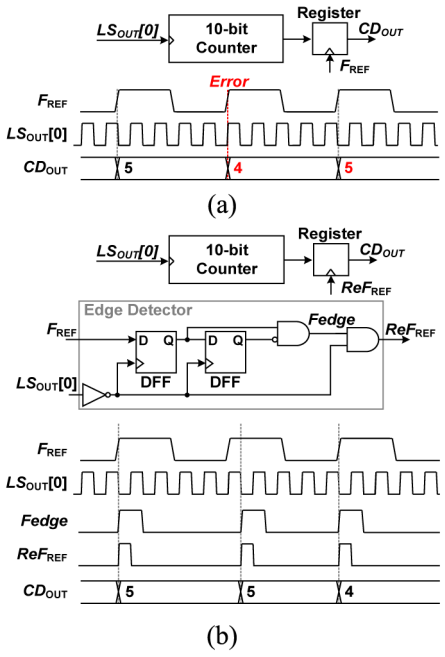


Fig. 4 Architecture and timing diagram of (a) the counter and (b) the counter with the edge detector.

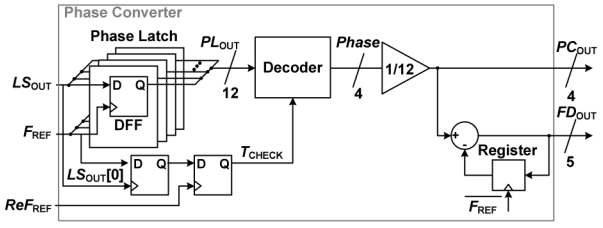


Fig. 5 Block diagram of the phase converter.

Table 1 Decoder code from PL to Phase.

PL[0]	PL[1]	PL[2]	PL[3]	PL[4]	PL[5]	PL[6]	PL[7]	PL[8]	PL[9]	PL[10]	PL[11]	Phase
L	H	X	X	X	X	X	X	X	X	X	X	0
X	L	H	X	X	X	X	X	X	X	X	X	1
X	X	L	H	X	X	X	X	X	X	X	X	2
X	X	X	L	H	X	X	X	X	X	X	X	3
⋮												
H	X	X	X	X	X	X	X	X	X	X	L	11

Figs. 5 and 6). The range of *Phase* depends on the number of the DCO output phases, which is 12 phases in this design. The decoder block can correct the latch timing error of converted data if the value of *Phase* is outside of the phase range. To eliminate the latch timing error, *Phase* is corrected using T_{CHECK}, which is determined by sampling $DCO_{\mathrm{OUT}}[0]$ at the rising edge of F_{REF}. T_{CHECK} indicates the $DCO_{\mathrm{OUT}}[0]$ state at the rising edge of F_{REF}. When the phase of $DCO_{\mathrm{OUT}}[0]$ is from $-180°$ to $0°$, T_{CHECK} is set to 0. On the other hand, when the phase of $DCO_{\mathrm{OUT}}[0]$ is from $0°$ to $180°$, T_{CHECK} is set to 1. The latch error can be determined by comparing the T_{CHECK} and *Phase*.

The decoder gain is 1/12 because the number of the DCO phase is 12. Here the phase converter output denotes the phase code (PC_{OUT}). The difference between the PC_{OUT} and the previous PC_{OUT} is the fine frequency code (FD_{OUT}). In the same manner of the digital loop filter, the phase converter output is latched at the falling edge of F_{REF}.

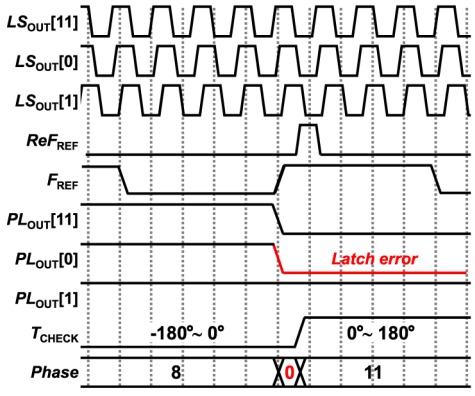


Fig. 6 Timing diagram of the latch error canceller and decoder.

3. Temperature Compensated Oscillator Tuning Word (OTW) Estimation

As described in Sect. 1, temperature variation affects the settling time. Therefore, we propose the temperature compensated *OTW* estimation technique.

3.1 Algorithm

Figure 7(a) shows the measured example of DCO temperature characteristics. As shown in Fig. 7(a), the estimated OTW_{EST} is fluctuated by the temperature. The period of oscillation in a ring oscillator can be defined by the NMOS discharging current I_{N} and the PMOS charging current I_{P} [12]. The DCO output frequency with *OTW* and F_{DCO} is given as follow;

$$F_{\mathrm{DCO}}(OTW,T)=\frac{2}{MCV_{\mathrm{DD}}}\left(\frac{1}{I_{\mathrm{N}}(T)}+\frac{1}{I_{\mathrm{P}}(OTW,T)}\right)^{-1}. \quad (1)$$

Here, C is a load capacitance of the inverter. M is the number of oscillator stages. V_{DD} is a supply voltage. Then, I_{N} and I_{P} are affected by the temperature. I_{P} is also affected by *OTW* as shown in Fig. 3.

Next, the maximum frequency of the DCO with the maximum *OTW* (OTW_{MAX}) is normalized as follow;

$$NF=\frac{F_{\mathrm{DCO}}(OTW,T)}{F_{\mathrm{DCO}}(OTW_{\mathrm{MAX}},T)}$$
$$=\left(\frac{1}{I_{\mathrm{N}}(T)}+\frac{1}{I_{\mathrm{P}}(OTW,T)}\right)^{-1}\Big/\left(\frac{1}{I_{\mathrm{N}}(T)}+\frac{1}{I_{\mathrm{P}}(OTW_{\mathrm{MAX}},T)}\right)^{-1}. \quad (2)$$

Here, the normalized frequency (*NF*) is expressed by I_{N} and I_{P}. The drain-source current I can be simplified as follow [13].

$$I(T)\cong I_{DF}\cdot\left(1-\frac{2}{\alpha_{VT}T}\Delta V_{GS}\right)=I_{DF}\cdot I_{CON}(T). \quad (3)$$

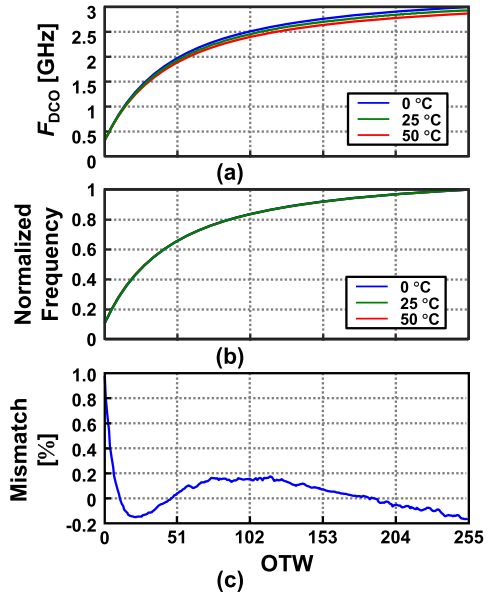


Fig. 7 (a) Temperature characteristic of DCO frequency, (b) normalized frequency with maximum *OTW* and (c) average mismatch between NF and each DCO frequency.

Here, I_{DF} is the temperature-independent part of the drain current equation. ΔV_{GS} is the deviation from V_{GSF}. The temperature dependency of the drain-source current can be negligible at V_{GSF}. V_{BIAS} can be expressed as $V_{BIAS} = V_{GSF} + \Delta V_{GS}$. α_{VT} is the temperature coefficient of the threshold voltage. $I_{CON}(T)$ is the function of the temperature. From (3), I_{N} and I_{P} can be simplify as follow.

$$\begin{aligned} I_{\mathrm{N}}(T) &\cong I_{DF\_N} \cdot I_{CON}(T). \\ I_{\mathrm{P}}(T) &\cong I_{DF\_P}(OTW) \cdot I_{CON}(T). \end{aligned} \tag{4}$$

The amount of I_{DF_P} is changed by *OTW*. According to (2), (4) can be rewritten as follow;

$$NF = \frac{\{I_{DF\_N} + I_{DF\_P}(OTW_{MAX})\} \cdot I_{DF\_P}(OTW)}{I_{DF\_P}(OTW_{MAX}) \cdot I_{DF\_P}(OTW) + I_{DF\_N} \cdot I_{DF\_P}(OTW_{MAX})}. \tag{5}$$

Finally, *NF* can eliminate the temperature effect by normalizing the DCO frequency with OTW_{MAX} as shown in Fig. 7(b). To simplify the Eq. (5), the current source consists of only pmos. If the current source is composed of both pmos and nmos, the Eq. (5) becomes more complex. In this design, OTW_{MAX} is set to 255. The DCO frequency model formula can be defined by a rational approximation using *NF*. The model formula is

$$NF = OTNF(OTW) = \frac{a \cdot OTW + b}{c \cdot OTW + d}. \tag{6}$$

Here, a, b, c, and d are constant values. These values can be calculated in the self-calibration process by a MCU using least squares method, because they are only affected by the process variation. Note that the constant values a, b, c, and d are calculated only in the initial calibration state at first time of use. The average miss match between *NF* and each DCO frequency is denoted in Fig. 7(c). When *OTW* is larger than 7, the mismatch becomes lower than ±0.2%. In other words, the frequency mismatch is about ±5 MHz. Then, the counter and the phase converter are used to scan the DCO output frequency with each *OTW*. *OTNF* in (5) is the *OTW*-to-normalized frequency function. By using this model formula, the estimation accuracy is unaffected by temperature fluctuation.

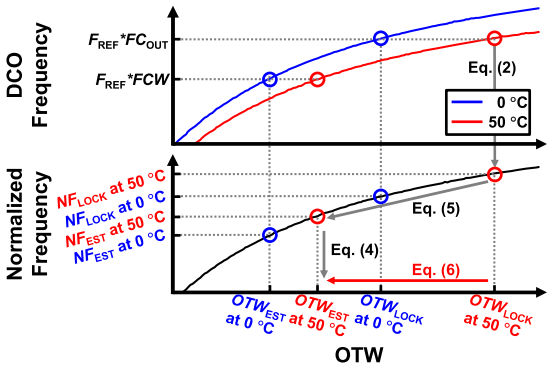


Fig. 8 TCPC algorithm to estimate an optimum *OTW*.

Next, we propose the optimum *OTW* estimation algorithm according to the DCO model formula. We present the algorithm in Fig. 8. To estimate the optimum *OTW* (OTW_{EST}), the estimation algorithm requires the previous locked *OTW* (OTW_{LOCK}) and the previous frequency code (FC_{OUT}). From (6), the previous *NF* (NF_{LOCK}) is expressed as

$$NF_{\mathrm{LOCK}} = \frac{a \cdot OTW_{\mathrm{LOCK}} + b}{c \cdot OTW_{\mathrm{LOCK}} + d}. \tag{7}$$

NF_{LOCK} is directly proportionate to FC_{OUT} because the FC_{OUT} expresses the DCO output frequency. The target normalized frequency (NF_{EST}) is also directly proportionate to *FCW*. Therefore, the ratio of NF_{LOCK} to NF_{EST} is given as follow;

$$NF_{\mathrm{LOCK}} : NF_{\mathrm{EST}} = FC_{\mathrm{OUT}} : FCW. \tag{8}$$

From (8), NF_{EST} can be derived as follow;

$$NF_{\mathrm{EST}} = \frac{FCW}{FC_{\mathrm{OUT}}} \cdot NF_{\mathrm{LOCK}}. \tag{9}$$

The OTW_{EST} can be calculated using the inverse function of (7), $OTNF^{-1}$. Therefore, the OTW_{EST} is represented as follow;

$$OTW_{\mathrm{EST}} = OTNF^{-1}(NF_{\mathrm{EST}}) = \frac{d \cdot NF_{\mathrm{EST}} - b}{-c \cdot NF_{\mathrm{EST}} + a}. \tag{10}$$

From (7), (9) and (10), the OTW_{EST} can be given as

$$OTW_{\mathrm{EST}} = \frac{d \cdot FCW \cdot A - b \cdot FC_{\mathrm{OUT}} \cdot B}{-c \cdot FCW \cdot A + a \cdot FC_{\mathrm{OUT}} \cdot B}, \tag{11}$$

Here, A is $a \times OTW_{\mathrm{LOCK}} + b$, and B is $c \times OTW_{\mathrm{LOCK}} + d$. Finally, the TCPC can estimate the OTW_{EST} using (10). The settling time of the proposed ADPLL can be reduced using

OTW_{EST}.

3.2 Implementation

This section describes the hardware implementation of the settling-time reduction using the proposed algorithm. We call the settling-time control block as the temperature compensation PLL controller (TCPC). When the target of output frequency is changed by *FCW*, the TCPC calculates the OTW_{EST} to minimize the settling time. The flowchart of the TCPC is shown in Fig. 9. As described in Sect. 3.1, the TCPC uses the digital calibration algorithm based on the frequency characteristic of DCO.

In the initialization state, the TCPC collects the frequency characteristics of the DCO. Then, *OTW* is swept from minimum *OTW* to maximum *OTW*. After that, the constant values in (6) are calculated by the processor. Next, the TCPC estimates OTW_{EST} from (11). Whenever *FCW* is changed, the TCPC calculate OTW_{EST} again.

The block diagrams of the TCPC and the digital loop filter are presented in Fig. 10. The gains of the digital loop filter, K_a and K_b, are changed according to the phase error (PFD_{OUT}). When PFD_{OUT} is larger than 3, K_a and K_b are set to 2^{-1} and 2^{-3}. When PFD_{OUT} is smaller than 3, K_a and K_b are set to 2^{-3} and 2^{-5}. The inputs of TCPC are *FCW*, FC_{OUT}, and *OTW*. The TCPC outputs two control signals, OTW_{INIT} and *INIT*. OTW_{INIT} controls the DCO frequency directly. *INIT* switches the ADPLL operation. An estimation block in the TCPC calculates (11). A TCPC controller in Fig. 10 is a sequencer, which controls the timing of output signals and the estimation block using $FLAG_{OTW}$ and $FLAG_{EST}$.

Figure 11 portrays a timing diagram of the TCPC operation. When *FCW* is changed, *INIT* becomes high and the output of the digital loop filter will be OTW_{LOCK} as presented Fig. 11(a). The TCPC detects FC_{OUT} because the estimation method requires FC_{OUT}. Next, the TCPC controller set $FLAG_{EST}$ to trigger the calculation of OTW_{EST} as shown in Fig. 11(b). Then, the estimation block calculates OTW_{EST} using (11). OTW_{EST} calculation process requires two refer-

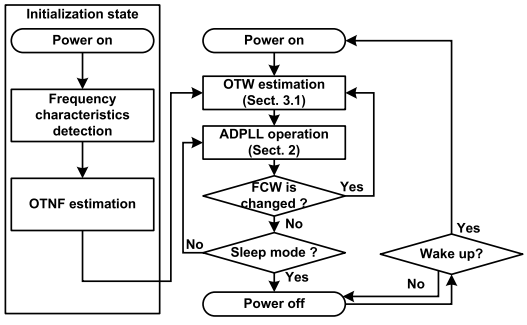


Fig. 9 Flowchart of the temperature compensation PLL controller.

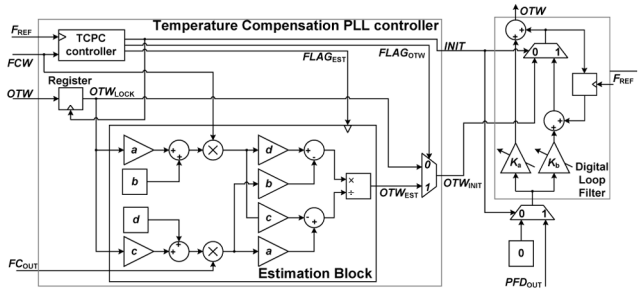


Fig. 10 Block diagram of a TCPC, a digital loop filter and a selector.

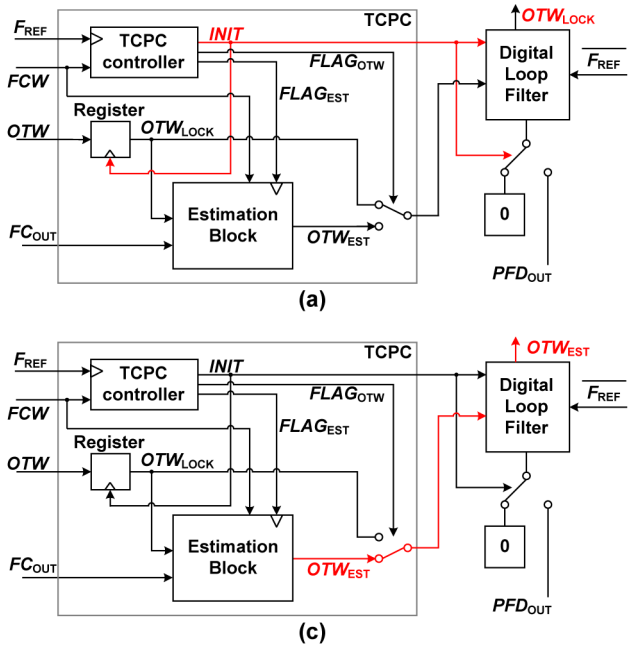


Fig. 11 Operation of the TCPC and the digital loop filter.

ence clock cycles. After that, $FLAG_{OTW}$ becomes high to output OTW_{EST}. The ADPLL receives OTW_{EST} and the output frequency is locked to the target frequency as shown in Fig. 11(c). The total cycles of the TCPC are seven reference clock cycles.

4. Performance Evaluation

A test chip is fabricated in a 65 nm CMOS process. Figure 12 presents the microphotograph and the layout plot. The ADPLL occupies $0.27 \times 0.36\,\mathrm{mm}^2$. Table 1 presents a performance of the ADPLL and the TCPC. The carrier frequency is 2.4 GHz. The total power consumption is 8.85 mW. Then, the DCO, counter, phase latch, and other circuits respectively consume 2.48 mW, 3.01 mW, 2.53 mW, and 0.83 mW. In this evaluation, the TCPC block is implemented using an FPGA. The estimated area and power estimations of the TCPC are $0.20 \times 0.10\,\mathrm{mm}^2$ and $813\,\mu$W in a 65-nm process. The power overhead and the area overhead of the TCPC are 9% and 20%, respectively. Note that the TCPC block is only activated in the setup phase of the ADPLL. Therefore, the effect of its power overhead is limited in the total power consumption of the ADPLL. Figure 13 presents a measurement result of phase noise and frequency transient with 15-MHz FREF. The phase noise is -70 dBc/Hz at 1MHz.

Figure 14 shows the measurement result of settling time of the ADPLL. F_{REF} is set to 15 MHz. In the test chip, the calculated constraints a, b, c, and d in (6) are 1.11, 2.613, 1.0, and 31.27, respectively. The blue line represents the average of five samples. The FCW is changed from 2.4 GHz to 2.415 GHz at 25°C. Here, the conventional method only using the conventional gain shift which shown in Fig. 1. As shown in Fig. 13, the phase locked time without TCPC is 7.33 μs (110 cycles). Here, the locked time means the time that PFD_{OUT} converge to less than 0.1. On the other hand, the phase locked time with the TCPC is improved to 3 μs (45 cycles). As presented in Fig. 15, even if the FCW is repeatedly changed with short duration, the TCPC can reduce the settling time correctly. The grey area shows the standard deviation. In this case, the shirt duration is every 5 μs. Table 3 presents settling times and energies at several temperatures. Then, at least 47% of the settling time is reduced. Furthermore, at least 42% of the energy consumption in the setup phase is reduced including the power overhead of the TCPC.

Figure 16 shows the measurement result of the relationship between the settling time and the estimation error. In this measurement, the OTW_{EST} is input from off-chip. From Table 3 and Fig. 16, the accuracy of the OTW estimation is smaller than 5 MHz.

Table 4 shows the performance comparison of fast settling ADPLLs. To compare with other ADPLLs, we focus

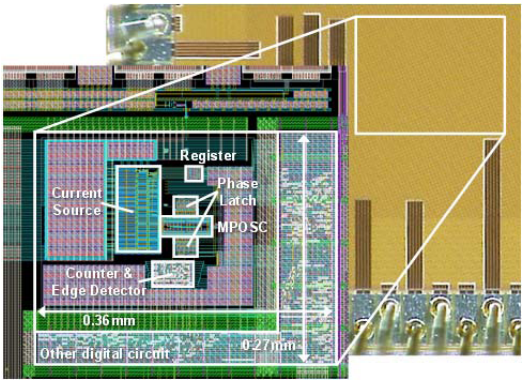


Fig. 12 Chip micrograph and layout of the proposed 65 nm ADPLL.

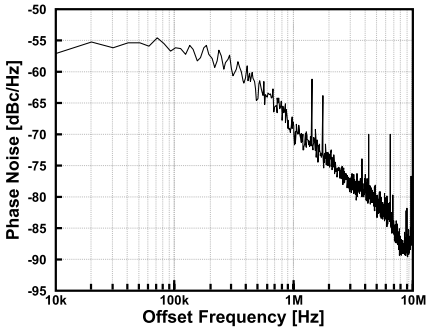


Fig. 13 Measurement result of phase noise.

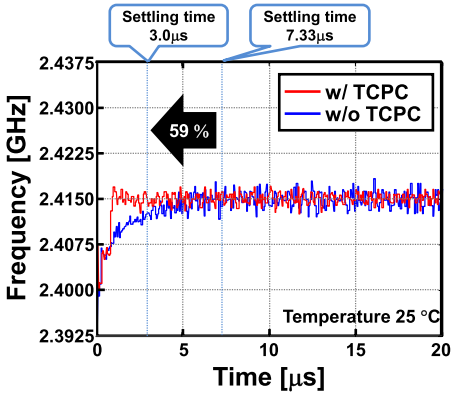


Fig. 14 Measurement results of settling time at 25°C w/o TCPC and w/TCPC.

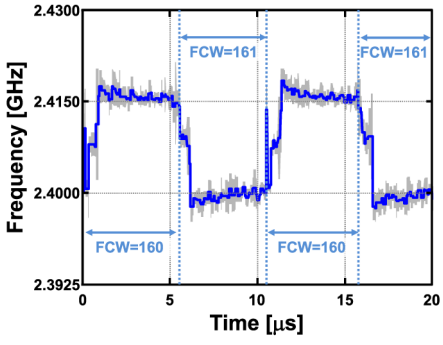


Fig. 15 Measurement result of settling time at 25°C when the FCW is changed repeatedly.

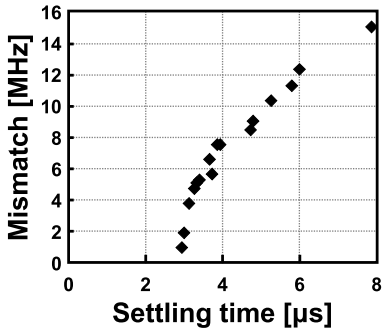


Fig. 16 Measurement result of relationship between settling time and estimation error.

Table 2 ADPLL performance summary.

			This work
Process [nm]			65
Ref. Freq. [MHz]			15
Freq. range [GHz]			1.50-2.80
FCW [bit]			16.000
Carrier Freq. [GHz]			2.40
RMS Jitter [ps]			2.23
Area [mm^2]	ADPLL		0.097
	TCPC		0.020
Power [mW]	ADPLL	DCO	2.48
		Counter	3.01
		Phase Latch	2.53
		Other circuits	0.83
		Total	8.85
	TCPC		0.81

Table 3 Settling time and energy comparison.

	Settling time [μs]		Enegy [nJ]		Reduction[%]	
Temp.[°C]	w/ TCPC	w/o TCPC	w/ TCPC	w/o TCPC	Settling time	Enegy
10	3.13	5.86	30.2	51.9	47	42
20	3.33	6.60	32.2	58.4	50	45
25	3.00	7.33	29.0	64.9	59	55
30	3.33	7.40	32.2	65.5	55	51
40	3.40	7.87	32.9	69.6	57	53
50	3.53	7.87	34.1	69.6	55	51

Table 4 Comparison of performance with other ADPLLs.

	This work	[4]	[14]	[15]	[16]
Process (nm)	65	22	28	90	90
Ref. Freq. (MHz)	15	100	50	60	30
OSC type	Ring	Ring	Ring	LC	LC
Settling time (us)	3	2.31	1	0.74	0.23
Settling cycle (cycles)	45	231	50	45	7
RMS Jitter (ps)	2.2	0.8	3	0.68	1.7
Power (mW)	9.66	3.4	0.64	9.6	8
FoM (Eq. (12))	-250.24	-249.35	-258.42	-260.46	-269.46

on the tradeoff between settling cycle and jitter. In the previous study [17], the FoM including the settling time has been proposed to consider lock time v.s. jitter trade-off. However, the settling time is affected by the reference frequency. Therefore, we use the settling cycle instead of the settling time to calculate the FoM as follows;

$$FoM = 10\log\left[\left(\frac{Jitter}{1s}\right)^2 (Settlingcycle)^2 \left(\frac{Power}{1mW}\right)\right]. \quad (12)$$

5. Conclusion

In this work, we propose the temperature variation compensated *OTW* estimation algorithm and its implementation for the fast settling ADPLL. The settling time and the energy consumption are respectively reduced by 47% and 42% at least. Because the proposed TCPC requires only the relationship between the digital code and the oscillation frequency of DCO, the proposed TCPC can be adapted to other divider-less ADPLLs using ring oscillator based DCO.

Acknowledgments

The research was supported by a Grant-in-Aid for Young Scientists (B) No. 24760279 from MEXT Japan. The chip design was supported by VDEC of The University of Tokyo in collaboration with Synopsys Inc., Cadence Design Systems Inc., and Mentor Graphics Corp.

References

[1] R.B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J.L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I.Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O.E. Eliezer, E. de-Obaldia, and P.T. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," IEEE J. Solid-State Circuits, vol.39, no.12, pp.2278–2291, Dec. 2004.

[2] R.B. Staszewski and P.T. Balsara, "All-digital PLL with ultra fast settling," IEEE Trans. Circuits Syst. II, vol.54, no.2, pp.181–185, Feb. 2007.

[3] J.A. Tierno, A.V. Rylyakov, and D.J. Friedman, "A wide power supply range, wide tuning range, all static CMOS all digital PLL in 65 nm SOI," IEEE J. Solid-State Circuits, vol.43, no.1, pp.42–51, Jan. 2008.

[4] N. August, H.-J. Lee, M. Vandepas, and R. Parker, "A TDC-less ADPLL with 200-to-3200 MHz range and 3 mW power dissipation for mobile SoC clocking in 22 nm CMOS," 2012 IEEE International Solid-State Circuits Conference, pp.246–248, 2012.

[5] V.K. Chillara, Y.-H. Liu, B. Wang, A. Ba, M. Vidojkovic, K. Philips, H. de Groot, and R.B. Staszewski, "An 860μW 2.1-to-2.7 GHz all-digital PLL-based frequency modulator with a DTC-assisted snapshot TDC for WPAN (Bluetooth Smart and ZigBee) applications," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp.172–173, 2014.

[6] G. Yu, Y. Wang, H. Yang, and H. Wang, "Fast-locking all-digital phase-locked loop with digitally controlled oscillator tuning word estimating and presetting," IET Circuits Devices Syst., vol.4, no.3, pp.207–217, May 2010.

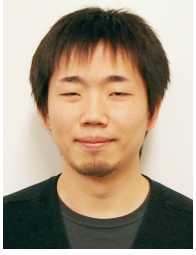
[7] A. Elshazly, R. Inti, W. Yin, B. Young, and P.K. Hanumolu, "A 0.4-to-3 GHz digital PLL with supply-noise cancellation using deterministic background calibration," 2011 IEEE International Solid-State Circuits Conference, pp.92–94, 2011.

[8] J. Liu, T.-K. Jang, Y. Lee, J. Shin, S. Lee, T. Kim, J. Park, and H. Park, "A 0.012 mm^2 3.1 mW bang-bang digital fractional-N PLL with a power-supply-noise cancellation technique and a walking-one-phase-selection fractional frequency divider," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp.268–269, 2014.

[9] M.S.-W. Chen, D. Su, and S. Mehta, "A calibration-free 800MHz fractional-N digital PLL with embedded TDC," 2010 IEEE International Solid-State Circuits Conference (ISSCC), pp.472–473, 2010.

[10] K. Takinami, R. Strandberg, P.C.P. Liang, G.L.G. de Mercey, T. Wong, and M. Hassibi, "A distributed oscillator based all-digital PLL with a 32-phase embedded phase-to-digital converter," IEEE J. Solid-State Circuits, vol.46, no.11, pp.2650–2660, Jan. 2011.
[11] T. Konishi, H. Lee, S. Izumi, T. Takeuchi, M. Yoshimoto, and H. Kawaguchi, "A low-power multi-phase oscillator with transfer gate phase coupler enabling even-numbered phase output," IEICE Trans. Fundamentals, vol.E94-A, no.12, pp.2701–2708, Dec. 2011.
[12] A.A. Abidi, "Phase noise and jitter in CMOS ring oscillators," IEEE J. Solid-State Circuits, vol.41, no.8, pp.1803–1816, Aug. 2006.
[13] I.M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., vol.48, no.7, pp.876–884, July 2001.
[14] S. Hoppner, S. Haenzsche, G. Ellguth, D. Walter, H. Eisenreich, and R. Schuffny, "A fast-locking ADPLL with instantaneous restart capability in 28-nm CMOS technology," IEEE Trans. Circuits Syst. II, vol.60, no.11, pp.741–745, Nov. 2013.
[15] J.-Y. Lee, M.-J. Park, B.-H. Min, S. Kim, M.-Y. Park, and H.-K. Yu, "A 4-GHz all digital PLL with low-power TDC and phase-error compensation," IEEE Trans. Circuits Syst. I, vol.59, no.8, pp.1706–1719, Aug. 2012.
[16] J.-Y. Lee, M.-J. Park, H.-K. Yu, and C.-S. Kim, "A 230 ns settling time type-I PLL with 0.96 mW TDC power and simple TV calculation algorithm," 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), pp.370–373, 2014.
[17] P. Paliwal, P. Laad, M. Sattineni, and S. Gupta, "Tradeoffs between settling time and jitter in phase locked loops," 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), pp.746–749, 2013.
[18] K. Okuno, K. Masaki, S. Izumi, T. Konishi, H. Kawaguchi, and M. Yoshimoto, "A 2.23 ps RMS jitter 3 μs fast settling ADPLL using temperature compensation PLL controller," 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp.68–71, 2014.

Keisuke Okuno received a B.E. and M.Eng. degree in Computer and Systems Engineering from Kobe University, Hyogo, Japan in 2011 and 2013. Currently, he is a Ph.D. candidate at Kobe University. His current research interests include digital signal processing and adaptive filters. He is a member of the IEEE.



Shintaro Izumi respectively received his B.Eng. and M.Eng. degrees in Computer Science and Systems Engineering from Kobe University, Hyogo, Japan, in 2007 and 2008. He received his Ph.D. degree in Engineering from Kobe University in 2011. He was a JSPS research fellow at Kobe University from 2009 to 2011. Since 2011, he has been an Assistant Professor in the Organization of Advanced Science and Technology at Kobe University. His current research interests include biomedical signal processing, communication protocols, low-power VLSI design, and sensor networks. He is a member of the IEEE, IEICE, and IPSJ.

Kana Masaki received a B.E. degree in Computer and Systems Engineering from Kobe University, Hyogo, Japan, in 2014. Currently, she is a master course student at Kobe University. Her current research interests include digital signal processing.

Hiroshi Kawaguchi received B.Eng. and M.Eng. degrees in electronic engineering from Chiba University, Chiba, Japan, in 1991 and 1993, respectively, and earned a Ph.D. degree in electronic engineering from The University of Tokyo, Tokyo, Japan, in 2006. He joined Konami Corporation, Kobe, Japan, in 1993, where he developed arcade entertainment systems. He moved to The Institute of Industrial Science, The University of Tokyo, as a Technical Associate in 1996, and was appointed as a Research Associate in 2003. In 2005, he moved to Kobe University, Kobe, Japan. Since 2007, he has been an Associate Professor with The Department of Information Science at that university. He is also a Collaborative Researcher with The Institute of Industrial Science, The University of Tokyo. His current research interests include low-voltage SRAM, RF circuits, and ubiquitous sensor networks. Dr. Kawaguchi was a recipient of the IEEE ISSCC 2004 Takuo Sugano Outstanding Paper Award and the IEEE Kansai Section 2006 Gold Award. He has served as a Design and Implementation of Signal Processing Systems (DISPS) Technical Committee Member for IEEE Signal Processing Society, as a Program Committee Member for IEEE Custom Integrated Circuits Conference (CICC) and IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips), and as an Associate Editor of IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences and IPSJ Transactions on System LSI Design Methodology (TSLDM). He is a member of the IEEE, ACM, IEICE, and IPSJ.

Masahiko Yoshimoto joined the LSI Laboratory, Mitsubishi Electric Corporation, Itami, Japan, in 1977. From 1978 to1983 he had been engaged in the design of NMOS and CMOS static RAM. Since 1984 he had been involved in the research and development of multimedia ULSI systems. He earned a Ph.D. degree in Electrical Engineering from Nagoya University, Nagoya, Japan in 1998. Since 2000, he had been a professor of Dept. of Electrical & Electronic System Engineering in Kanazawa University, Japan. Since 2004, he has been a professor of Dept. of Computer and Systems Engineering in Kobe University, Japan. His current activity is focused on the research and development of an ultra-low power multimedia and ubiquitous media VLSI systems and a dependable SRAM circuit. He holds on 70 registered patents. He has served on the program committee of the IEEE International Solid State Circuit Conference from 1991 to 1993. Also he served as Guest Editor for special issues on Low-Power System LSI, IP and Related Technologies of IEICE Transactions in 2004. He was a chair of IEEE SSCS (Solid State Circuits Society) Kansai Chapter from 2009 to 2010. He is also a chair of The IEICE Electronics Society Technical Committee on Integrated Circuits and Devices from 2011–2012. He received the R&D100 awards from the R&D magazine for the development of the DISP and the development of the realtime MPEG2 video encoder chipset in 1990 and 1996, respectively. He also received 21th TELECOM System Technology Award in 2006.